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# Practical guide for in-house solid-state nanopore fabrication and characterization

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## ABSTRACT

Solid-state nanopores are considered a better alternative to biological nanopores for several sensing applications due to their better chemical, mechanical, and temperature stability. In addition to sequencing, nanopores currently also find applications in education, biomarker identification, quantification, single-molecule chemistry, and DNA computing. Nanopore technology's simplicity and wide interdisciplinary applications have raised further interest among industry and scientific community worldwide. However, further development in solid-state nanopore technology and exploring its applications presents the need to have the capability to fabricate them in-house. This will be a more financially viable and flexible approach, especially in resource-limited situations. In order to do an in-house fabrication of solid-state nanopores, two key steps are involved. The first step is to fabricate suspended thin films, and the second one is the drilling of pores in these suspended thin membranes. Successful implementation of these two steps involves tedious optimization and characterization of the fabricated chips and nanopores. In this work, we describe the nanopore fabrication process in a ready-to-follow step-by-step guide and present solutions for several practical difficulties faced during the silicon nitride pore fabrication process. This work will help anyone new to this field and make the pore fabrication process more accessible.





## I. INTRODUCTION

Solid-state nanopore technology has received much interest due to numerous advantages, such as robustness and large-scale integration capabilities over their biological counterpart. The solid-state nanopores are currently being explored in various applications, such as protein and DNA sequencing, DNA computing, biomarker identification, quantification, and single-molecule chemistry.[1] Owing to the diversity in applications, low complexity of the technique, and expected enormous impact on science and society, several research groups and industries worldwide have begun working in solid-state nanopore technology, including biology and material science, to computing streams.[2–4] However, the complete process, including nanopore fabrication and translocation measurements, is riddled with enormous practical challenges. Other problems include relatively high prices and increased waiting time for the delivery of commercial solid-state nanopores. Overcoming these challenges requires developing in-house nanopore fabrication expertise, which helps to quickly customize the nanopore to meet the specific research requirements. Optimizing the fabrication protocols and conducting successful translocation measurements will take time, money, and effort, as several practical challenges could arise in the fabrication process (Fig. 1). These are usually not explicitly discussed in the existing solid-state nanopore-related literature, increasing the difficulties for novices in the field. This work addresses these problems by giving a ready-to-follow, step-by-step protocol to fabricate a silicon nitride nanopore starting from a bare silicon wafer.

## II. FABRICATION PROTOCOLS

The entire fabrication process of silicon nitride nanopores involves two major steps (Fig. 2), which are (1) suspending a thin silicon nitride membrane and (2) fabrication of nanopores (in this case sub-10 nm diameter). Proper optimization of these two steps is essential for precisely controlling the pore size and thickness. This helps achieve better spatial and temporal resolution, enabling a high signal-to-noise ratio during translocation measurements for single molecular sensing.

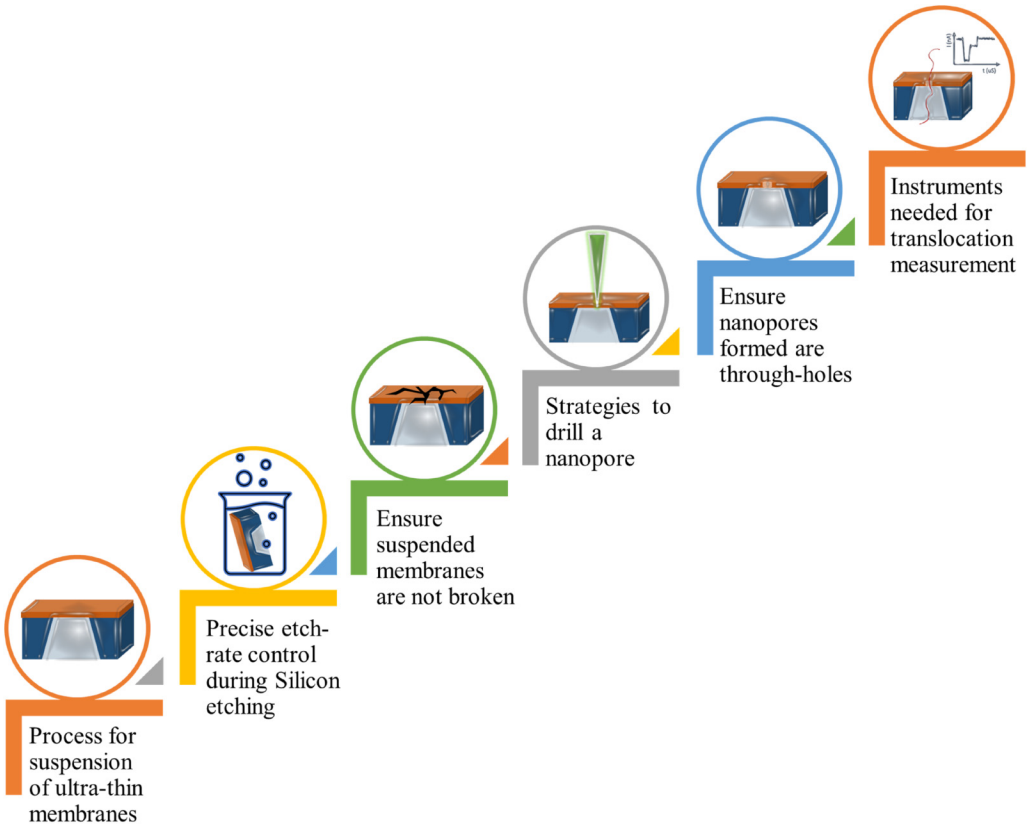


**FIG. 1.** Graphical representation of the challenges encountered when establishing an in-house solid-state nanopore fabrication process.



## A. Suspending silicon nitride membrane

The thin silicon nitride membrane can be successfully released by careful optimization and tuning of parameters involved in this step, which otherwise will lead to membrane failures. Sections II A 1–II A 5 have detailed the silicon nitride membrane suspension starting from a bare silicon wafer.

### *1. Procuring silicon wafers and cleaning techniques*

Silicon wafers are available in a wide range of sizes, generally from 2- to 12-in. wafers. These wafers can also be customized and procured as per the requirement. The details of standard silicon wafers are given in Table I.

For the current fabrication protocol, 2-in. n-type Si (100) wafers were chosen taking into consideration the fabrication tool constraints and the ease of wafer handling. For instance, choosing a wafer of lower thickness gives the advantage of less time required for etching bulk silicon using KOH. Also, the TEM (transmission electron microscopy) sample holder in our facility can easily accommodate the thickness of ~300 um silicon substrate for the fabrication of nanopores. The wafers were procured from Silicon Valley Microelectronics (Single side polished wafers) and WaferPro (Double side polished wafers). The membrane fabrication process is undertaken in the National Nanofabrication Centre at the Centre for Nano Science and Engineering (CeNSE), a research facility located at the Indian Institute of Science, Bangalore.

Before starting any device preparation processes, the newly procured wafers are recommended to be cleaned using a standard cleaning procedure used in the semiconductor industry. This standard cleaning procedure is a two-step process. The first step involves performing an RCA-1 clean or Standard clean-1 on the freshly procured wafers. This step comprises immersing these wafers in a mixture of 1:1:5 vol. % $H_2O_2$:$NH_4OH$:$H_2O$ at 80 °C for 10 min. This procedure helps in cleansing organic residues and films from the silicon wafers. The second step in the cleaning procedure is called RCA-2 or standard clean-2. This step comprises immersing these wafers in a mixture of 1:1:5 vol. % $H_2O_2$:HCl:$H_2O$ at 80 °C for 10 min. This step ensures that the wafers are cleansed of any metallic contamination that could have been present. The cleaning of the wafers is followed by a 30 s dip in a mixture of 1:50 vol. % of HF:$H_2O$ to eliminate any thin silicon dioxide film that would be present on the surface of the Silicon wafers. It is to be noted that after each step, the wafers are thoroughly rinsed with de-ionized water (DI) water and blow-dried well with nitrogen gas before going for the membrane deposition process.

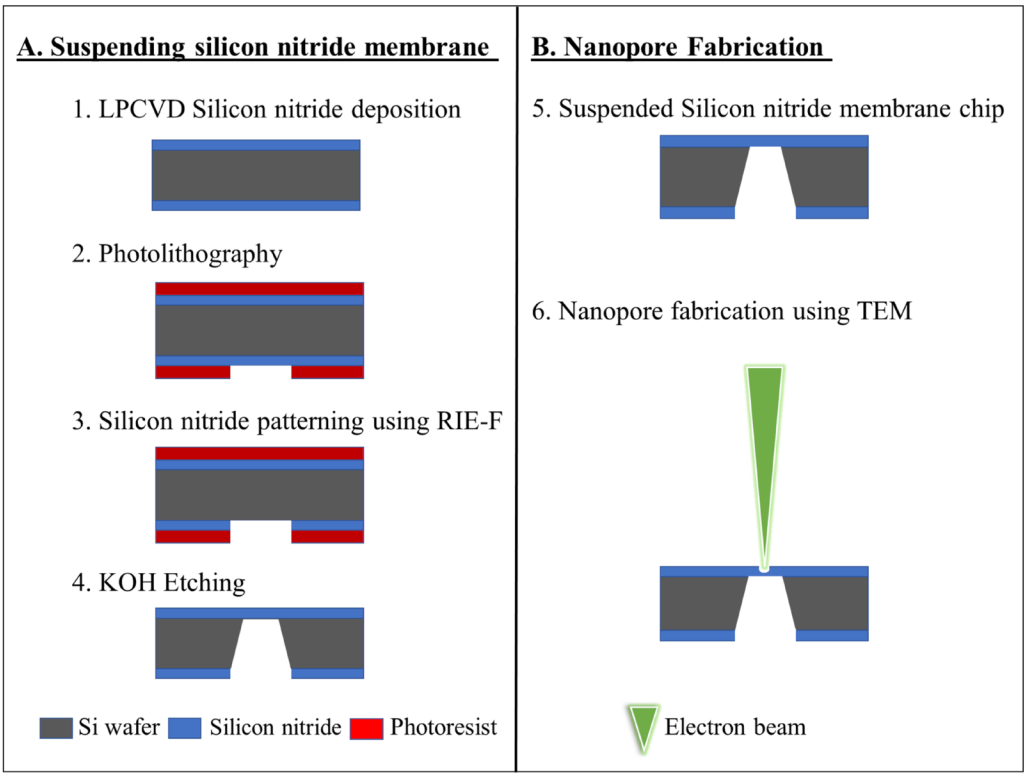


**FIG. 2.** Schematic illustration of the complete silicon nitride nanopore fabrication process. (a) Process flow for suspension of thin silicon nitride membranes. (b) Process flow for fabrication of nanopores in the suspended silicon nitride membranes using TEM.



### 2. Silicon nitride coating on a silicon wafer

After cleaning the silicon wafers, the immediate process is depositing low-pressure chemical vapor deposition (LPCVD) silicon nitride on both sides of the cleaned silicon wafer. This is crucial to prevent the formation of a thin silicon oxide layer on the bare wafer. LPCVD is a high throughput method for fabricating stable silicon nitride membranes. The silicon nitride layer deposited is mostly uniform and conformal at pressures below 1 Torr.[5] Silicon nitride has been chosen as the membrane material due to its popularity and compatibility with most semiconductor processes. These films are amorphous, stable against oxidation, dense, and provide a good barrier against moisture penetration.[6] As specified earlier, we will be using a 2-in. silicon wafer given that it is easy to handle, cheap, and of less thickness (~290 um), which will help reduce the overall process time to achieve membrane suspension. The LPCVD deposition process in the current fabrication protocol involves depositing silicon nitride film of thickness 30 nm on both sides of the bare Si wafer. The deposition is done at a temperature and pressure of 750° and 200 mTorr. Dichlorosilane (DCS) and ammonia ($NH_3$) are the source gases used with a gas flow rate of DCS: $NH_3$ = 10:70 sccm. The deposited silicon nitride film of thickness 30 nm was measured and verified to be uniform throughout the Si wafer using Ellipsometry (J. A. Woollam) with a standard deviation of 0.2 nm. The LPCVD can be followed by an annealing process, which can significantly reduce the residual stress as reported.[7] A high temperature annealing (~1000 °C) is required to reduce the residual stress considerably. We have not carried out an annealing process after LPCVD, as it can possibly increase the roughness of surface.[7]

**TABLE I.** Details of standard silicon wafers.

| Types of wafers (in.) | Thickness (um) |
|---|---|
| 2 | 275 |
| 3 | 375 |
| 4 | 525 |
| 6 | 675 |
| 8 | 725 |
| 12 | 775 |

### 3. Optical lithography for pattern transfer

After the silicon nitride thin film is deposited on the wafers, the next step is the process of creating patterns on silicon

nitride-coated wafers. This can be done by transferring patterns using optical lithography. For this, a positive photoresist (PR) (AZ5214E) is coated on the wafer using a spin coater (Laurell H6-23 Spin Coater). The spin coating process is performed with the conventional parameters of 4000 rotations per minute (rpm) for a duration of 40 s. After coating, the photoresist-coated wafer is soft baked for 1 min at 110 °C to remove photoresist solvents. The designed mask is then patterned on to the photoresist-coated wafer using a direct writing tool (Heidelberg UPG 501) that writes the pattern directly onto the substrate using a focused laser beam (exposure wavelength: 390 nm). This mask is designed to fabricate chips of 3 $\times$ 3 $mm^2$ throughout the 2-in. wafers having circles of diameter ~500 um at the center. This chip dimension has been chosen to make it compatible with our TEM facility for pore fabrication. The standard TEM sample holder can contain a sample of 3 mm diameter size and can be customized to hold larger sizes such as 8 mm. The layout for pattern writing can be designed on any layout editor tool, such as CleWin.[8] If required, a model mask design for nanopore can be downloaded from our research group website (https://sites.google.com/view/nanoporegroup/resources). Once the direct writing is completed, the substrate is dipped in the developer solution to remove the PR from exposed areas. We have used the MIF726 developer for the same, and it may take nearly 30 s for the development process to complete. These recipes were optimized for a temperature of 20 °C and relative humidity of 45 in a class 100 cleanroom. Once the development is complete, the PR-patterned samples are hard baked for 3 min at 110 °C to drive off any remaining solvents or moisture from the sample surface.

### 4. Backside silicon nitride removal prior to wet etching

The LPCVD silicon nitride is deposited on both sides of the bare Si wafer. To release membranes, we need to pattern the thin silicon nitride film from the PR-patterned side of the wafer to facilitate Si etching. Reactive ion etching based on fluorine chemistry can be used for patterning the thin layer of Silicon nitride. The Plasma lab systems 100 from Oxford Instruments are used for the dry etching using $CHF_3$ and $O_2$ gases (1:10 gas ratio). The recipe was optimized for a temperature and pressure of 20 °C and 55 mT. Once patterned, this thin silicon nitride layer will act as a hard mask during silicon etching.

### 5. Wet etching for suspending silicon nitride membrane

Once the etching patterns are formed on the silicon nitride hard mask, the membranes can be suspended by etching the silicon from the backside using dry or wet etching techniques or an optimized combination of both. The classic dry etching technique to etch out all 280 um or a significant part of the 280 um thick silicon is to use a deep reactive ion etching (DRIE) tool. The process involves using gases $SF_6$ and $C_4F_8$ and is done at a temperature and pressure of −10 °C and 200 mT with a gas ratio of 1:2.4. The etch rate of silicon was measured as ~37 um/min using a Dektak XT Surface profiler. This high etch rate gives us less control over the etching when we approach the membrane, causing membrane failure for almost all chips. This is a key argument for not utilizing

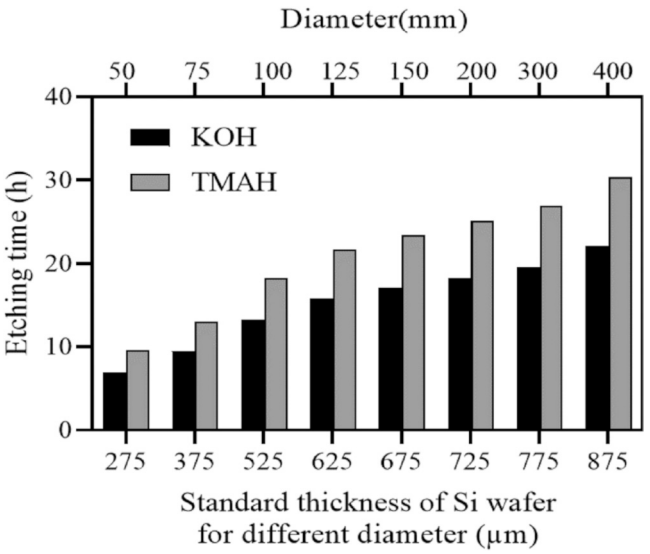


**FIG. 3.** Etching time to form through holes in different thickness silicon wafer using 5 wt. % TMAH and 20 wt. % KOH at 70 °C. Reprinted from Pal *et al.*, Micro Nano Syst. Lett. **9**(1), 4 (2021). Copyright (2021) Springer Nature under a Creative Commons License.

the dry etching technique to completely etch the silicon out of the etch pattern.

The typical technique for silicon wet etching is to use the potassium hydroxide solution (KOH)/tetramethylammonium hydroxide (TMAH) solution. The etching times of both solutions are compared in Fig. 3.[9]

These wet etching techniques are well-established anisotropic etching processes due to the dependence of the silicon etch rate on the temperature and concentration of the etchant solution and the crystal plane orientation, allowing precision in the geometry of the structures to be fabricated. This gives us better control over the etching than the dry etching technique when we etch close to the membrane and helps us ensure successful membrane suspension in most devices. We have used the KOH etching protocol to remove the silicon from the patterned area. A 30% KOH solution by weight is used for the process (EMPARTA Potassium Hydroxide Pellets, DI water). The standard KOH etching process requires the solution to be consistently maintained at 70 °C for approximately 7 h, as shown in Fig. 3. To avoid this time-consuming procedure, we have divided the process into two steps of KOH etching carried out at two different temperatures. The first step involves etching at 90 °C for 1 h 45 min, followed by etching done at 80 °C for 1 h 50 min. The temperature specified here is the temperature of the solution. This is controlled using standard hot plates (IKA C MAG H7 Hotplates). A single etching step of maintaining the solution at 90 °C for 2 h 30 min also works given that you control the stirring well, reducing the chances of membrane damage (Fig. 4). The details of the etching setup and devices used for precise temperature controller are discussed in Sec. IV.

Alternatively, a combination of DRIE and KOH etching processes can be optimized and adapted to achieve successful silicon

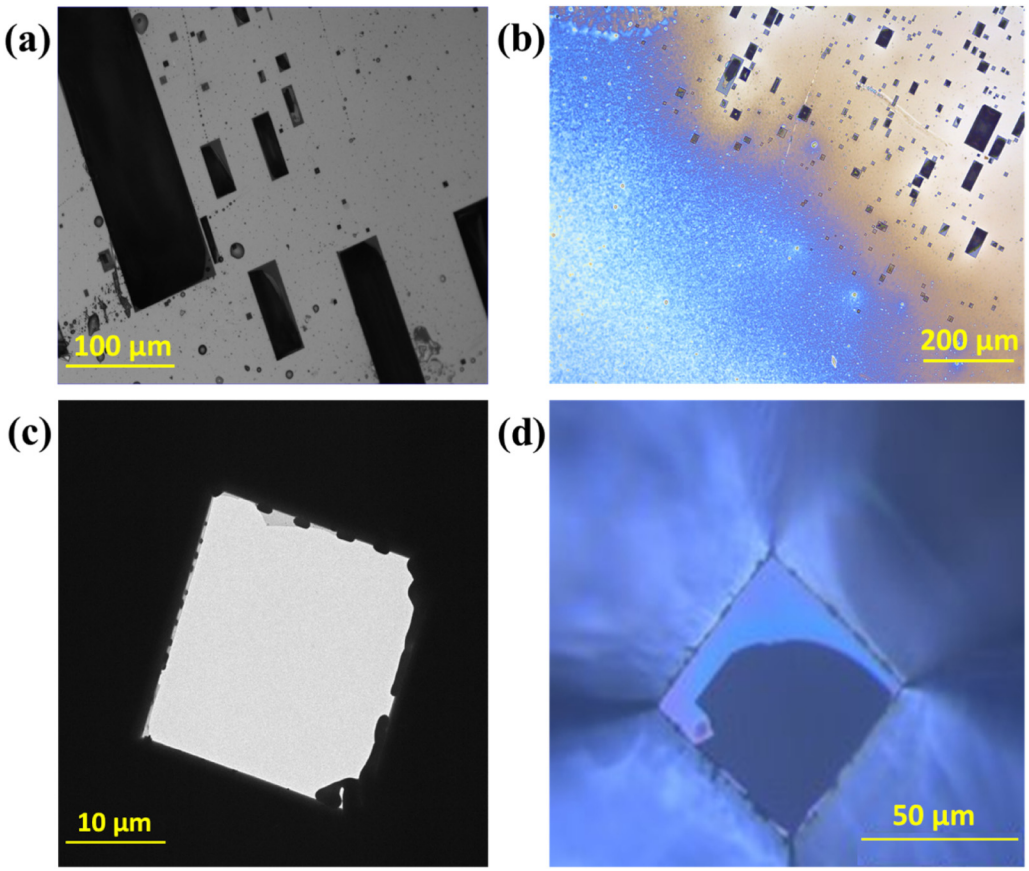




**FIG. 4.** (a) and (b) Optical microscope images of multiple microslit formations. (c) TEM image of the broken membrane. (d) Optical microscopy image of the broken silicon nitride window.

etching. For this, it is recommended to perform dry etching using DRIE [SPTS LPX Pegasus DRIE system] for 6.5 min and then wet etching in 30% vol KOH solution at 80 °C for 45 min. The etching time required for DRIE and KOH Etching has been measured using a Dektak XT Surface profiler. The etching patterns in the hard mask need to be designed accordingly. This method ensures a quick initial etching that saves time for the fabricator and then a slow and more controlled etching as we etch closer to the membrane, thus taking care that fewer membranes are damaged.

Once the membrane is suspended successfully (Fig. 5) and is confirmed by observing through an optical microscope, dipping the sample in isopropyl alcohol for 3 min and in DI Water for 1 min is advised to clean the chip.

### B. Nanopore fabrication using TEM

TEM-based nanopore fabrication is the most precise nanopore fabrication technique currently available,[10] and it is a well-established technique.[2,11] Even though dielectric breakdown-based nanopore fabrication[12] is emerging, lack of control over the location and size of the nanopore is still a significant problem. Unlike other tools, TEM provides live visual confirmation of pore formation and has several applications in the solid-state nanopore domain, from pore drilling to bioimaging.[10] The conventional sample size for TEM is 3 mm, even though it can be customized up to 8 mm diameter samples. We have used a transmission electron microscope (Titan Themis 300 kV from Thermofisher Scientific) for pore fabrication, which is available in the Micro and Nano characterization facility at CeNSE, Indian Institute of Science, Bangalore.[13] The nanopore can be drilled in approximately half a minute by electron beam exposure (Fig. 6). Although operational values of TEM to drill a nanopore vary from instrument to instrument, it is helpful to have an idea about the parameters, such as the size of the beam, dosage (number of electrons falling on a unit area of the thin film), and intensity for the reproduction of exact pore sizes. Usually, an accelerating voltage of 200 or 300 kV is commonly used for the fabrication of nanopores. The electron beam with an intensity of $10^8$–$10^9$ e/nm$^2$ s with full width half maxima of 2–10 nm is tightly focused on the silicon nitride membrane to drill a nanopore of size ranging 3–6 nm. Defocused beams can be used

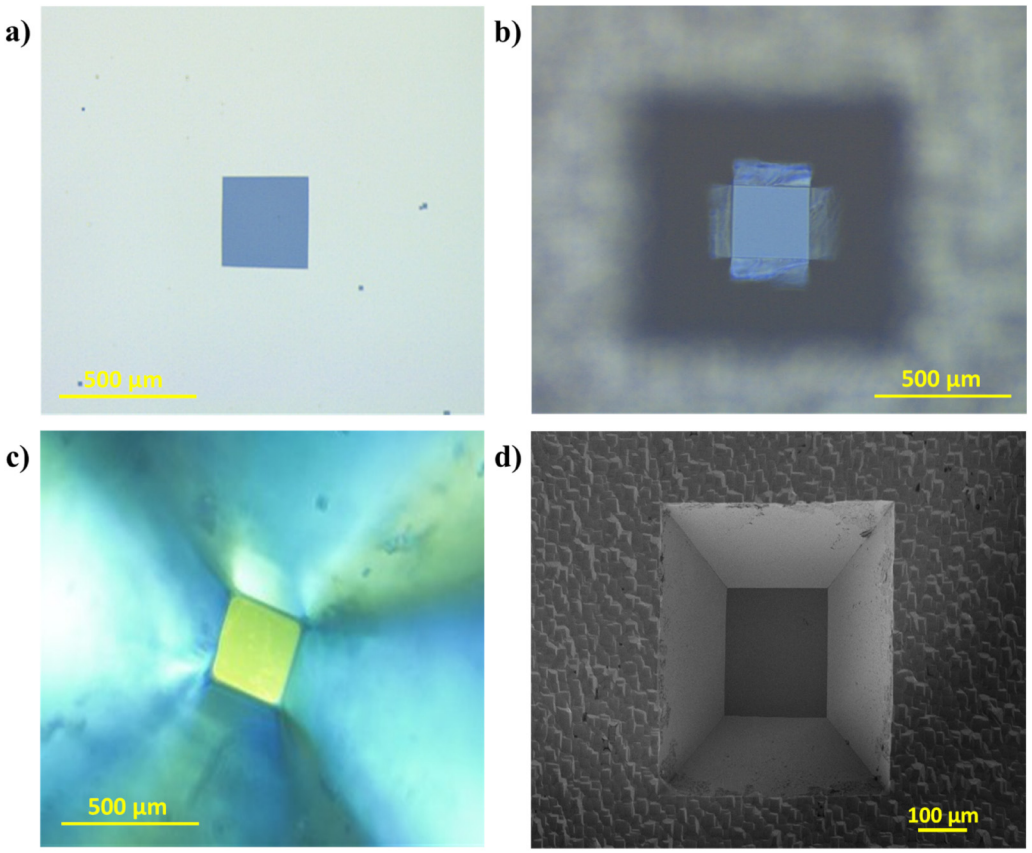


**FIG. 5.** Suspended silicon nitride membrane under the optical microscope: (a) top view, (b) bottom view, (c) suspended membrane imaged using differential interference contrast mode of the optical microscope, and (d) SEM image of KOH etched area.



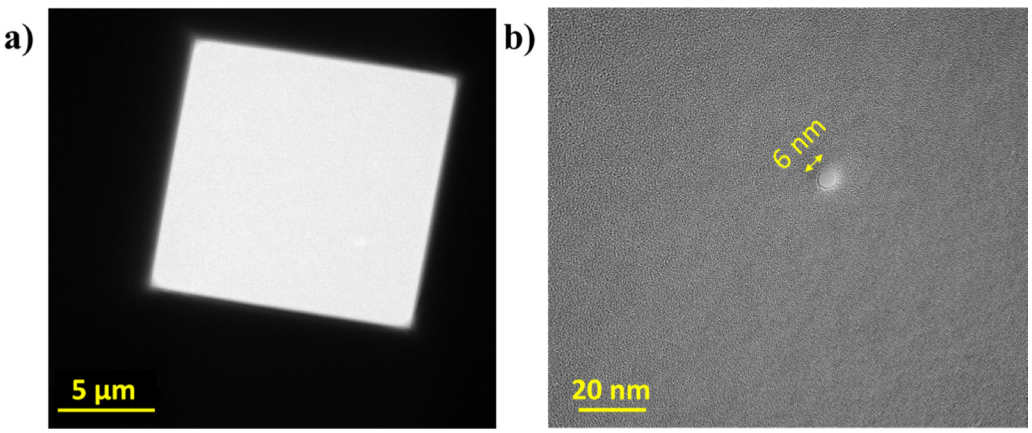


**FIG. 6.** (a) TEM image of the suspended silicon nitride window. (b) 6 nm pore fabricated using TEM.

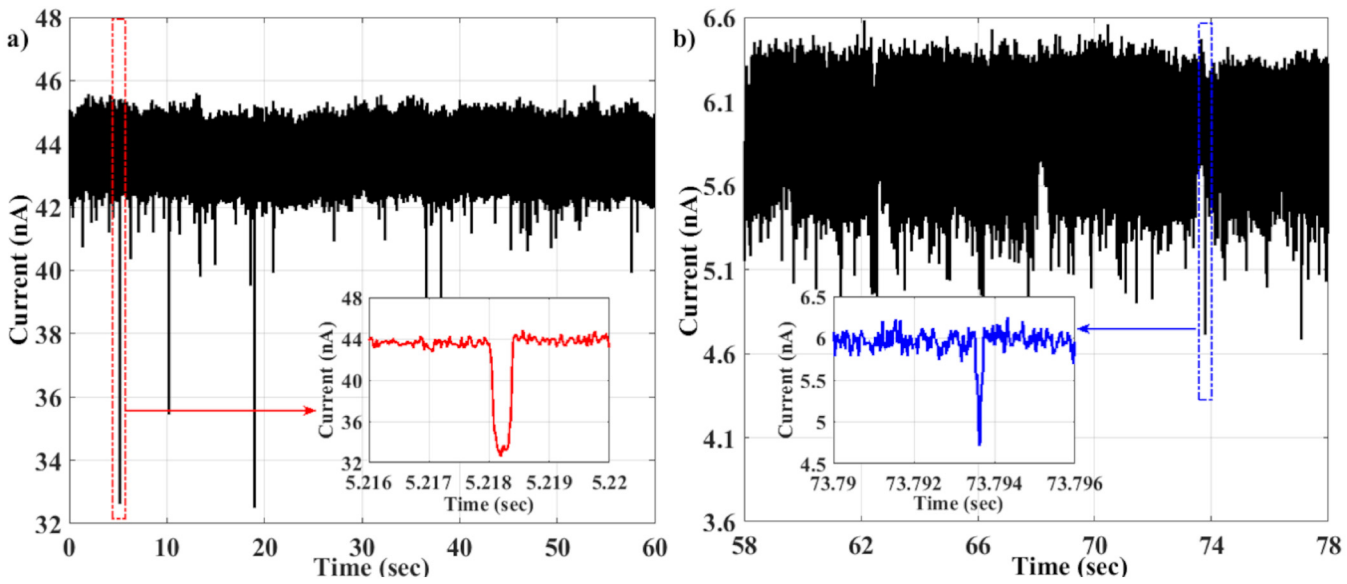


**FIG. 7.** (a) Current measurement data of translocation of 6HB through the nanopore (raw data). Inset shows the zoomed in detail of a single event. (b) Current measurement data of translocation of DNA Duplex through the nanopore (raw data). Inset shows the zoomed in detail of a single event.

to enlarge (if needed) and to fine-tune the size and shape of the pore. The theory and experimental aspects of electron beams assisted nanopore fabrication are explained in detail in an earlier review paper from our group.[10]

## III. DETECTION OF TRANSLOCATION OF BIOMOLECULES USING THE FABRICATED NANOPORE

The sensing capability of solid-state nanopores fabricated using the protocol explained in this work is shown in this section.



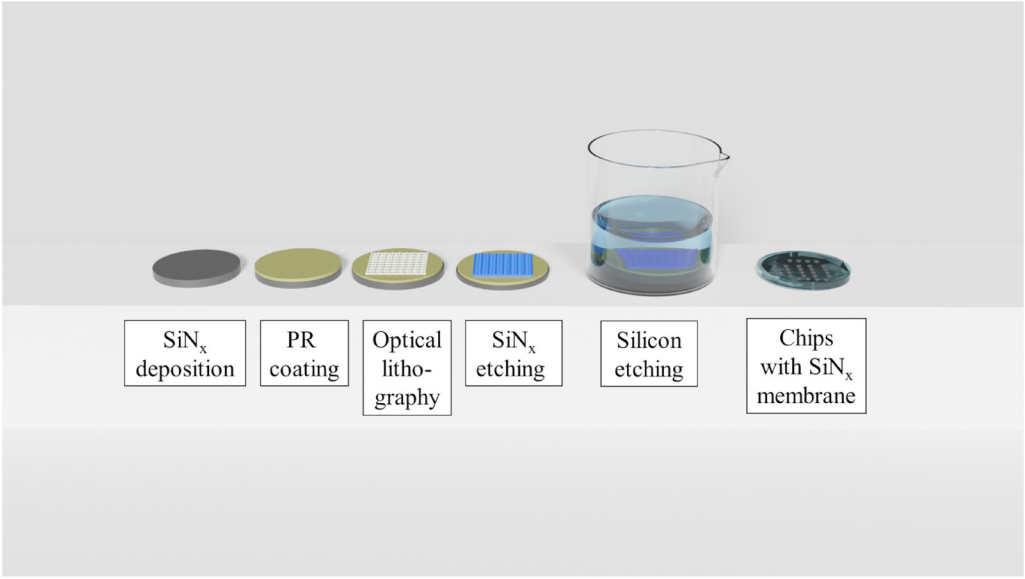


**FIG. 8.** Simple schematic of the cleanroom fabrication process for membrane suspended TEM compatible chips.

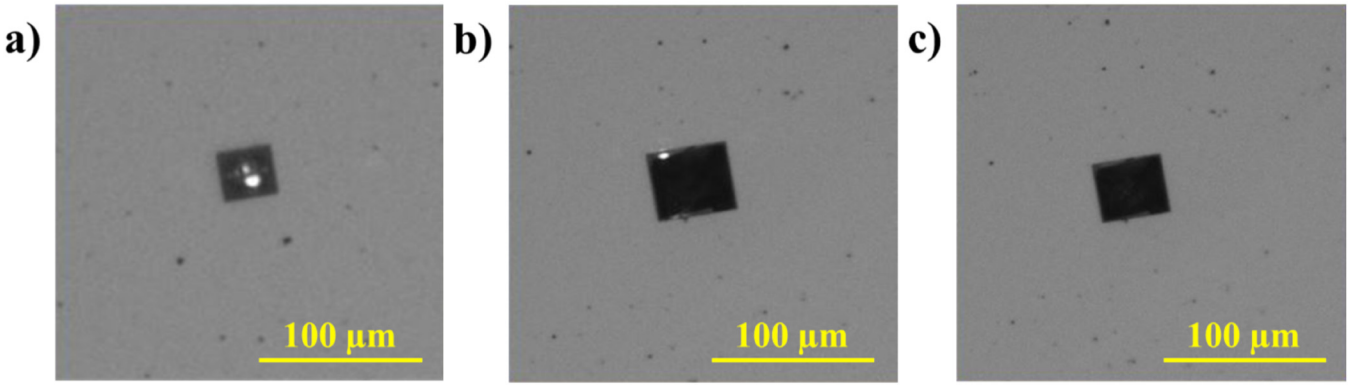


**FIG. 9.** Images captured using the laser Doppler vibrometer. The central black square is the membrane region. (a) Reflection of the laser (see white dot) from the membrane region confirms the presence of an intact membrane. (b) Laser dot reflects from an edge of a partially broken membrane. (c) No laser reflection can be seen in the membrane region when the membrane is completely broken.

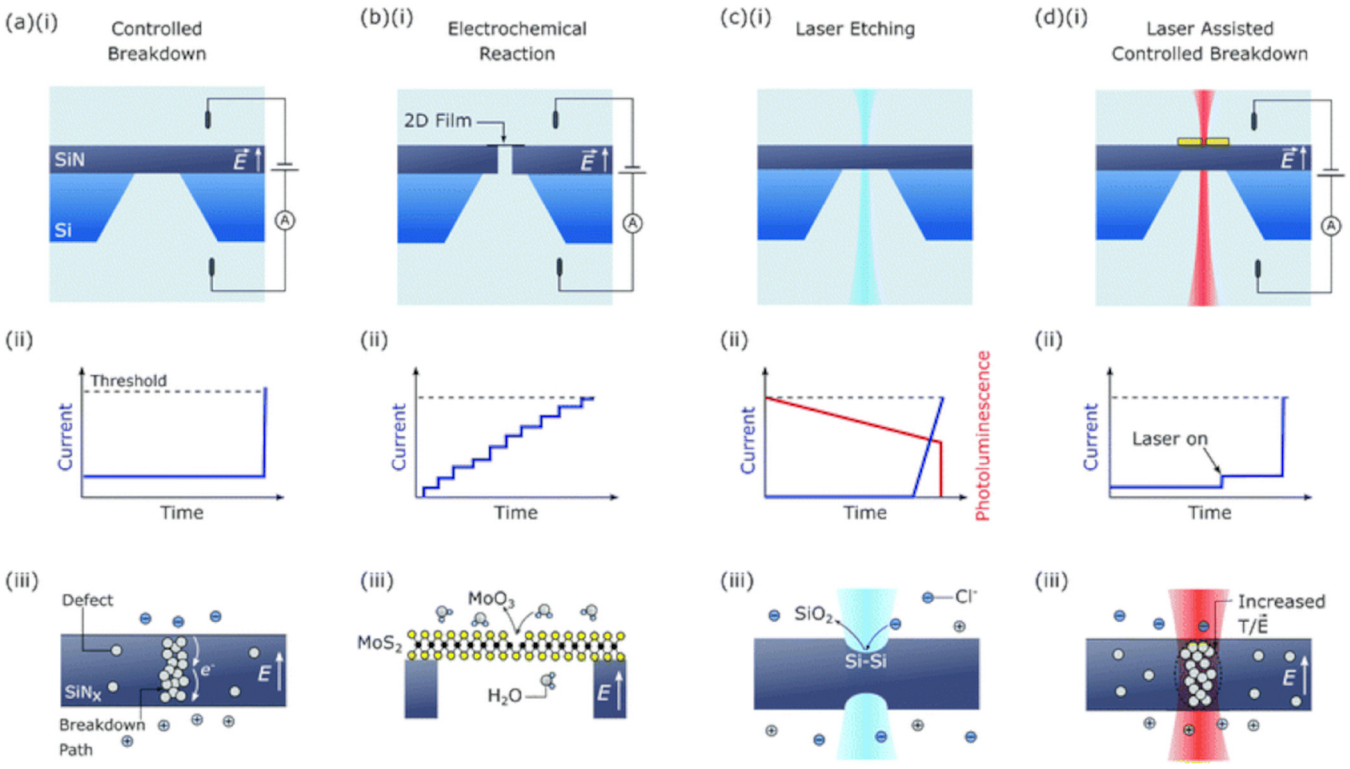


**FIG. 10.** Schematics of the experimental setup (top), measurement trace (middle), and pore formation mechanism (bottom) for the four *in situ* pore fabrication techniques. (a) Controlled breakdown (CBD) whereby nanopores are formed by applying a large electric field (~0.6–1 V $nm^{-1}$) across a dielectric membrane. Such electric fields result in charge trap accumulation that forms a percolation path and results in the physical breakdown in the membrane as a result of Joule heating. (b) ECR where nanopores are formed in suspended two-dimensional films due to electrochemical reactions originating from a defect in the film. (c) Laser etching whereby nanopores are formed as a result of photochemical etching of Si-rich $SiN_x$ membranes in solution. (d) la-CBD whereby a laser is focused on the membrane simultaneous to the application of an electric field to induce breakdown at the focal point of the laser. This can be due to either localized heating, laser etching, or enhanced electromagnetic fields. Note that the threshold current shown in the experimental measurement trace schematics will not be the same magnitude for each technique. Reprinted from Fried *et al.*, Chem. Soc. Rev. **50**(8), 4974–4992 (2021). Copyright (2021) Royal Society of Chemistry under a Creative Commons License.

Translocation signals of six helix bundles (6HB) (using approx. 20 nm pore) and 29 bp DNA (using approx. 5 nm pore) through the fabricated nanopore at an applied voltage of 200 and 600 mV, respectively, are shown in Fig. 7. The 6HB is made by DNA origami technique using M13mp18 (New England Biolabs). Buffer with the concentrations of 1 M KCl, 10 mM Tris-HCl, 1 mM EDTA at pH 7.5 is used for the experiment. Data were collected using Elements SRL nanopore reader at 50 kHz.

## IV. SOLUTIONS FOR PRACTICAL DIFFICULTIES DURING FABRICATION

We have discussed in detail the step-by-step fabrication protocol for membrane suspension and nanopore fabrication (Fig. 2) in Sec. II. Several practical issues arise during different steps of the nanopore fabrication process. These are not usually mentioned in the existing literature. With the view that this work serves as a practical guide, the major challenges encountered and their proposed solutions are listed in this section.

### A. How to ensure that the silicon nitride membrane is suspended successfully?

The first major step toward fabricating nanopores is the successful release of thin silicon nitride membranes (Fig. 8).

The cross-sectional SEM is an excellent tool for the optimization of KOH etching. Once the membrane is suspended, confirmation of the presence of an intact suspended membrane is one of the major issues both during fabrication and transportation. As the color of silicon nitride membrane varies with respect to thickness and becomes more transparent at ultralow thickness, this can be challenging. The membrane can break due to several reasons if we are not careful enough, even during transportation, as shown in Figs. 4(c) and 4(d). If the membrane has a high aspect ratio, the chances of membrane breakage are higher. Along with ionic current measurement, there are several rough and ready ways to check if membranes are intact. Optical microscope [Figs. 5(a) and 5(b)], the differential interference contrast mode of the optical microscope [Fig. 5(d)], and shining laser on the membrane and imaging the same (the laser Doppler vibrometer instruments are equipped with this facility as shown in Fig. 9) can be used to check if membranes are still intact.

### B. How to avoid breakage of thin silicon nitride membrane?

One of the major challenges in successful membrane fabrication is the failure of the membrane due to loss of mechanical integrity in the thin film deposited. Literature as early as the 1960s suggests that the fracture responses of samples from the same material with different thicknesses are different.[14] This causes a crack to require different amounts of energy to stretch and damage along different planes of maximum shear stress. Since fabricating an ideal nanopore device requires releasing membranes as thin as possible, the breakage issue is even more severe. Silicon nitride is brittle, and its strength is directly correlated with the defects in the membrane. The defects can be reduced either by reducing the window area or by applying residual compressive surface stress to counteract the applied pressure, which causes the membrane to break.[15]

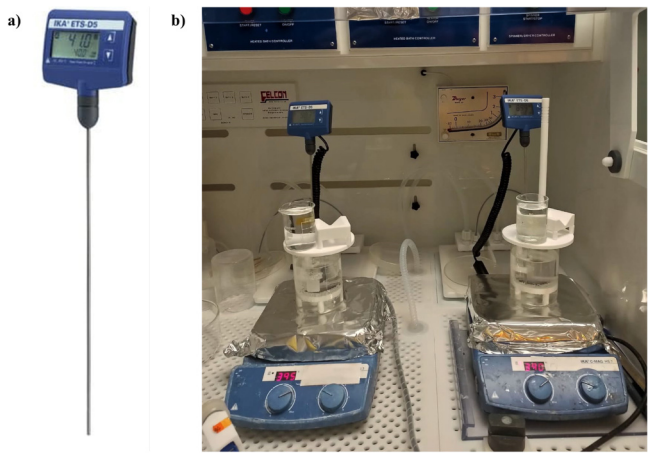


FIG. 11. (a) Automatic temperature controller. (b) Whole KOH etching setup.

Decreasing the silicon nitride membrane residual stress can also contribute to the same. This intrinsic residual stress in silicon nitride films can be altered by changing the silicon component of the films. This is usually done by adjusting the relative concentration of the gases, dichlorosilane, and ammonia, to achieve different ratios of silicon and nitrogen components in the film. Studies indicate that the intrinsic residual stress of Si-rich silicon nitride films is lower than the standard stoichiometric silicon nitride films due to reduced strain in the Si–N bond.[16] Additionally, LPCVD silicon nitride deposition at 700–900 °C is preferred over plasma enhanced chemical vapor deposition silicon nitride, as this film deposited is a denser and more stable thin film with fewer defects.[7]

Moreover, any amount of optimization of process conditions does not entitle us to even minor chip mishandling. Things like gel packs, lint-free cleanroom wipes, and polydimethylsiloxane (PDMS) -lined boxes can be used to carry them around to avoid membrane breakage during transportation. We would recommend against creating a vacuum within the desiccator as the potential pressure difference created could cause membrane failure.

### C. How to ensure no silicon remains at the backside of the membrane?

The thin silicon nitride membrane is transparent when observed through an optical microscope. A brownish color in the optical microscope image is an approximate indication of the presence of silicon remaining most of the time. This is one of the ways we can ensure that no silicon remains on the suspended silicon nitride membrane. Characterization techniques, such as Raman spectroscopy and TEM EDS, can also be used to check if any Silicon remains.

### D. What are the cost-effective alternative methods for TEM-based nanopore fabrications?

The accessibility of the field of nanopore research gets restricted to many researchers, especially in developing and underdeveloped countries, due to the complexity, low throughput, and

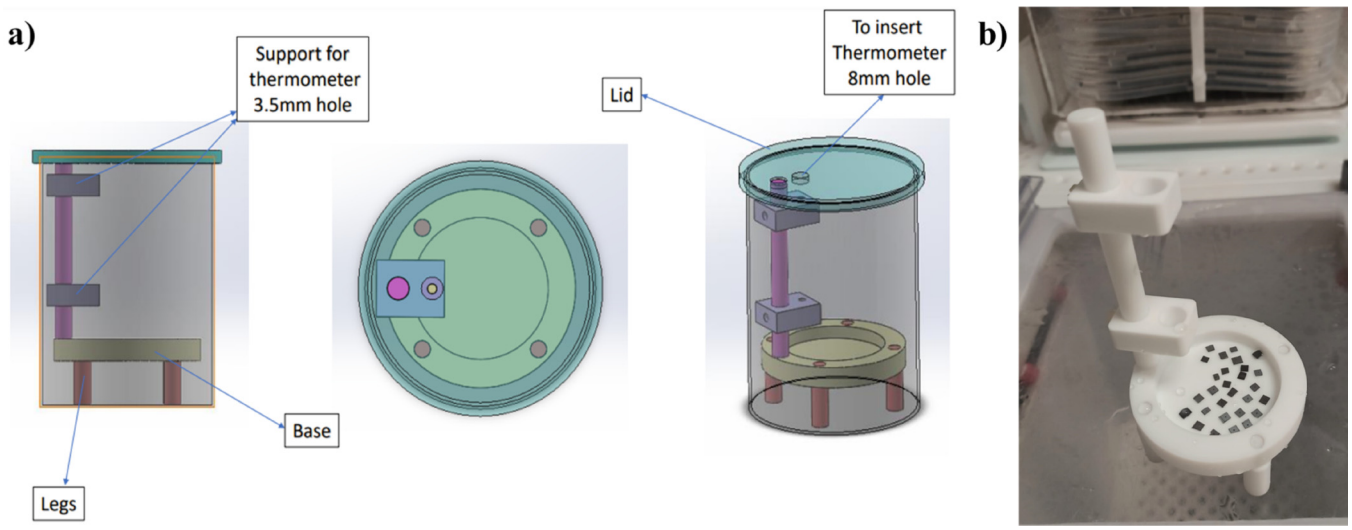


**FIG. 12.** (a) Design of sample holder with provisions to keep thermometer and enough gap for the magnetic rotator. (b) Fabricated Teflon holder with 3 mm chips.

expensive tools and techniques required. This restricts the research opportunities in this field to a relatively small community. TEM and FIB (focused ion beam milling) are not common facilities in labs worldwide, especially in universities and colleges in underdeveloped and developing countries. So, alternative, less complex, and low-cost strategies need to be developed to improve the reach of this research field.

One of the cost-effective alternatives for nanopore fabrication using TEM or FIB is controlled dielectric breakdown (CBD).[12] Figure 10(a) shows the typical dielectric breakdown setup, current measurement during nanopore fabrication, and pore formation mechanism. An electric field applied across the ultrathin membrane causes a small leakage current through the charge traps in the dielectric membrane. Over a period, depending on the thickness of the membrane, a sudden increase in the current is noted due to the formation of a percolation path through the charge traps signifying breakdown and formation of nanopore. At this point, the voltage supply is quickly turned off to prevent any further damage to the membrane. Despite its advantages like reduced cost and complexity, CBD exhibits low yield in forming nanopores of similar features for the same protocol.[17] Each run could present possibilities of forming multiple nanopores, thinned regions, or irregularly shaped nanopores along with the correctly fabricated nanopores.

Like the CBD method, the electrochemical reaction (ECR) method utilizes a similar experimental procedure. The major difference that can be pointed out between the two methods is that CBD is helpful for thicker dielectric materials like silicon nitride, and ESR is helpful for thinner conductive materials, such as $MoS_2$ and



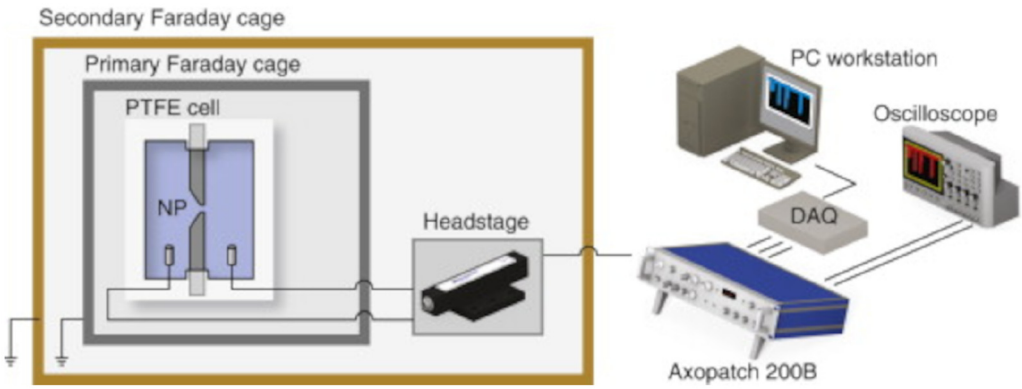


**FIG. 13.** Schematic diagram of typical nanopore sensing setup. Reprinted with permission from V. Tabard-Cossa, *Engineered Nanopores for Bioanalytical Applications* (Elsevier, ■, 2013). Copyright 2013 Elsevier.

**TABLE II.** List of tools required to perform nanopore translocation experiments.

| Instruments/accessories | Commercially available products |
|---|---|
| Amplifier | Axopatch 200B (Ref. 20), AM2400 (Ref. 21), Element SRL (Ref. 22) |
| DAQ | DAQ Card, Axon Digitizer (Ref. 23) |
| Dielectric breakdown setup | Northern Nanopore (Ref. 24) |
| Flow Cell | Teflon flow cell |
| O rings | Seals Shop (Ref. 25) |
| Solid-state nanopore starter kit | Zimmer and Peacock (Ref. 26) |

graphene. The details of the typical setup, current measurement while fabrication of nanopore, and the mechanism of pore formation are shown in Fig. 10(b). The nanopore formation in this method is expected to be due to the electrochemical removal of exposed atoms near the defect in the film.

Other than these, laser etching can also be used for the fabrication of nanopores. This method uses a low-power, highly focused blue-green laser to destabilize Si–Si bonds in Si-rich silicon nitride membranes, causing the eventual formation of nanopores. The nanopore formation can be monitored by applying a small transmembrane potential simultaneously with the laser illumination and keeping tabs on the measured ionic current. The experimental setup here is slightly more complex than the CBD technique but can still replace the traditional methods of TEM or FIB. The details of the typical setup, current measurement, and fabrication of nanopore and the mechanism of pore formation are shown in Fig. 10(c).

Another method built on these existing low-cost methods is laser-assisted controlled breakdown (la-CBD). The breakdown in the membrane can occur owing to photochemical etching at the focal point of the laser, localized heating in the membrane, or the effect on the charge traps in the membrane because of the enhanced electromagnetic field. The details of the typical experimental arrangement, current measurement while fabrication of nanopore, and the mechanism of pore formation are shown in Fig. 10(d).

### E. How to get good control of the KOH etch process?

As mentioned in Sec. II A 5, the etching process to release the silicon nitride membrane requires continuous monitoring over a long time. The process involves etching in two steps, each performed at different temperatures. This requires precise control of the temperatures for each step to avoid unmanageable etch rates of the Si substrate. Our setup uses an automatic temperature controller (IKA ETS D5) with a hot plate (IKA HS MAG 7) to achieve precise control (Fig. 11). This allows us to set the required temperature for the solution with high precision and does not require manual intervention.

### F. How to handle 3 mm-sized samples during etching?

Even though all nanofabrication facilities are equipped with wafer processing carriers, there will not be many options to deal with samples as small as 3 mm. A proper enclosure is also required to prevent KOH liquid evaporation, which otherwise will change the volume ratio. We have custom designed a holder that can be put in a standard 500 ml beaker and the provision to keep the thermometer, as shown in Fig. 12.

### G. How to prevent pore expansion over time?

The expansion of solid-state nanopores over time is a major challenge. The nanopores expand over time in electrolyte solutions, varying from ~0.2 to 3 nm/day. Atomic layer deposition of 1 nm hafnium oxide has been reported to prevent this long-term pore expansion.[18]

### H. What are the typical solid-state nanopore-based tools that can be used for measurement?

Once the nanopore chips have been successfully fabricated, we can move on to testing them for different applications. To do the DNA/protein translocation measurements, it is essential to set up dedicated amplifiers and filters optimized for nanopore measurements. Figure 13 shows a schematic diagram of all the building blocks required to assemble a nanopore setup optimized for low-noise and high-bandwidth current measurements.[19]

The nanopore chip is mounted in a fluidic cell made of Teflon with a tight seal between the two electrolyte reservoirs on either side of the chip. This flow cell is connected to a patch-clamp amplifier with good capacitive feedback to reduce the noise to as low as possible in the current recordings. The signal data can be directly observed on an oscilloscope or be recorded using a PC Workstation. A computer controlled DAQ setup helps digitize analog data signals obtained from the amplifier. We have presented the instruments required to carry out these low-noise nanopore experiments in Table II.

## V. CONCLUSIONS

Nanopore technology is recently gaining research interest due to its futuristic industrial applications and high societal impact. Its existing applications range from healthcare technologies (e.g., DNA sequencing) to DNA computing. Hence, researchers from multiple domains are increasingly working on solid-state nanopores. This work explains the step-by-step protocol to follow and address the common practical challenges and their solutions during the fabrication of silicon nitride nanopore. We have also shown the translocation data of DNA duplex and 6HB structures through these fabricated nanopores, as well as listed the typically used instruments required for nanopore experiments. This work will help anyone new to this field and make the pore fabrication process more accessible.

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## AUTHOR DECLARATIONS

### Conflict of Interest

The authors have no conflicts to disclose.

### Author Contributions

Anumol Dominic and Muhammad Sajeer P contributed equally to this work.

**Anumol Dominic:** Investigation (equal); Methodology (equal); Validation (equal); Writing – original draft (equal); Writing – review & editing (equal). **Muhammad Sajeer P:** Investigation (equal); Methodology (equal); Writing – original draft (equal); Writing – review & editing (equal). **Simran Nasa:** Methodology (supporting). **Manoj Varma:** Funding acquisition (lead); Investigation (equal); Methodology (equal); Resources (lead); Supervision (lead); Writing – review & editing (equal).

## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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