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Single Stage Low Noise Inductor-Less TIA for RF Over Fiber Communication

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ABSTRACT This paper presents design, mathematical analysis, and measurement of low noise single-stage transimpedance amplifier (TIA) with scalable bandwidth using 130 nm bipolar complementary metal-oxide-semiconductor (BiCMOS) silicon-germanium (SiGe) process. Common-emitter (CE) shunt-shunt feedback topology with active inductor peaking has been used in the design for improving noise, gain and driving capability of TIA by decreasing the input and output impedance, respectively. The use of active inductive peaking in CE shunt-shunt feedback topology has resulted in a new TIA configuration with better performance. The circuit has been optimized for low noise by adopting the proposed design technique. Validity of the mathematical analysis and design for the proposed TIA has been established with the help of simulations as well as measurement results. The measurement results of Ku-band TIA (10 MHz to 14 GHz) have demonstrated a transimpedance gain of 53.2 $dB\Omega$, input-referred current noise of 16.8 pA/$\sqrt{Hz}$ with power consumption of 9.8 mW. The design architecture is adaptable for higher frequency bands, which has been demonstrated by designing another TIA covering K- and Ka-bands (10 MHz to 35 GHz) with transimpedance gain of 33.4 dBΩ, input-referred current noise of 29.4 pA/$\sqrt{Hz}$ with power consumption of 28.1 mW in the post-layout simulation results, and occupies same chip area as that of 14 GHz, i.e., $0.1 \times 0.21\ mm^2$

INDEX TERMS BiCMOS, CE topology, inductive peaking, low noise, silicon-photonics, TIA.

I. INTRODUCTION

Silicon-photonics based optical communication has facilitated multiple GHz on-chip data transfer by integrating the complementary metal-oxide-semiconductor (CMOS), bipolar junction transistor (BJT) and photonic circuits on a single substrate. The optical receiver front-end consists of photodetector, followed by transimpedance amplifier (TIA), hence it should offer very low noise and high bandwidth to avoid any degradation in sensitivity. Hence, TIA design is very critical, considering the trade-off between input-referred current noise, gain, bandwidth, and power dissipation [1]–[5]. To realize such a TIA, devices with high transition frequency (f_t) and low noise are necessary.

Traditionally, III-V based semiconductors such as gallium arsenide (GaAs) and indium phosphide (InP) have superior noise and breakdown voltage characteristics and hence been a preferred technology choice for optical receiver [1], [2]. Typically, a 0.13 μm gate length InP high electron mobility transistor (HEMT) has an f_t of about 100 GHz and minimum noise figure of 1 dB at 26 GHz [2]. However, for TIA and other receiver circuit blocks, high breakdown voltage is not required, so BiCMOS/CMOS are preferred for their low cost and integration advantages, even if the noise performance is comparatively inferior. In SiGe-based BiCMOS technology, the BJT device has higher f_t due to higher carrier mobility, good noise performance (due to the much lower flicker noise as compared to MOSFETs), and high integration capability in comparison to CMOS. Typically, a BJT device has an f_t of about 200 GHz and minimum noise figure of 1 dB at 25 GHz for collector current density of 10 $mA/\mu m^2$ [3]. Hence, SiGe HBT-based BiCMOS designs are better candidates for the multiple GHz integrated optical front-end design.

Apart from high-speed data transmission, silicon-photonics [6], [7] is also being explored for on-chip, chip-to-chip or within an RF-over-fiber (RFoF) communication

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system [8]. This is due to the inherent properties of fiber such as low leakage, low interference and better signal confinement at very high frequencies with a small form factor. The architecture of TIA has to be selected based on the application. In the case of RFoF communication, apart from large bandwidth, TIA should also have low noise and high gain at the frequency of operation.

Various architectures have been proposed in the literature for TIA designs [9]–[14]. The high output parasitic capacitance of photodiode to the input node of TIA limits the operating bandwidth of the TIA. This problem can be addressed by using a common gate (CG) amplifier configuration, as this offers low input impedance using transistors with large transconductance (g_m). While, high g_m limits the bandwidth it also generates large noise current across the load resistance due to their large current. Similarly, a regulated cascode (RGC) TIA, used by Taghavi et.al. [13], Costanzo et. al. [15], [16], Hida et. al. [17] and Xie et. al. [18], is a CG TIA with auxiliary gain boosting amplifier to decrease input impedance. Though the designs proposed in [13], [15]–[18] offer better bandwidth, they have relatively low output voltage swing and poor noise performance. In [13], [19], this is due to CMOS with lower f_t. In the case of [20], a 3-stage TIA has been designed using inductors resulting in area overhead. In [21], 0.13 μm BiCMOS based multi-stage TIA has been designed with two TIAs and two variable gain amplifier (VGA) stages. This design is susceptible to stability problem, has larger area and consumes higher power at 32 Gb/s. Similarly, in [22], using 180nm CMOS process, a low noise multi-stage stagger-tuned 8.5 GHz TIA has been designed to overcome the transimpedance limit of single-stage shunt feedback TIA. However, this has led to proportional increase in power consumption and chip area. The broadband characteristics can be obtained by multi-stage design with distributed gain among different stages, however this increases the design complexity, power consumption and chip area [23], [24]. TIA proposed in [24] has demonstrated 3-dB bandwidth of 38.4 GHz, single-ended transimpedance gain of 66 $dB\Omega$, and input-referred noise current density of 14.8 pA/$\sqrt{Hz}$. However, these performance parameters are attained by the use of the multiple stages consisting of a level-shift circuit, post-amplifier, and dynamic feedback (DFB) compensation architecture. Using 130 nm CMOS technology, a common-source TIA with active inductor has been presented in [25] with a bandwidth of 2 GHz and transimpedance gain of 46.1 $dB\Omega$. The actual performance of this TIA may further get affected on fabrication.

In our work, we have designed two TIAs with bandwidths of 14 GHz (Ku-band TIA) and 35 GHz (K- and Ka-band TIA). The Ku-band TIA design has a single-stage with very low input-referred current noise ($<$ 30 pA$\sqrt{Hz}$) and broad bandwidth (10 MHz to 14GHz) with $<$ 30 mW power consumption. We have implemented a novel BJT-based shunt-shunt feedback single stage common emitter (CE) TIA with an active inductor. We have proposed a design procedure to optimize the active inductor and CE BJT configurations for better gain–bandwidth product and noise performance. The use of active inductor peaking helps to increase gain. The biasing of input BJT at optimal collector current density (J_{opt}) corresponding to minimum BJT device noise has led to minimum noise contribution. Performance analysis has been carried out by the measurement results of Ku-band TIA and supported by detailed mathematical analysis. A K- and Ka-band TIA has also been designed for RFoF communication with a broad bandwidth from 10 MHz to 35 GHz to demonstrate the adaptability of this TIA architecture for higher bands. This K- and Ka-band TIA design has proven the robustness of the proposed TIA architecture and its applicability for higher frequency bands. The second TIA has been designed by modifying device parameters without changing the circuit architecture. The post-layout simulation of the K- and Ka-band TIA has demonstrated low noise and high bandwidth, with minimum power, while retaining the same area as that of Ku-band TIA.

II. COMMON EMITTER TIA WITH SHUNT-SHUNT RESISTIVE FEEDBACK

Closed-loop TIAs are preferred over open-loop TIAs as they offers high bandwidth, low noise, and better circuit stability. Among the various feedback topologies, shunt-shunt feedback, i.e., voltage-current feedback topology is commonly used, in which, voltage is sensed at the output and accordingly current is fed back at the input. This technique helps in improving the bandwidth and driving capability of the TIA, which decreases the input and output impedance, respectively [26]–[28]. Another advantage of this type of topology is that the output resistance is independent of feedback resistance and hence eliminates the need for additional buffer circuit, i.e., source/emitter follower to drive the output or subsequent circuit block. Conventionally, BJT offers higher gain and bandwidth compared to MOSFET due to higher g_m and lower device parasitics. Also, at lower frequencies, BJT offers lower flicker noise than MOSFET. At higher frequencies, white noise offered by BJT ($\bar{i}^2{}_n \approx 2qI_c\Delta f$, where q is an elementary charge of an electron, I_c is the collector current in BJT and Δf is the single-sided bandwidth in hertz on which the noise is calculated) is less than that of thermal noise of MOSFET ($\bar{i}^2{}_n \approx 4kT\gamma g_m\Delta f$, where k is the Boltzmann's constant, γ is the body-effect parameter and g_m is the transconductance).

The circuit diagram and approximate small signal model of CE-TIA with shunt-shunt feedback resistor are given in the Fig. 1 (a) and Fig. 1 (b), respectively. In Fig. 1 (b), r_π is BJT's small signal input resistance and $C_{in} = C_{PD} + C_{PAD} + C_{ESD}$, where C_{PD}, C_{PAD} and C_{ESD} are the parasitic capacitances offered by photodetector, input pad and ESD, respectively, R_F is the feedback resistor, R_D is the load resistor and g_{m1} is the transconductance of BJT. As, the BJT input capacitance (C_π) $\ll$ C_{in}, it is not considered in the approximate small signal model.

Consider the detailed analysis of approximate small signal model for BJT based shunt-shunt CE TIA, to calculate

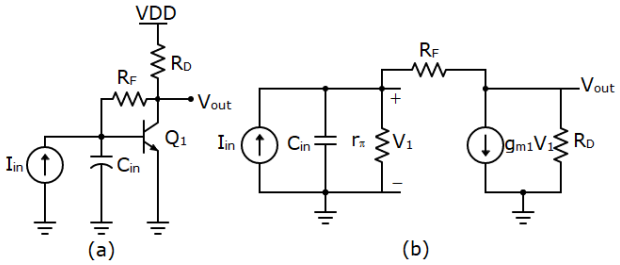

FIGURE 1. (a) Circuit diagram and, (b) approximate small signal model of CE-TIA with shunt-shunt feedback resistor.

transimpedance gain (Z_{BR}), bandwidth (BW_{BR}) and input-referred current noise ($\bar{i}^2_{n,in}$). Applying Kirchhoff's current law in Fig. 1 (b), I_{in} in transfer function domain (s) is given by,

$$I_{in} = V_1(sC_{in} + \frac{1}{r_\pi}) + \frac{V_{out}}{R_D} + g_{m1}V_1 \tag{1}$$

$$V_1 = \frac{I_{in} - \frac{V_{out}}{R_D}}{g_{m1} + sC_{in} + \frac{1}{r_\pi}} \tag{2}$$

Also, V_1 and voltage drop across R_F must add to V_{out}:

$$V_{out} = \frac{I_{in} - \frac{V_{out}}{R_D}}{g_{m1} + sC_{in} + \frac{1}{r_\pi}} + R_F[-\frac{V_{out}}{R_D} - g_{m1}\frac{I_{in} - \frac{V_{out}}{R_D}}{g_{m1} + sC_{in} + \frac{1}{r_\pi}}] \tag{3}$$

$$\frac{V_{out}}{I_{in}} = \frac{(R_D - g_{m1}R_DR_F)r_\pi}{r_\pi + R_D(r_\pi g_{m1} + 1) + R_F + (R_F + R_D)r_\pi sC_{in}} \tag{4}$$

Hence, the transfer function of CE TIA with shunt-shunt feedback and resistive load is given by (5)

$$Z_{BR}(s) \approx \frac{V_{out}}{I_{in}} = \frac{1}{[r_\pi + R_D(r_\pi g_{m1} + 1) + R_F]} \times \frac{(R_D - g_{m1}R_DR_F)r_\pi}{[1 + \frac{(R_F+R_D)r_\pi sC_{in}}{r_\pi + R_D(r_\pi g_{m1}+1)+R_F}]} \tag{5}$$

Comparing the denominator of (5) with the denominator of standard equation for 1^{st} order feedback closed loop circuit, i.e., $(1 + s/\omega_0)$, gives:

$$BW_{BR} \approx f_{-3dB} = \frac{1}{2\pi}[\frac{r_\pi + R_D(r_\pi g_{m1} + 1) + R_F}{(R_F + R_D)r_\pi C_{in}}] \tag{6}$$

Also,

$$\bar{i}^2_{n,in} \approx \frac{2qI_C}{g_m^2R_F^2} + \frac{4KT}{g_m^2R_F^2R_D} + \frac{4KT}{R_F} \tag{7}$$

III. ACTIVE INDUCTOR CONFIGURATION

The bandwidth of TIA can be enhanced by inductive peaking [10], [11], [29], [30] instead of load resistance, as shown in Fig. 2 (a,b). However, the use of passive inductor leads to an increase in the chip area, inferior noise performances due to increased coupling and cross-talk. In our work, the proposed shunt-shunt feedback TIA uses active inductive peaking (AL) for improving the gain without consuming much chip area. A simple active inductor configuration used in this paper has inductive impedance (Z_{AL}) and equivalent inductance (L), as shown in Fig. 2 (b), and given by:

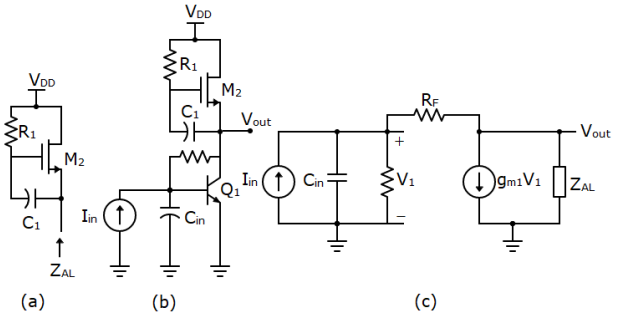

FIGURE 2. (a) Circuit diagram of active-inductor configuration, (b) CE-TIA and, (c) approximate small signal model for CE-TIA with shunt-shunt feedback resistor.

$$Z_{AL} \approx \frac{1 + sR_1C_1}{g_{m2} + sC_1} \qquad L \approx \frac{R_1C_1}{g_{m2} - \frac{1}{R_1}} \tag{8}$$

From the above equations, it is clear that the active inductor will introduce a zero at $w_z = 1/(R_1C_1)$ and pole at $w_p = g_{m2}/C_1$. The circuit will behave as inductor if $g_{m2} > 1/R_1$ for the frequencies between the pole and zero frequency. Apart from the bandwidth extension, the active inductor also helps in fixing the biasing voltage of BJT corresponding to the minimum BJT device noise. The biasing voltage can be fixed by varying the size of MOS (M2), hence the corresponding voltage drop. Though this change in the size of MOS (M2) also leads to change in g_{m2}, it only leads to variation in pole frequency which occurs much before the frequency of operation.

IV. DESIGN PROCEDURE

Fig. 3 shows a typical RF over fiber communication channel. A standalone photonics receiver usually consists of a TIA followed by a level shifter, VGA and 50 Ω output buffer [31].

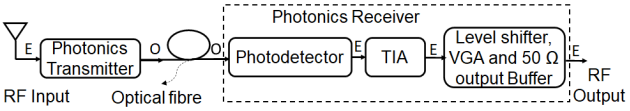

FIGURE 3. Block diagram of photonics transceiver for RF over fiber communication, *O* denotes: optical RF signal, *E* denotes: electrical RF signal.

To design a low noise single-stage TIA, the following design procedure is used:

- *Number of stages required in TIA*: For a given technology node, *gain–bandwidth product = constant* [32], hence, TIA with the required bandwidth is designed, and if the gain obtained in the first stage is not sufficient,

level shifter and variable gain amplifier VGA) are used to get the desired gain.

- *Transistor biasing*: Optimal collector current density (J_{opt}) is found corresponding to the minimum BJT device noise figure for required gain at the frequency of operation. J_{opt} is obtained by fixing the emitter area and sweeping collector current.
- *Fixing the BJT device size*: Corresponding to the J_{opt}, BJT device size is fixed as per output impedance offered by photo-diode and value of feedback resistor.
- *Fixing Active inductor size*: Active inductor is used for extending the bandwidth. The size of MOSFET used in active inductor is fixed corresponding to the J_{opt} and the frequency of operation.

V. PROPOSED TIA: CE TIA WITH ACTIVE INDUCTIVE PEAKING

Considering the advantages of active inductive peaking, we have designed shunt-shunt feedback CE TIA with active inductive peaking. From the approximate small signal model and detailed analysis of this TIA in Fig. 2(c), its transimpedance gain (Z_{BAL}), bandwidth (BW_{BAL}) and input-referred current noise ($\bar{i}^2_{n,inL}$) can be derived.

Rewriting the (4), gives

$$\frac{V_{out}}{I_{in}} = \frac{(1 - g_{m1}R_F)r_\pi R_D}{r_\pi + R_F + R_F r_\pi s C_{in} + R_D(r_\pi g_{m1} + r_\pi s C_{in} + 1)} \tag{9}$$

To get the transfer function of CE TIA with shunt-shunt feedback and active inductive load using small signal model in Fig. 2 (c), replacing R_D in (9) with Z_{AL} and its equivalent expression from (8) gives:

$$\frac{V_{out}}{I_{in}} = \frac{(1 - g_{m1}R_F)(1 + sR_1C_1)r_\pi}{\left[(r_\pi + R_F + R_F r_\pi s C_{in})(g_{m2} + sC_1) + (1 + sR_1C_1)(r_\pi g_{m1} + r_\pi s C_{in} + 1)\right]} \tag{10}$$

Rearranging the (10) gives:

$$\frac{V_{out}}{I_{in}} = \frac{(1 - g_{m1}R_F)(1 + sR_1C_1)r_\pi}{\left[1 + r_\pi(g_{m1} + g_{m2}) + R_F g_{m2} + s(R_F g_{m2} r_\pi C_{in} + R_F C_1 + r_\pi C_{in} + r_\pi C_1 + R_1 C_1 r_\pi g_{m1} + R_1 C_1) + s^2(R_F r_\pi C_{in} C_1 + R_1 C_1 r_\pi C_{in})\right]} \tag{11}$$

Further, rearranging the (11) in the form of standard equation for 2^{nd} order feedback closed loop circuit gives:

$$Z_{BAL}(s) \approx \frac{V_{out}}{I_{in}} = \frac{(1 - g_{m1}R_F)(1 + sR_1C_1)r_\pi}{(R_F r_\pi C_{in} C_1 + R_1 C_1 r_\pi C_{in})\left(\frac{1 + r_\pi(g_{m1} + g_{m2}) + R_F g_{m2}}{R_F r_\pi C_{in} C_1 + R_1 C_1 r_\pi C_{in}} + s\frac{(R_F g_{m2} r_\pi C_{in} + R_F C_1 + r_\pi C_{in} + r_\pi C_1 + R_1 C_1 r_\pi g_{m1} + R_1 C_1)}{(R_F r_\pi C_{in} C_1 + R_1 C_1 r_\pi C_{in})} + s^2\right)} \tag{12}$$

Comparing the denominator of (12) with the denominator of standard equation for 2^{nd} order feedback closed loop circuit with damping factor ζ, i.e., $s^2 + 2\zeta\omega_0 s + \omega_0^2$, gives:

$$\omega_0^2 = \frac{1 + r_\pi(g_{m1} + g_{m2}) + R_F g_{m2}}{r_\pi C_{in} C_1 (R_F + R_1)} \tag{13}$$

Hence,

$$BW_{BAL} \approx f_{-3dB} = \frac{1}{2\pi}\sqrt{\frac{1 + r_\pi(g_{m1} + g_{m2}) + R_F g_{m2}}{r_\pi C_{in} C_1 (R_F + R_1)}} \tag{14}$$

Similarly,

$$\bar{i}^2_{n,inL} \approx \frac{2qI_C}{g_{m1}^2 R_F^2} + \frac{4KT}{R_F} + \bar{i}^2_{Z_{AL}n,inL} \tag{15}$$

where $\bar{i}^2_{Z_{AL}n,inL}$ is the input-referred current noise of the active inductor.

From (5), (8), (12), $|Z_{AL}| > R_D$ (i.e., $R_D < 1/g_{m2}$) and approximation similar to shunt-shunt CS-TIA in [26], implies $|Z_{BAL}| > |Z_{BR}|$. Similarly, comparing (6) and (14) gives $BW_{BAL} > BW_{BR}$. Also, input-referred current noise introduced by R_D is always higher than that of Z_{AL}, since $(1/R_D) > g_{m2}$. Therefore, comparing (7) and (15) gives $\bar{i}^2_{n,inL} < \bar{i}^2_{n,in}$. Hence, the proposed shunt-shunt CE-TIA with active inductive feedback has better transimpedance gain, bandwidth and noise performance in comparison to shunt-shunt CE-TIA with resistive feedback.

A. DESIGN AND SIMULATION OF Ku-BAND TIA

Ku-band TIA (10 MHz to 14 GHz), has been designed using the proposed CE TIA with active inductive peaking. Design has been done as per the design procedure discussed in section IV. Specifications of the design have been achieved by following the mathematical analysis given in section V and using the following equations: (8) for active inductor pole position, (12) for transimpedance gain, (14) for bandwidth and (15) for input-referred noise calculations. Further, the values of component parameters were optimized iteratively based on the post-layout electromagnetic (EM) simulation results. Accordingly, the summary of final values for the devices used in the Ku-band TIA design is given in Table 1. Performance of the Ku-band TIA at the layout level has been benchmarked with the help of post layout EM simulation results, and are elaborated in section VI.

B. DESIGN AND SIMULATION OF K- AND Ka-BAND TIA

The proposed TIA architecture is adaptable to higher frequency bands. The robustness of the design for higher frequency bands has been demonstrated by designing one more TIA covering frequencies in K- and Ka-band (10 MHz to 35 GHz). The design procedure discussed in Section IV is also used for K- and Ka-band TIA design. The summary of optimized device parameters for K- and Ka-band TIA is given in Table 1. Performance of the TIA has been characterized by post-layout EM simulation results.

TABLE 1. Summary of final values for the devices used in the designs of Ku-band TIA and K- and Ka-band TIA.

Circuit component	Ku-band TIA	K- and Ka-band TIA
Feedback resistor (R_F)	288 Ω	39 Ω
Size of NMOS used in active inductor	80 μm/0.2 μm	32 μm/0.2 μm
Current density of input BJT	5.8 $mA/\mu m^2$	6.24 $mA/\mu m^2$

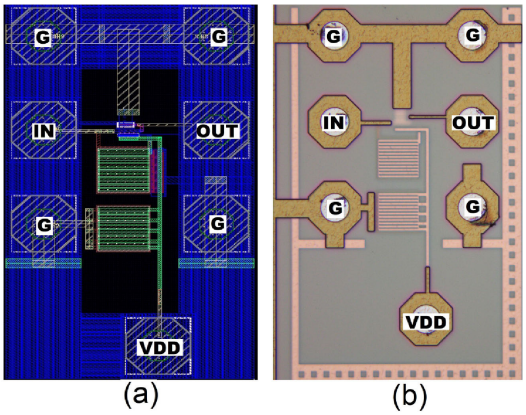

FIGURE 4. (a) Chip micrograph of Ku-band TIA (b) Layout image of the proposed K- and Ka-band TIA, both with active area of 0.10 × 0.21 mm^2.

The layout and post-layout simulations the proposed TIA have been carried out using standard EM guidelines. Fig. 4(a) shows a compact chip layout with 0.35 × 0.6 mm^2 area as per RF probe measurement requirements. The layout area of TIA without the input and output probe pads is only 0.10 × 0.21 mm^2.

Fig. 5 and Fig. 6 show the variation of post-layout simulated input/output return-loss (S_{11}/S_{22}) and power gain (S_{21}) with frequency. The post-layout simulated S-parameters have show an input/output return loss better than 8.5 dB across the bandwidth and S_{21} of approximately −2.5 dB to −3 dB in the active inductive peaking spectrum (10 MHz to 35 GHz). Fig. 7 shows the post-layout simulated transimpedance-gain from DC to 90 GHz, and also shows the impact of active inductive peaking on the transimpedance-gain beyond 1 MHz. As per (16), gain peaking in the transimpedance-gain plot is a result of gain-peaking in S_{21}, since $S_{11} \ll 1$. Fig. 8 and Fig. 9 show the variation of post-layout simulated transimpedance-gain and input-referred current noise with frequency, respectively. It is observed that a transimpedance gain of 33.4 dBΩ and input-referred current noise of 29.4 pA/$\sqrt{Hz}$ are achieved. The degradation in gain and noise performance of K- and Ka-band TIA in comparison to Ku-band TIA is due to increase in device parasitics effect and BJT device noise with increase in frequency.

VI. MEASUREMENT RESULTS OF Ku-BAND TIA

TIA and photodiode are generally designed in two different technologies due to performance limitation of the silicon

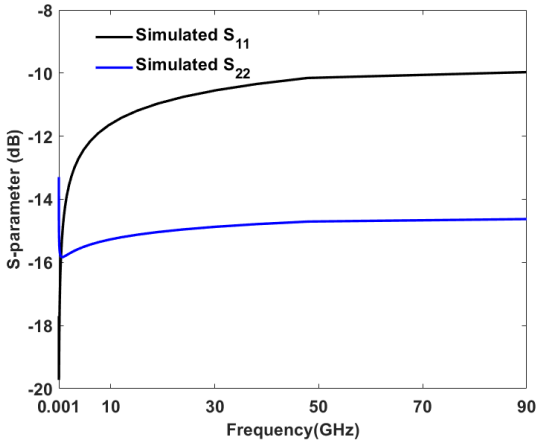

FIGURE 5. Variation of post-layout simulated input/output return losses with frequency for K- and Ka-band TIA from 1 MHz to 90 GHz on linear frequency scale.

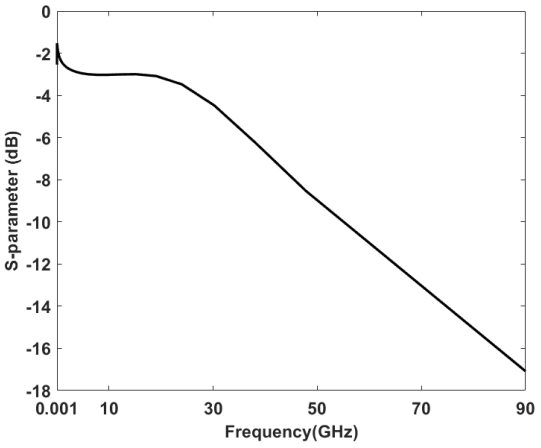

FIGURE 6. Variation of post-layout simulated S_{21} with frequency for K- and Ka-band TIA from 1 MHz to 90 GHz on the linear frequency scale.

substrate for photodiode diode realization, and are integrated at package level [24]. In case, if they are not integrated in the same technology platform, then the input/output are matched to 50 Ω impedance. The same approach has been adopted here, as well as in literature [16], [17]. At the measurement level, as per the available literature, it is not possible to measure transimpedance gain (Z_t) directly and is always calculated from the S-parameters [16], [17].

$$Z_t = Z_0 \times \left[\frac{S_{21}}{1 - S_{11}}\right] \tag{16}$$

For noise measurement, the output noise power of the TIA is measured without applying signal at the input. To calculate the current noise at the input, the measured output noise power of the TIA is referred back at its input by using measured transimpedance gain [16].

The designs have been targeted only for transmission and reception of analog RF signal, hence the simulation, measurement and characterization have been carried out accordingly only for relevant parameters and not for other parameters

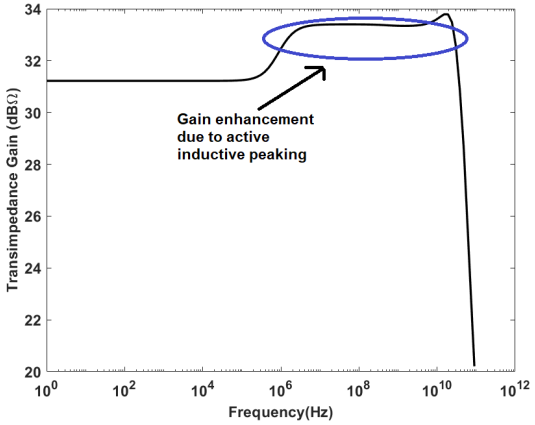

FIGURE 7. Variation of post-layout simulated transimpedance-gain with frequency for K- and Ka-band TIA from DC to 90 GHz on the logarithmic frequency scale.

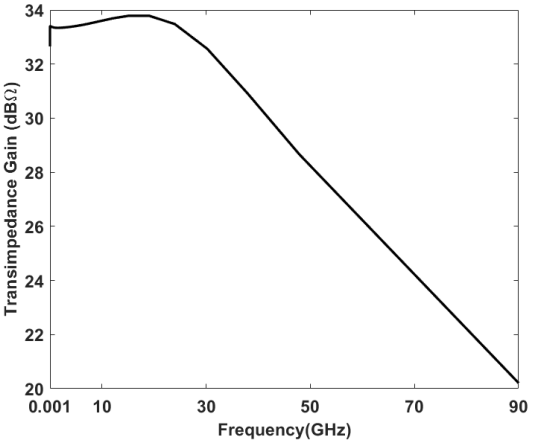

FIGURE 8. Variation of post-layout simulated transimpedance-gain with frequency for K- and Ka-band TIA from 1 MHz to 90 GHz on the linear frequency scale.

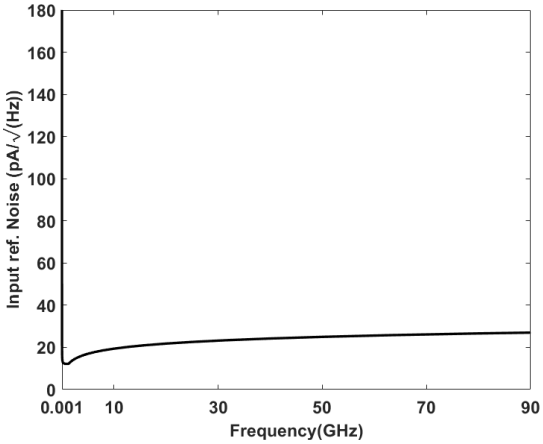

FIGURE 9. Variation of post-layout simulated input-referred current noise with frequency for K- and Ka-band TIA from 1 MHz to 90 GHz on the linear frequency scale.

such as eye-diagram etc. which are relevant for data communication applications where input/output are digital signals.

Ku-band TIA has been designed and fabricated using SiGe 130 nm HBT BiCMOS technology [5] with f_t/f_{max} of the order of 250/340 GHz. Layout has been carried out by using the top-metal layers for minimum resistivity contribution. To minimize the effect of parasitics, pads with minimum available size and distance between ground-signal-ground (GSG) pads have been chosen. 3D EM simulation has been done using Keysight ADS to benchmark the performance of the circuit at layout level. The core chip area is only $0.1 \times 0.21\ mm^2$ due to the absence of any bulky inductor. The performance of the Ku-band TIA has been validated using post-layout simulations as well as measured results. Fig. 4(b) shows the fabricated chip micrograph of Ku-band TIA.

The measurements of the fabricated Ku-band TIA has been carried out using 50 Ω GSG probes with Cascade probe station, Keysight PNA-X and spectrum analyser. The measured and simulated input/output return-losses (S_{11}/S_{22}) and power gain (S_{21}) of the Ku-band TIA up to 40 GHz frequency are shown in Fig. 10 and Fig. 11, respectively. The variations of measured and simulated S-parameters for Ku-band TIA have shown similar trends. This TIA has demonstrated an input/output return loss better than 9 dB over the entire bandwidth (i.e., till 14 GHz) and approximately a flat S_{21} of 18 dB in the active inductive peaking spectrum (i.e., in the target broadband frequency range from 10 MHz to 14 GHz).

Fig. 12 shows the plot of measured and simulated transimpedance-gain with frequency from DC to 40 GHz on the logarithmic frequency scale, which demonstrated the impact of active inductive peaking on transimpedance-gain beyond 500 kHz frequency. As per the (16), this gain peaking in the transimpedance-gain plot resulted from gain-peaking in S_{21}, since $S_{11} \ll 1$. The measured and simulated transimpedance-gain, and input-referred current noise with frequency for Ku-band TIA are shown in Fig. 13 and Fig. 14, respectively. The measured results of transimpedance-gain, and input-referred current noise with frequency are in good agreement with the simulation results. Measurement results have demonstrated a gain of 53.2 dBΩ, and input-referred current noise of 16.8 pA/$\sqrt{Hz}$. Use of active inductive peaking leads to a decrease in the input impedance and hence a higher value feedback resistor is required. Thus, active inductive peaking in CE- shunt-shunt feedback TIA helps in increasing the gain. It offers superior noise performance since it uses CE configuration, and moreover, the BJT has negligible flicker noise and low thermal noise compared to MOS device.

A. COMPARATIVE ANALYSIS

Table 2 presents a comparison of our TIA design with other existing TIAs in literature. From Table 2, it is clear that although the proposed TIA is a single single-stage TIA, its performance is better than other multiple-stage TIAs [4], [15] in terms of bandwidth/data-rate, noise, gain, power consumption and area efficiency. This design is adaptable for higher frequency bands, without increase in area and power with competitive gain and noise performance [21], [23] at

TABLE 2. Comparison of the proposed TIAs and reference TIAs in literature.

Reference	[4]	[15]	[21]	[23]	**This work Ku-band TIA**	**This work K & Ka-band TIA**
$3-dB$ Bandwidth (GHz)	7	11	33	35	**14**	**35**
Technology	130nm CMOS	65nm CMOS	130nm BiCMOS	130nm BiCMOS	130nm BiCMOS	130nm BiCMOS
Transimpedance gain ($dB\Omega$)	53	62	74	41	**53.2**	33.4
Input-referred noise ($pA/sqrt(Hz)$)	27	30	12.2	39.8	**16.8**	**29.4**
Input capacitor (fF)	1000	200	NA	100	230	230
Number of TIA stages	2	3	2+2VGA	3	**1**	**1**
Inductor used	No	Yes	No	Yes	No	No
Power consumption (mW)	108	66	218	24	**9.8**	28.1
Area (mm^2)	$0.024^{\dagger}$	0.08^{γ}	2^{ζ}	0.04^{ν}	**0.021**	**0.021**

†Active area of TIA and 1st stage of limiting amplifier without pads.
γActive area without pads.
ζTotal active area without pads.
νTotal active area without pads.

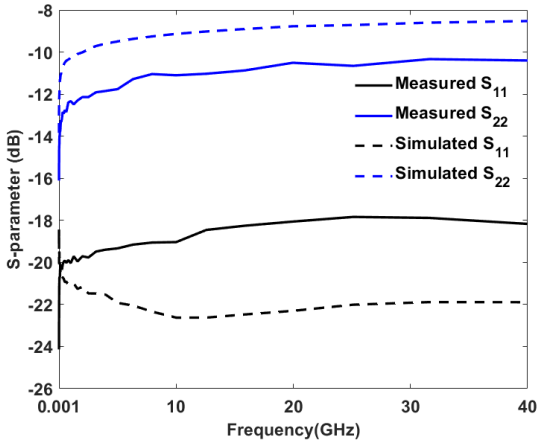

FIGURE 10. Variation of measured and simulated input/output return losses with frequency for Ku-band TIA from 1 MHz to 40 GHz on the linear frequency scale.

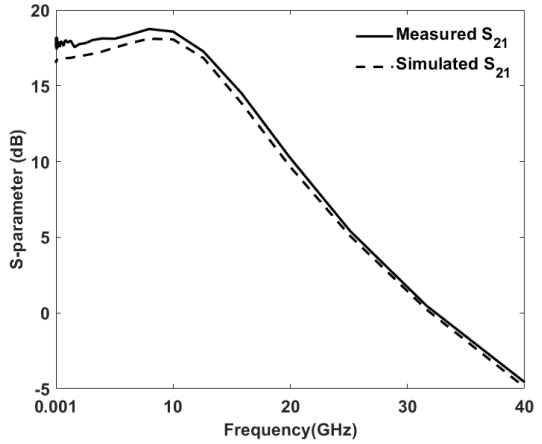

FIGURE 11. Variation of measured and simulated S_{21} with frequency for Ku-band TIA from 1 MHz to 40 GHz on the linear frequency scale.

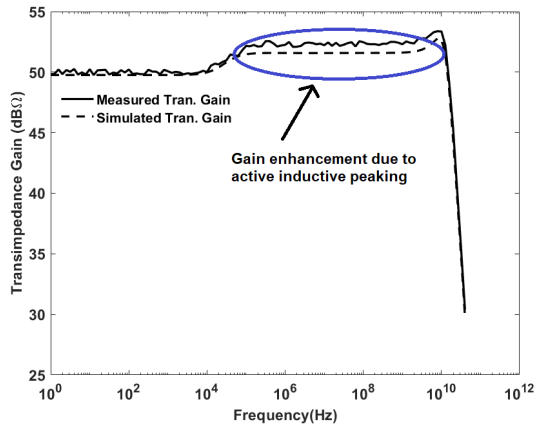

FIGURE 12. Variation of measured and simulated transimpedance-gain with frequency for Ku-band TIA from DC to 40 GHz on the logarithmic frequency scale.

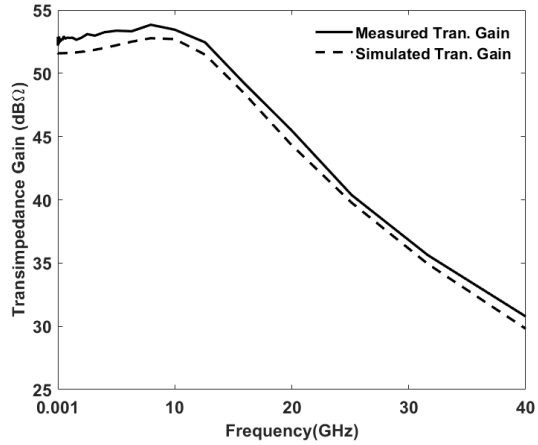

FIGURE 13. Variation of measured and simulated transimpedance-gain with frequency for Ku-band TIA from 1 MHz to 40 GHz on the linear frequency scale.

higher bandwidths. Although higher gain and bandwidth/ data-rate can be achieved by the use of multiple stage TIA, such topologies consume more area, power, and are prone to stability problems due to increased design complexity and may have inferior noise performance. To the best of our knowledge, the detailed mathematical analysis of shunt-shunt feedback TIA with resistive feedback and active inductive peaking presented in this paper have not been reported so far,

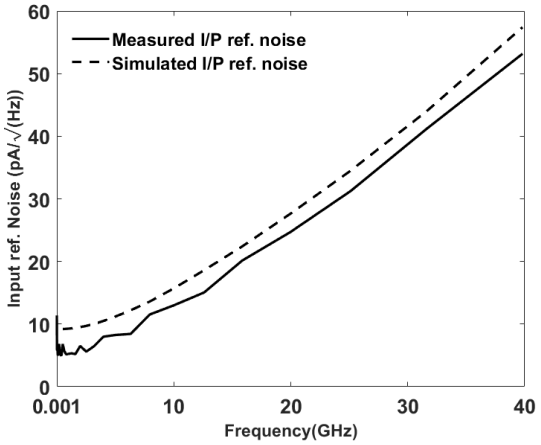

FIGURE 14. Variation of measured and simulated input-referred current noise with frequency for Ku-band TIA from 1 MHz to 40 GHz on the linear frequency scale.

and the measured performance of this TIA is better among various single stage TIAs available in the literature. This analysis has been validated with simulation and measurement results.

VII. CONCLUSION

In this work, we have designed and fabricated a single-stage shunt-shunt feedback common-emitter TIA with active inductive peaking using 130 nm SiGe BiCMOS. For the enhancement of TIA gain, we have introduced active inductive peaking in CE TIA, which has resulted in 3 dB increase in TIA bandwidth. To demonstrate the adaptability of the proposed TIA for higher frequency bands, two TIAs were designed using the same circuit by changing the device parameters. Performance of proposed TIA architecture is supported by detailed mathematical analysis and has been validated by characterizing the fabricated chip. Measured results of this Ku-band single-stage TIA (10 MHz to 14 GHz) have demonstrated transimpedance gain of 53.2 $dB\Omega$ and input-referred current noise of 16.8 pA/$\sqrt{Hz}$ with a power consumption of 9.8 mW. Post-layout simulation results of the K- and Ka-band TIA (10 MHz to 35 GHz) have demonstrated transimpedance gain of 33.4 $dB\Omega$ and input-referred current noise of 29.4 pA/$\sqrt{Hz}$ with a power consumption of 28.1 mW. As per the measurement and simulation results, for a particular bandwidth, this single stage TIA has demonstrated superior performance in comparison to other TIAs available in the literature, either in terms of one or more performance parameters, i.e., transimpedance gain, input-referred current noise, power consumption or chip area.

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