A Multilevel 30-sided Space Vector Structure Generation for an Induction Motor Drive Using a Single DC-link

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***Abstract*—This paper proposes the generation of a multilevel 30-sided space vector structure (SVS) from a single DC-link for an open-end induction motor (OEIM) drive. This scheme exhibits the inherent advantages of multilevel inverters like usage of low voltage blocking switches, less dv/dt in phase voltage etc. As the SVS generated is a 30-sided, lower order harmonics till 25th order is eliminated from the motor phase voltage. Linear modulation range is also extended till 99.63% of the base speed as the SVS is closer to a circle. The topology consists of a DC-link fed hybrid 5-level inverter feeding one end of the OEIM and a capacitor fed hybrid 5-level inverter feeding from the other end of the OEIM. Active DC-link fed inverter acts as the only source of active power while the inverter feeding from the other end acts as a switched harmonic filter. Simulation studies and experimental verification of the proposed scheme are performed and presented in this paper.**

I. Introduction

Induction motors (IM) are preferred in industry due to their simple construction and lesser maintenance cost. To perform speed control of an IM, drive schemes which can generate variable frequency and variable voltage are used. The simplest realization of an IM drive is a conventional 2-level inverter. Conventional 2-level inverters have drawbacks of high dv/dt across the motor phase voltage, high voltage stress across the switches etc. To overcome these disadvantages multilevel inverters (MLIs) have been proposed in the literature. MLI offers usage of less voltage blocking switches, lesser dv/dt in motor phase voltage etc.

Popular MLIs are Flying Capacitor (FC) inverter, Neutral Point Clamped (NPC) inverter and Cascaded H-bridge (CHB) inverter [1]. As the number of output levels increases, the required number of power switches, capacitors and active DC sources (in case of CHB) increases. To overcome this issue, hybrid topologies have come into practice [2], [3]. A topology to generate a 5-level hexagonal SVS with a DC-link fed FC inverter cascaded with a capacitor fed CHB is explained in [4]. This topology uses a single DC-link to generate 5-levels with less number of switches.

All the above mentioned IM drive schemes produce a hexagonal voltage SVS. The linear modulation range of a hexagonal voltage SVS is 0.577 times DC-link voltage, which corresponds to 90.6% of base speed. To operate the machine above linear modulation region, significant lower order harmonics (5th, 7th etc) are introduced in the machine phase voltage, leading to undesirable 6th harmonic torque ripple in the motor shaft.

To eliminate these lower order harmonics, passive LC filters [5] and selective harmonic elimination (SHE) technique [6], [7] are employed. Usage of passive LC filter makes the system bulky and will make the drive response slow during dynamics. SHE works on the principle of introducing notches in applied voltage to eliminate the required harmonics. Elimination of more number of lower order harmonics results in computational intensive algorithms. Moreover, introduction of notches reduces the maximum fundamental voltage that can be extracted from a particular DC-link.

In this scenario, polygonal voltage SVSs are a preferred choice to eliminate lower order harmonics in machine phase voltage and to increase the linear modulation range. In [8] research has been done on dodecagonal SVS which eliminates 5th and 7th order harmonics from the motor phase voltage. These schemes use multiple DC-links which makes the scheme difficult to perform four quadrant operation. In [9], [10] studies were performed on generation of dodecagonal and 24-sided SVS using a single DC link. In [11], a 30-sided polygonal SVS was proposed which eliminates all the lower order harmonic voltage till 25th order from the motor phase voltage.

This paper proposes the generation of a multilevel 30-sided SVS using a single DC-link for OEIM. In this scheme, all the lower order harmonics like 5th, 7th, 11th, 13th, 17th, 19th, 23rd and 25th order are eliminated from motor phase voltage. Multilevel SVS reduces the voltage error w.r.t the actual reference to be synthesized in the motor phase voltage. The topology consists of a DC-link fed Inverter1 connected to one end of the OEIM and a capacitor fed Inverter2 feeding from the other end. Here, Inverter1 sources all the active power for the scheme and Inverter2 acts as a harmonic filter.

The paper is arranged in the following manner: Section II discuses about the inverter configuration, followed by details

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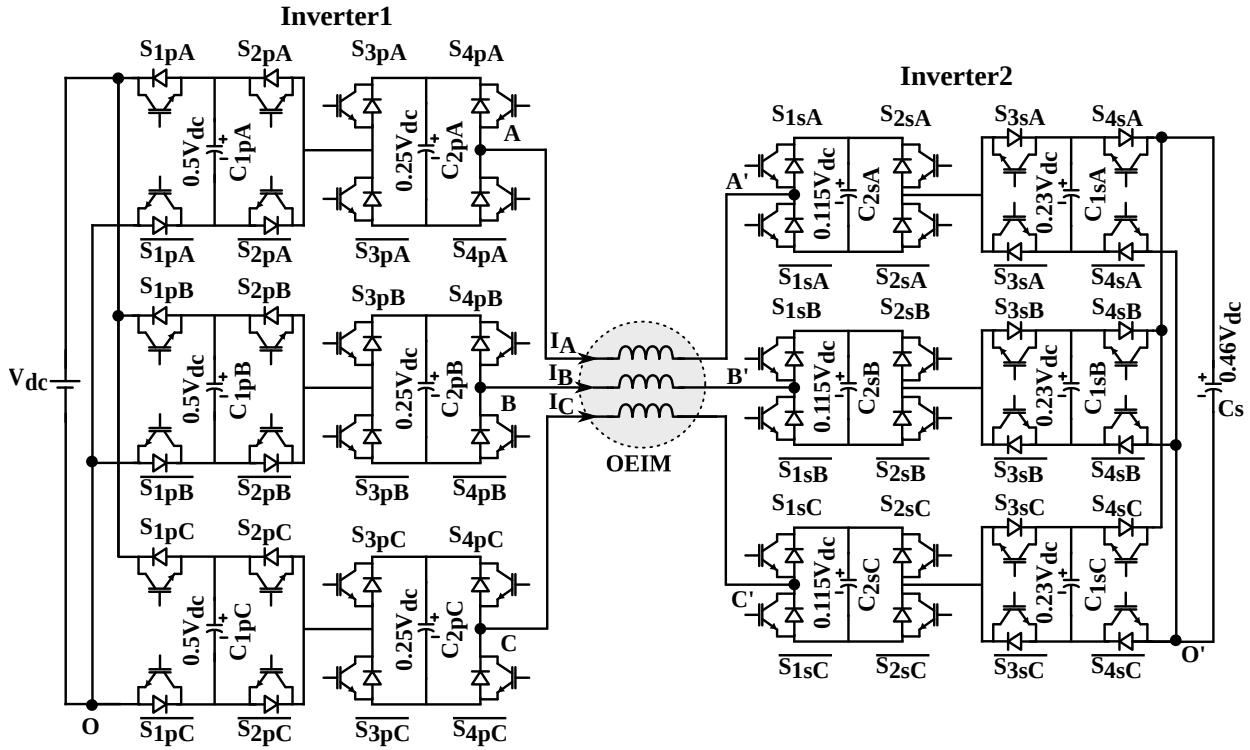

Figure 1. Power circuit of the proposed scheme

of SVS and generation of a space vector location in section III. Capacitor balancing of the floating capacitors and implementation of the proposed scheme is explained in Section IV and section V respectively. Simulation studies and experimental results are shown in section VI and the paper is concluded in section VII.

II. Inverter Configuration

The power circuit configuration (Figure.1) consists of two 5-level inverters namely Inverter1 and Inverter2, feeding from either end of an OEIM.

Inverter1 (Figure.1) is a hybrid topology, cascading an active DC-link fed FC inverter with a CHB inverter. The ratio of DC-link voltage: Inverter1-FC capacitor voltage: Inverter1-CHB capacitor voltage is maintained at 4:2:1. The pole voltages obtained from Inverter1 are, V_{XO} = 0, $0.25V_{dc}$, $0.5V_{dc}$, $0.75V_{dc}$ and V_{dc} (X= A,B,C phase). Here FC inverter switches are rated for a voltage of $0.5V_{dc}$ and CHB inverter switches are rated for a voltage of $0.25V_{dc}$.

Inverter2 (Figure.1) also has the same construction as that of Inverter1, i.e cascade of an FC inverter with a CHB inverter. Here the DC-link of FC inverter is a capacitor (referred as common capacitor throughout this paper), which is maintained at its nominal value by the PWM strategy explained in section IV. For generation of the 30-sided SVS, the Inverter2 common capacitor (C_s) voltage is maintained at $0.46V_{dc}$. The ratio of Inverter2-common capacitor voltage: Inverter2-FC capacitor voltage: Inverter2-CHB capacitor voltage is maintained at 4:2:1. The pole voltages obtained from Inverter2 are, $V_{X'O'}$ = 0, $0.115V_{dc}$, $0.23V_{dc}$, $0.345V_{dc}$ and $0.46V_{dc}$, (X= A,B,C phase). Here FC inverter switches are rated to block a voltage of $0.23V_{dc}$ and CHB inverter switches are rated for $0.115V_{dc}$.

III. Space Vector Structure

A. Generation of multilevel 30-sided SVS

A single layer 30-sided SVS generation using a single DC-link is explained in [11]. In [11], a 30-sided vector of radius $0.957V_{dc}$ is generated from the vector sum of a space vector from the primary inverter and a switch-averaged vector from the 5-level secondary inverter. Primary inverter generates a 2-level hexagonal SVS of radius V_{dc} and secondary inverter generates a 5-level SVS of radius $0.46V_{dc}$.

In the proposed work, Inverter1 produces a 5-level hexagonal SVS of radius V_{dc}, which can be visualized as a combination of four independent hexagons of radii $0.25V_{dc}$. These independent $0.25V_{dc}$ radii hexagons combine with the switched average vector from the Inverter2 resulting in generation of a 5-level 30-sided SVS of radius $0.957V_{dc}$ (Figure. 2). The resultant 30-sided is split into 480 congruent triangles and any reference vector lying within any of these triangles is realized by switch averaging the 30-sided vectors forming the vertices of the triangle. For example in Figure.2, reference vector V_R, is realized by time averaging the vectors OA, OB and OC with appropriate timings. The generation of vector 30-sided vector OA from Inverter1 space vector and Inverter2 space vector are explained in Section III-B. Since the resultant SVS is a 30-sided polygon, linear modulation is extended till 99.63% of base speed as compared to 90.6% for a hexagonal SVS. Even during over modulation, all the

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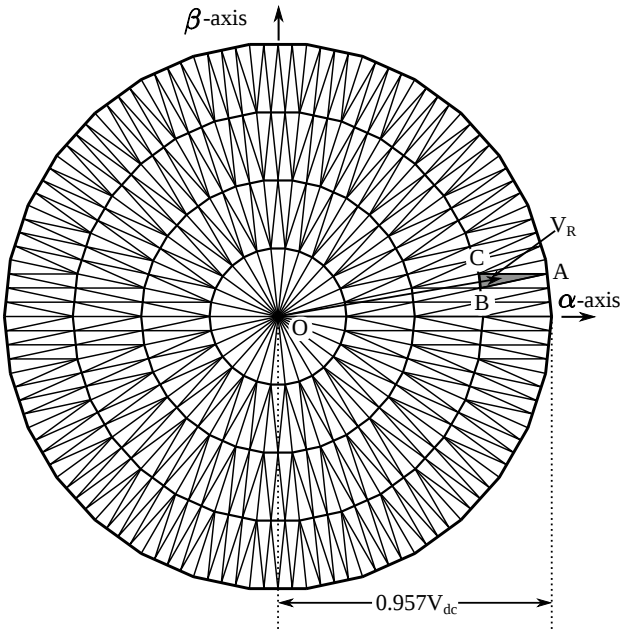

Figure 2. Resultant multilevel 30-sided SVS

harmonics till 25th order are eliminated from the motor phase voltage.

B. Generation of 30-sided space vector OA (Figure. 2)

To generate the 30-sided space vector OA ($0.953V_{dc}\angle 9°$) (Figure. 3), Inverter1 vector OH_1 ($V_{dc}\angle 0°$) is superimposed with Inverter2 vector H_1A, as given in (1).

$$\begin{aligned} &OA = OH_1 + H_1A \\ \Rightarrow &H_1A = 0.953V_{dc}\angle 9° - V_{dc}\angle 0° \\ \Rightarrow &H_1A = 0.16V_{dc}\angle 111.58° \end{aligned} \tag{1}$$

The vector from Inverter2 (H_1A) does not overlap with any space vector location of the 5-level SVS generated by Inverter2. So the vector H_1A is generated by switch averaging the nearest hexagonal vectors. Here, vectors H_1P ($0.23V_{dc}\angle 120°$), H_1Q ($0.20V_{dc}\angle 90°$) and H_1R ($0.115V_{dc}\angle 120°$) are switch averaged in ratios of k_0: k_1: 1-(k_0+k_1) respectively to generate H_1A (2).

$$\begin{aligned} &H_1A = H_1P\ k_0 + H_1Q\ k_1 + H_1R\ *(1-(k_0+k_1)) \\ \Rightarrow &0.16V_{dc}\angle 111.58° = 0.23V_{dc}\angle 120°\ k_0 + 0.20V_{dc}\angle 90°\ k_1 \\ &\qquad + 0.115V_{dc}\angle 120°\ *(1-(k_0+k_1)) \\ \Rightarrow &\qquad k_0 = 0.264, \\ &\qquad k_1 = 0.236, \\ &\qquad 1-(k_0+k_1) = 0.5 \end{aligned} \tag{2}$$

During application of 30-sided space vector OA, if the time ratio obtained in (2) is not maintained, the Inverter2 common capacitor (C_s) will deviate from its nominal value of $0.46V_{dc}$. This property is utilized to bring back the capacitor voltage to its nominal value in case the capacitor voltage has deviated from the nominal value.

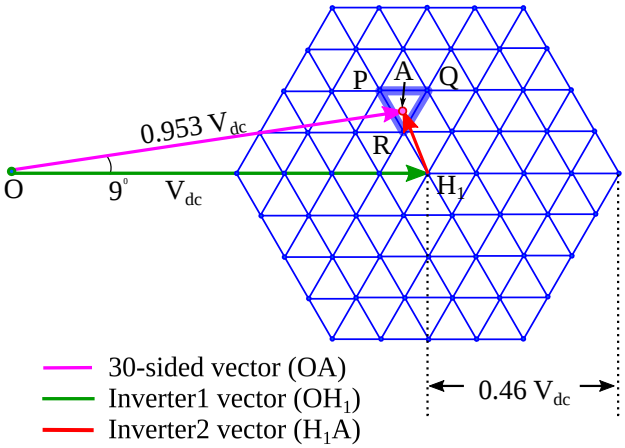

Figure 3. Generation of 30-sided space vector OA

IV. Capacitor Balancing

A. Inverter1 FC and CHB capacitors

Inverter1 FC and CHB capacitors are balanced by applying pole voltage redundancies. For example, to apply a pole voltage of $0.25V_{dc}$ in A-phase (V_{AO} = $0.25V_{dc}$), there are 3 possible redundant ways: (a) 0 + 0 + $0.25V_{dc}$, (b) 0 + $0.5V_{dc}$ - $0.25V_{dc}$ and (c) V_{dc} - $0.5V_{dc}$ - $0.25V_{dc}$. For redundancy "a", CHB capacitor will discharge and for redundancies "b" and "c", CHB capacitor will get charged for positive direction of phase current. For negative value of phase current, redundancy "a" will charge the CHB capacitor and redundancies "b" or "c" will discharge the CHB capacitor. According to phase current direction and state of the capacitor (overcharged or undercharged), appropriate redundancies are applied to charge balance the CHB capacitors. Now, it can be observed that while applying redundancy "a" FC capacitor is not affected and during redundancy "b" and "c" FC capacitor is affected. If redundancy "b" is applied, FC capacitor will discharge and while applying redundancy "c" FC capacitor will charge for positive polarity of phase current. For negative phase current, the effect on FC capacitor is vise versa. By properly selecting the redundancies according to the state of capacitor and phase current polarity, the FC capacitors can be charge balanced.

B. Inverter2 FC, CHB and Common capacitor

In Inverter 2, the ratio of Inverter2- Common capacitor voltage: FC capacitor voltage: HB capacitor voltage is maintained at 4:2:1, which is similar to that of Inverter1. So the CHB capacitor voltage and the FC capacitor voltage can be maintained at the nominal value using pole voltage redundancies as discussed in the above section (Section IV-A).

Inverter2 common capacitor (C_s) voltage is controlled by varying the k_0 and k_1 ratio in a similar algorithm as discussed in [11].

V. Implementation

A. PWM Implementation

The resultant 30-sided SVS is split into 480 triangles. Any reference vector (V_R) lying in this triangle is generated by

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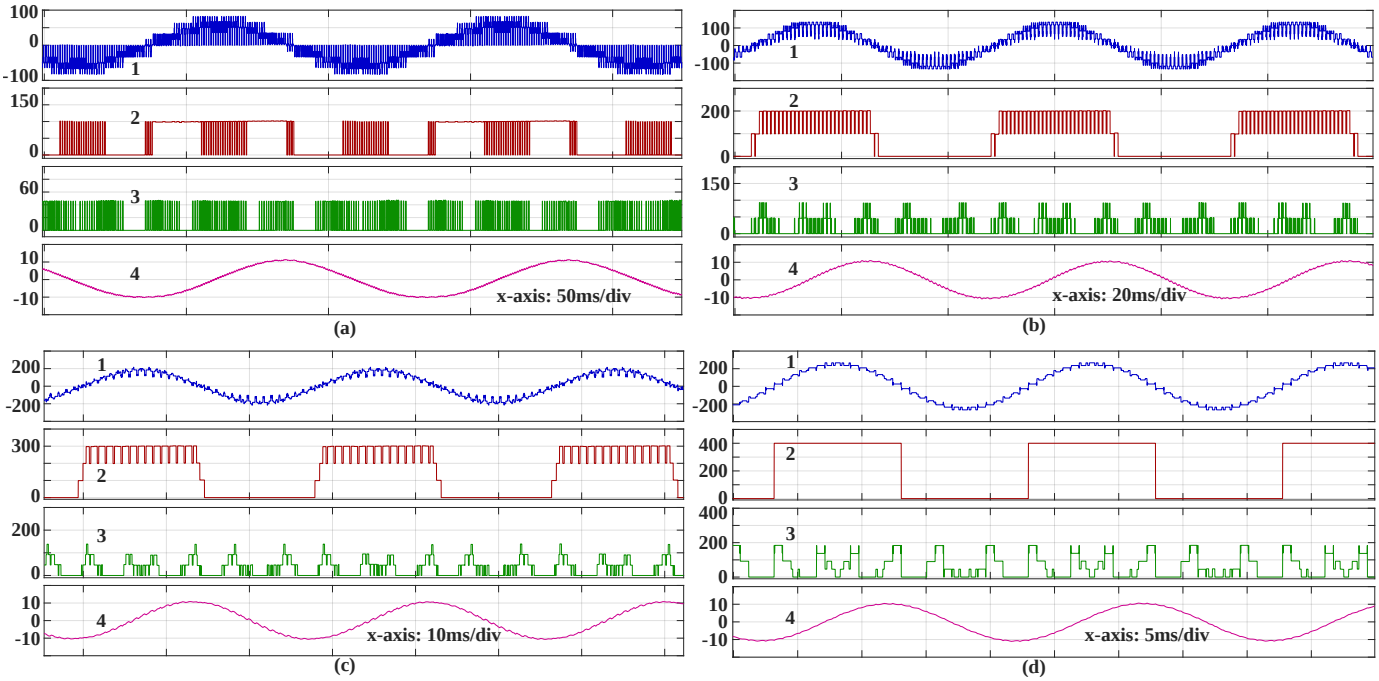

Figure 4. Simulation results for (a) 10Hz, (b) 22Hz, (c) 35Hz and (d) 50Hz. Traces: 1. Motor phase voltage ($V_{AA'}$), 2. Inverter1 pole voltage (V_{AO}), 3. Inverter2 pole voltage ($V_{A'O'}$) and 4. Motor phase current (I_A)

time averaging the vertex vectors of the triangle V_0, V_1 and V_2 for time duration T_0, T_1 and T_2 respectively for a sampling duration T_S, as given in (3) .

$$V_R T_s = V_0 T_0 + V_1 T_1 + V_2 T_2 \tag{3}$$

In this work, PWM sequence of V_1-V_0-V_2 is applied for T_1-T_0-T_2 duration . Usage of this PWM strategy reduces the number of switching in the high voltage blocking Inverter1. In every T_x (x = 0,1,2) duration, Inverter2 vectors are switch averaged in k_0: k_1: 1-(k_0+k_1) ratio to generate the required Inverter2 space vector.

B. Simulation and Hardware implementation

The proposed scheme is simulated on MATLAB Simulink environment by modelling the inverter and motor. Then the scheme is also verified experimentally on a 200V, 10kW, 50Hz open end induction motor. For generating the gating pulses, DSP-FPGA platform is used. Texas instrument's TMS320F28335 is used as DSP and Xilinx XC3S200 is used as FPGA. The gate signals are passed through a hardware logic which adds an extra layer of protection to any accidental shoot through of the DC-link. Semikron's SKM100GB12T4 is used for power switches for the proposed scheme.

VI. Results

Simulation studies are performed to validate the proposed scheme. A DC-link voltage of 400V (V_{dc} = 400V) is considered for simulation. The steady state results obtained during 10Hz, 22Hz, 35Hz and 50Hz are shown in Figure.4 . It can be noted from the Inverter1 pole voltage (Figure.4 Trace 2) that, Inverter1 which blocks higher voltage have less number of switching transitions during a fundamental cycle. This results in reduced switching losses in the system.

Figure. 5 shows the frequency spectrum of the motor phase voltage, Inverter1 pole voltage and Inverter2 pole voltage at 35Hz of operation (steady state waveform shown in Figure. 4). Here the lower order harmonics generated by Inverter1 (Figure. 5 Trace 2) is cancelled by the pole voltage generated by Inverter2 (Figure. 5 Trace 3), yielding a motor phase voltage devoid of lower order harmonics till 25th order from motor phase voltage.

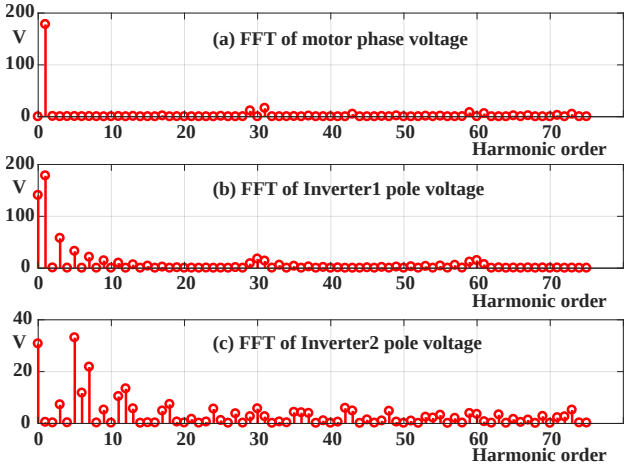

Figure 5. FFT at 35 Hz of operation (a) Motor phase voltage ($V_{AA'}$), (b) Inverter1 pole voltage (V_{AO}) and (c) Inverter2 pole voltage ($V_{A'O'}$)

Figure. 6 shows the capacitor voltages during 35Hz of operation. The floating capacitors C_{1pA}, C_{2pA}, C_{1sA}, C_{2sA}

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and C_s are maintained at 200V, 100V, 92V, 46V and 184V respectively at their nominal value by PWM operation.

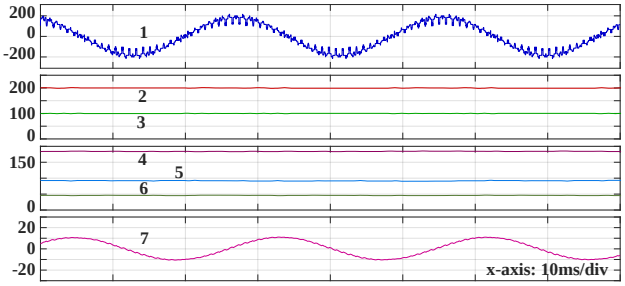

Figure 6. Steady state operation at 35 Hz of operation with floating capacitor voltages. Traces: (1) Motor phase voltage ($V_{AA'}$) (V), (2) Inverter1 FC capacitor (V_{C1pA}) voltage (V), (3) Inverter1 CHB capacitor (V_{C2pA}) voltage (V), (4) Inverter2 common capacitor (V_{Cs}) voltage (V), (5) Inverter2 FC capacitor (V_{C1sA}) voltage (V), (6) Inverter2 CHB capacitor (V_{C2sA}) voltage (V) and (7) Motor phase current (I_A)

Transient operation of the drive is performed in Figure. 7, where the motor is accelerated from 10Hz to 49Hz. It can be noted that, all the floating capacitors are tightly maintained to its nominal value even during transients.

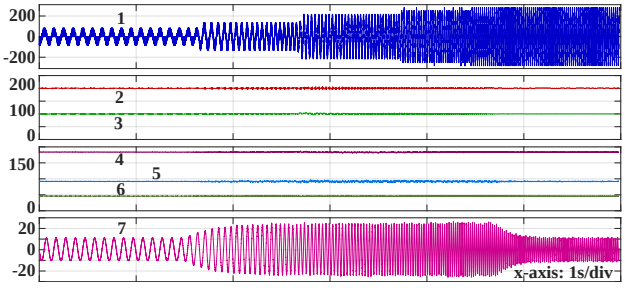

Figure 7. Acceleration of the motor from 10Hz to 49Hz. Traces: (1) Motor phase voltage ($V_{AA'}$) (V), (2) Inverter1 FC capacitor (V_{C1pA}) voltage (V), (3) Inverter1 CHB capacitor (V_{C2pA}) voltage (V), (4) Inverter2 common capacitor (V_{Cs}) voltage (V), (5) Inverter2 FC capacitor (V_{C1sA}) voltage (V), (6) Inverter2 CHB capacitor (V_{C2sA}) voltage (V) and (7) Motor phase current (I_A)

Experimental result of steady state operation at 35Hz is shown in Figure. 8. Motor phase voltage, Inverter1 pole voltage, Inverter2 pole voltage and phase current can be seen in Trace 1, Trace 2, Trace 3 and Trace 4 respectively. It can be clearly observed that the experimental oscillogram shown in Figure. 8 have a close resemblance with the simulated result shown in Figure. 4(c).

VII. Conclusion

A 5-level, 30-sided polygonal SVS using a single DC link is proposed in this paper. This scheme eliminates lower order harmonics (till 25th order) from the machine phase voltage throughout the modulation range including over-modulation. The scheme enables the advantages of multilevel inverters like lesser dv/dt in machine phase voltage, use of lower voltage blocking devices etc. Here, higher voltage blocking switches in Inverter1 has lesser switching transitions compared to low voltage blocking switches in Inverter2, thereby reducing the overall switching loss in the system. Due to the elimination

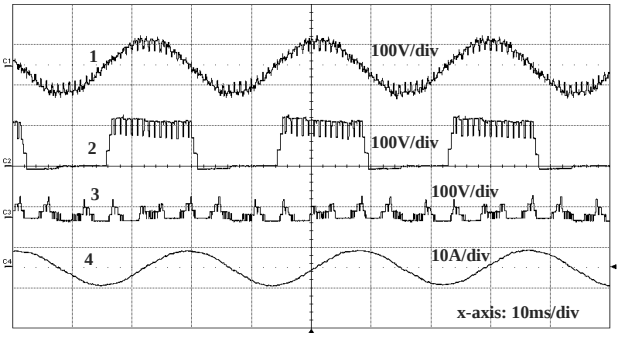

Figure 8. Experimental waveform at 35Hz operation. Traces: 1. Motor phase voltage ($V_{AA'}$), 2. Inverter1 pole voltage (V_{AO}), 3. Inverter2 pole voltage ($V_{A'O'}$) and 4. Motor phase current (I_A)

of lower order harmonics, this scheme is an apt alternative to bulky passive LC filters. As this scheme delivers refined output voltage, this scheme can be used for high performance medium to high power drive applications.

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