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# Charge-Density Wave Driven Giant Thermionic-Current Switching in 1T-$TaS_2$/2H-$TaSe_2$/2H-$MoS_2$ Heterostructure

*Mehak Mahajan and Kausik Majumdar**

**1T-$TaS_2$ exhibits several resistivity phases due to the modulation of charge density wave (CDW). The fact that such phase transition can be driven electrically has attracted a lot of attention in the recent past toward *active-metal* based electronics. However, the bias-driven resistivity switching is not very large (less than five-fold), and an enhancement in the same will highly impact such phase transition devices. One aspect that is often overlooked is that such phase transition is also accompanied by a significant change in the local temperature due to the low thermal conductivity of 1T-$TaS_2$. In this work, such electrically driven phase transition induced temperature change is exploited to promote carriers over a thermionic barrier in a 1T-$TaS_2$/2H-$TaSe_2$/2H-$MoS_2$ T-Junction, achieving a 964-fold abrupt switching in the current through the $MoS_2$ channel. The device is highly reconfigurable and exhibits an abrupt reduction in current as well when the biasing configuration changes. The results are promising for several electronic applications, including neuromorphic chips, switching, nonlinear devices, and industrial electronics such as current and temperature sensing.**

## 1. Introduction

The charge density wave (CDW) driven phase transition in layered materials like $TaS_2$, $TaSe_2$, $NbSe_2$, and $TiSe_2$ has attracted a lot of attention in the recent past due to their structural, thermal, magnetic, electrical, and optical properties.[1–5] Out of all these, 1T-$TaS_2$ exhibits polymorphic states with distinctive resistive phases, that can be achieved by thermal,[6,7] mechanical,[8,9] optical,[10,11] and electrical[12,13] excitation. On heating, 1T-$TaS_2$ transits from commensurate (C) to triclinic (T) phase at 223 K, T to non-commensurate (NC) phase at 283 K, NC to incommensurate (IC) phase at 353 K and IC to metallic phase at 550 K. On the other hand, 2H-$TaSe_2$ that undergoes C to NC phase transition at 90 K and NC to metallic phase at 120 K shows a slight change in slope of resistance versus temperature curve. Unlike 1T-$TaS_2$, 2H-$TaSe_2$ does not exhibit a sharp change in the resistance during the phase transitions.

The fact that in 1T-$TaS_2$, the resistance switching through such phase transitions can be obtained through Joule heating by electrical driving,[12–14] has led to several electronic and optoelectronic device applications.[10,15–17] The resistance switching ratio plays an important role in determining the performance of these devices. However, the degree of the resistance switching is often weak, less than five,[12,13,16] depending on the flake thickness, measurement temperature, and crystal quality. Any technique that can enhance the ratio of the resistance switching will be of great importance in such phase transition-based device applications. In this work, we propose a method using a 1T-$TaS_2$/2H-$TaSe_2$/2H-$MoS_2$ T-junction, where we achieve a gate-controllable current switching ratio up to 964 driven by CDW phase change in 1T-$TaS_2$ – which is more than 190-fold enhancement in the switching ratio compared to existing reports. The principle of operation of the device exploits the abrupt change in the junction temperature due to an abrupt change in the current resulting from Joule heating induced CDW phase transition in $TaS_2$. This, in turn, helps to promote carriers over a thermionic barrier, modulating the net probe current. Interestingly, the proposed device is electrically reconfigurable between a positive jump (enhancement in current) and a negative jump (reduction in current). Such reduction in current can be modeled as an effective negative differential resistance (NDR), as shown earlier.[17]

## 2. Results and Discussion

The 3D schematic diagram of the proposed triple layered T-junction is shown in **Figure 1**a. The inset of Figure 1b shows the optical image of the device $D_a$ fabricated by exfoliating a few layer $MoS_2$ flake on Si/$SiO_2$ substrate followed by layer-by-layer dry transfer of $TaSe_2$ and $TaS_2$ flakes, respectively (see Experimental Section for complete fabrication steps). The current ($I$)–voltage ($V$) characteristics of the $TaS_2$/$TaSe_2$ junction of the device $D_a$ probed between terminals T and $T_S$ (with terminal M kept open) at 296 K are shown in Figure 1b. The abrupt hysteretic jump in the current (≈1.24) results from the reduction in the $TaS_2$ resistance owing to electrically driven NC-IC CDW phase transition. Note that $TaSe_2$ being highly conductive, carries ample current to drive NC–IC phase transition of $TaS_2$ in $TaS_2$/$TaSe_2$ junction.[3] Also, the low thermal conductivity of $TaSe_2$ compared to Au contact further aids in raising the local

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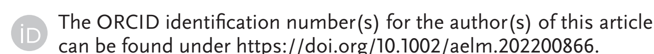
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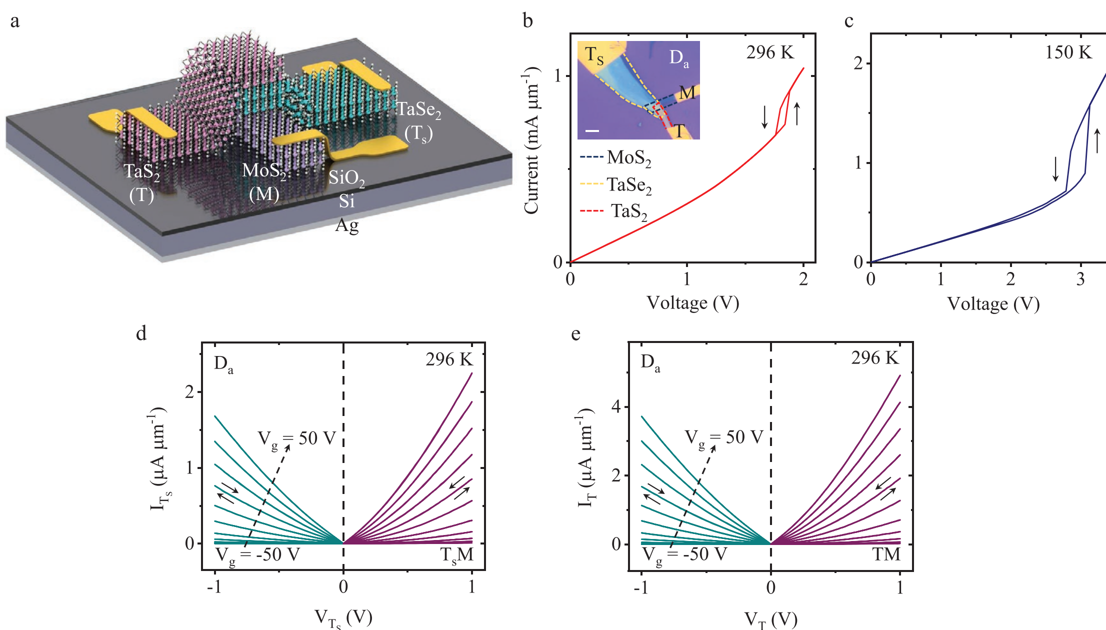


**Figure 1.** Electrical characterization of individual materials and heterojunctions of the T-junction. a) Schematic representation of triple layered T-junction. The Ag contact is used as a global back gate. b) Current–voltage characteristics of two-probe $TaS_2/TaSe_2$ junction (probed between terminals $T_S$ and T of $D_a$) indicating the NC-IC phase transition of $TaS_2$ at 296 K. Inset: the optical image delineating each layer of the fabricated triple layered T-junction ($D_a$) (scale bar: 5 µm). c) Current–voltage characteristics of $TaS_2/TaSe_2$ junction at 150 K. Forward and reverse sweeps are indicated by black arrows. d) *I–V* characteristics of $TaSe_2/MoS_2$ junction, probed between terminals $T_S$ and M keeping terminal T open, for $V_g$ varying from −50 to 50 V in steps of 10 V at 296 K. e) *I–V* characteristics of $TaS_2/MoS_2$ junction, probed between terminals T and M keeping terminal $T_S$ open, as a function of $V_g$ varying from −50 to 50 V in steps of 10 V at 296 K.

temperature of the channel.[18,19] The current jump can be further enhanced at low temperatures by invoking phase transition through multiple metastable states of $TaS_2$ using the external electric field.[10,16] Figure 1c depicts the *I–V* characteristics of the $TaS_2/TaSe_2$ junction of the device $D_a$ at 150 K showing a current jump of ≈1.77. Note that when a material with lower conductivity (such as $SnSe_2$) replaces the series resistance material (i.e., $TaSe_2$), the overall current is suppressed, which reduces the Joule heating. Hence, the phase transition in $TaS_2$ does not occur anymore (Figure S1, Supporting Information).

The current–voltage characteristics of $TaSe_2/MoS_2$ junction (probed between terminals $T_S$ and M keeping terminal T open) and $TaS_2/MoS_2$ junction (probed between terminals T and M keeping terminal $T_S$ open) as a function of back-gate voltage ($V_g$) varying from −50 to 50 V in steps of 10 V at 296 K are outlined in Figure 1d,e, respectively. The forward and reverse sweep directions of the voltage during measurement (indicated by the black arrows in Figure 1d,e) show negligible hysteresis, suggesting excellent interface quality in the device. The corresponding gate-dependent current–voltage characteristics of both the junctions at 150 K are depicted in Figure S2a,b, Supporting Information, respectively.

### 2.1. Reconfigurable Abrupt Current Switching in T-Junction

We now show the characteristics of 1T-$TaS_2$/2H-$TaSe_2$/2H-$MoS_2$ T-junction that is reconfigurable between abrupt current increment and decrement by utilizing the modulation of the $MoS_2$ resistance through an external gate voltage. In this device, we pass a high current through a voltage bias through the $TaS_2/TaSe_2$ path and use the branched out $MoS_2$ channel current as a probe. The equivalent circuit diagram of the four terminal device $D_a$ is shown in **Figure 2**a wherein $R_1$, $R_2$, and $R_3$ correspond to the effective resistance of $TaSe_2$, $TaS_2$, and $MoS_2$ flakes, respectively. Here, $R_3$ includes both the $TaSe_2/MoS_2$ Schottky junction resistance and the $MoS_2$ channel resistance, and both the components are tunable by the gate voltage. A global back gate is connected to the fourth terminal of the device. Figure 2b shows the variation of $MoS_2$ channel current ($I_M$) with $V_{T_S}$ of the device $D_a$ when we apply the bias at $T_S$ terminal while keeping T and M terminals grounded. The characteristics show current decrement behavior for both $V_{T_S} < 0$ V and $V_{T_S} > 0$ V for $V_g$ varying from −50 to 50 V in steps of 10 V at 296 K. When the external bias exceeds the threshold voltage for the NC-IC phase transition of $TaS_2$, the $TaS_2$ resistance abruptly reduces resulting in the abrupt increment in the $TaS_2$ current, and hence a simultaneous reduction in the $MoS_2$ current. The peak-to-valley current ratio (PVCR) obtained for $V_{T_S} < 0$ V and $V_{T_S} > 0$ V at 296 K are shown in bottom panel of Figure 2g. A simplistic way to further improve the PVCR values is by increasing the switching ratio of the $TaS_2$ resistance, which directly regulates the abrupt change in the $MoS_2$ current. A base temperature lower than the C-T phase transition temperature can be utilized to achieve such enhancement. We operate the device ($D_a$) at a temperature below the C-T transition temperature to invoke field-driven metastable states of $TaS_2$ that increase the abrupt current jump by 1.42 × in comparison to room temperature. Figure 2c depicts $I_M$ versus $V_{T_S}$ characteristics delineating current decrement at


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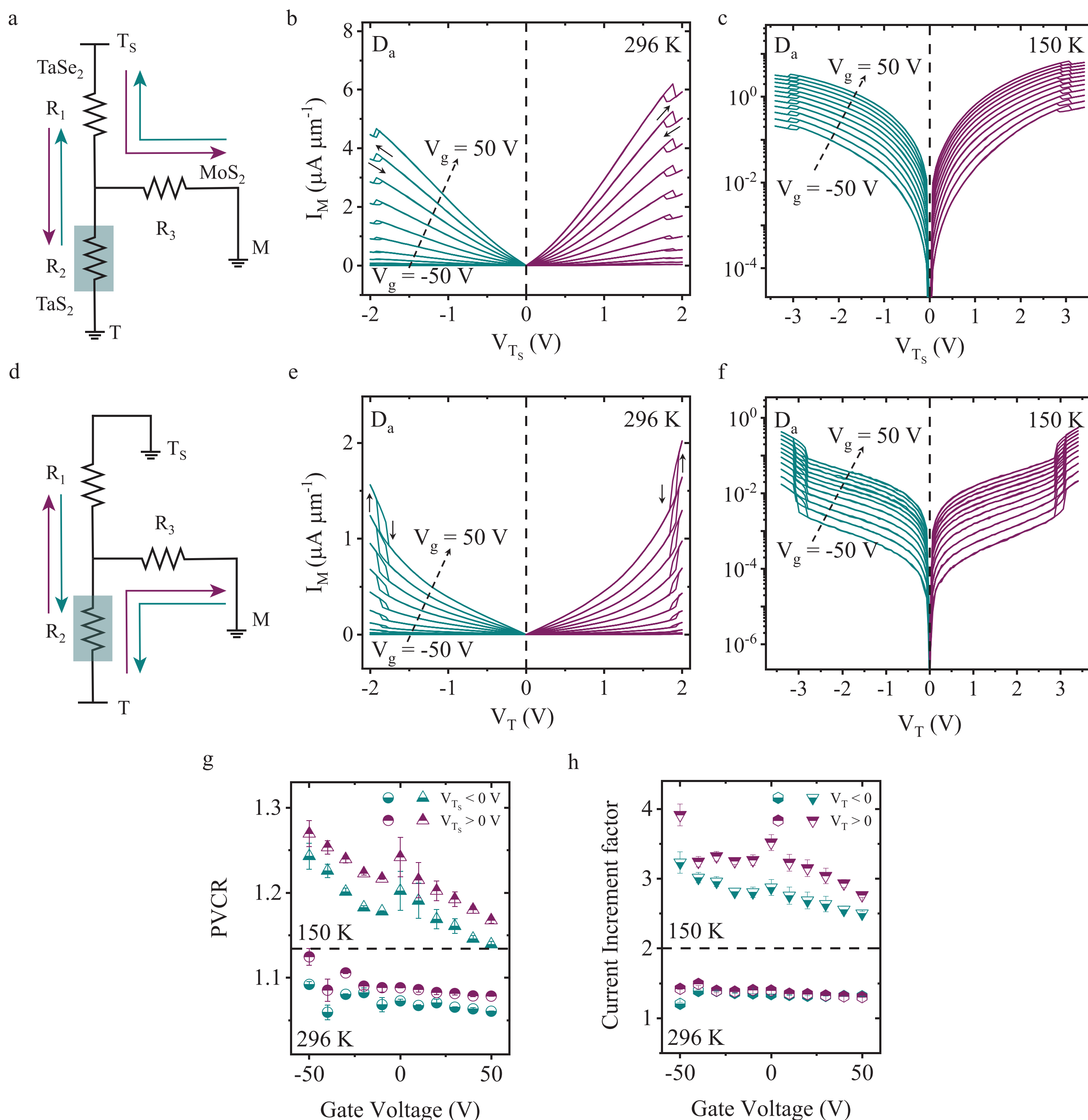


**Figure 2.** Gate-tunable, reconfigurable abrupt current increment and negative differential resistance. a,d) The three branches of the device $D_a$ depicted by three effective resistances $R_1$, $R_2$, and $R_3$, corresponding to $TaSe_2$, $TaS_2$, and $MoS_2$, respectively, for $TaSe_2$ (T) biasing (in (a)) and $TaS_2$ ($T_S$) biasing (in (d)). $R_3$ includes the $MoS_2$ branch resistance and the $TaSe_2/MoS_2$ Schottky junction resistance. The cyan box (in the $TaS_2$ branch) indicates the branch where CDW phase transition occurs. The arrows indicate the direction of the current flow in different biasing configurations. b,c) Current through the $MoS_2$ branch ($I_M$) versus $V_{T_s}$ as a function of $V_g$ varying from −50 to 50 V in steps of 10 V at 296 and 150 K depicting current decrement for both $V_{T_s} > 0$ and $V_{T_s} < 0$. Forward and reverse sweeps are indicated by black arrows. e,f) $I_M$ versus $V_T$ as a function of $V_g$ varying from −50 to 50 V in steps of 10 V at 296 and 150 K depicting abrupt current increment for both $V_T > 0$ and $V_T < 0$. Forward and reverse sweeps are indicated by black arrows. g) Peak-to-valley current ratio (PVCR) as the function of $V_g$ at 296 and 150 K in bottom and top panel respectively. h) Current increment factor as a function of $V_g$ at 296 and 150 K in bottom and top panel, respectively.

150 K. The corresponding PVCR values at 150 K are shown in the top panel of Figure 2g reaching a maximum value of 1.27 at $V_g = -50$ V for $V_{T_s} > 0$ V which is higher in comparison to the room temperature values.

Suppose we apply the bias at the $TaS_2$ terminal while keeping terminals $T_S$ and M grounded as depicted in the equivalent circuit in Figure 2d. In that case, the $MoS_2$ current exhibits an abrupt increment instead of a decrement at the phase

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transition. When we apply a high electric field across the $TaS_2$/$TaSe_2$ junction, the $TaS_2$ phase transition occurs, which reduces the resistance of the $TaS_2$ branch resulting in the abrupt increment in the $TaS_2$ current as well as the $MoS_2$ current. Here, the total current flow through $R_2$ instead of $R_1$ (in the case of $TaSe_2$ biasing) as shown by the arrows in Figure 2d. Figure 2e,f shows the gate voltage ($V_g$) dependent current increment characteristics for both $V_T < 0$ V and $V_T > 0$ V at 296 and 150 K, respectively. The corresponding current increment factor as the function of $V_g$ for both 296 and 150 K is shown in Figure 2h. Current increment factor reaches a maximum value of ≈4 at 150 K for $V_T > 0$ V which is ≈2.75 × higher than the room temperature value.

The low-temperature current increment factor of four cannot solely result from phase transition induced resistance switching of $TaS_2$ as it is limited to a factor of ≈1.77 as shown in Figure 1c. In addition to 1T-$TaS_2$, 2H-$TaSe_2$ also exhibits CDW phase transitions at 90 and 120 K. However, it does not cause any abrupt discontinuity in the $TaSe_2$ resistance apart from a slight slope change in resistance versus temperature curve.[3,20,21] The overall change in resistance of the $TaSe_2$ branch from the estimated temperature values (discussed later) is small and rules out the contribution of $TaSe_2$ resistance change to the current jump. Also, the heat equation solution of the channel and the in situ Raman measurement exclude the possibility of structural phase transition of $MoS_2$ from the semiconducting (2H) to metallic (1T) phase. The abrupt current increment due to the $TaS_2$ phase transition increases the local temperature along the device channel. The 1D heat equation solution (using FEM) for the $TaS_2$/$TaSe_2$ channel estimates that the local temperature increment due to Joule heating is sufficient to invoke $TaS_2$ phase transitions (see Figure S3, Supporting Information), depending upon the base temperature as well as the external bias. However, it is not enough to induce structural 2H to 1T phase transition in $MoS_2$.[22] This argument is further supported by bias-dependent Raman measurement (see Figure S4, Supporting Information), wherein j-peaks have not been observed, which could otherwise confirm the presence of the 1T-phase of $MoS_2$.

Such a large current increment can be explained by the enhanced thermionic carrier injection across the $TaSe_2$/$MoS_2$ barrier with a sudden increase in the junction temperature resulting from the Joule heating induced phase transitions of $TaS_2$, as detailed next. The mechanism is schematically illustrated in **Figure 3**a,b. The abrupt jump in temperature due to the CDW phase transition in $TaS_2$ causes a corresponding increment in temperature at the $TaSe_2$/$MoS_2$ junction due to efficient heat conduction through the $TaS_2$/$TaSe_2$ interface. That, in turn, enhances the kinetic energy of the carriers, helping them overcome the $TaSe_2$/$MoS_2$ Schottky barrier.

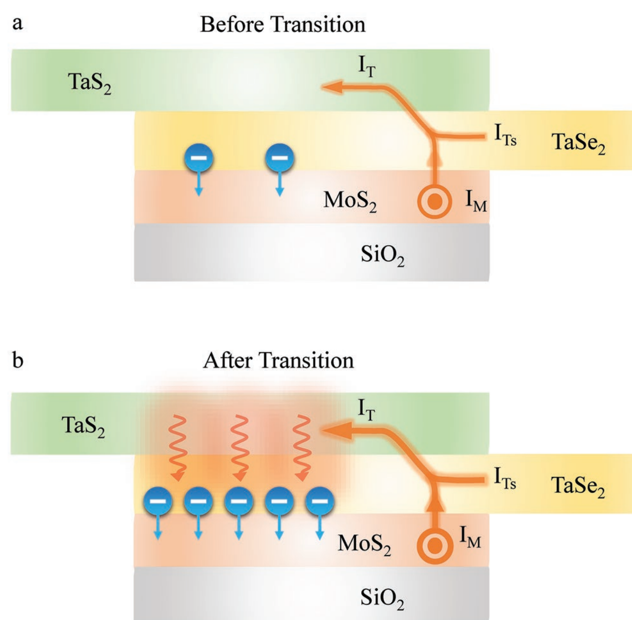


**Figure 3.** Schematic illustration of the mechanism. Schematic representation of the situation a) before and b) after the CDW phase transition in $TaS_2$. The orange arrow and the out-of-plane direction symbol indicate the direction of the current flow though the junction and in the $MoS_2$ channel, respectively. The heat flow from $TaS_2$ to the $TaSe_2$/$MoS_2$ junction in (b) is indicated by the red curved arrows. The abrupt enhancement in temperature promotes a larger number of electrons through the $TaSe_2$/$MoS_2$ Schottky barrier, in turn causing an abrupt change in the $MoS_2$ channel current.

### 2.2. Giant Current Increment Driven by Thermionic Switching

To explore the thermionic effect due to local temperature switching, we fabricate another triple layered T-junction ($D_b$) comprising a narrow $MoS_2$ channel with a reduced junction overlap area (see the optical image in the inset of **Figure 4**a). Here we choose a small junction overlap area between $MoS_2$ and the $TaS_2$/$TaSe_2$ to further increase the temperature by forcing the hot electrons to pass through a smaller region. Apart from weaker heat dissipation efficiency, the smaller junction area helps in two other ways. First, when the junction area is small, the fractional contribution of the junction resistance to the total device resistance increases. That helps to achieve a larger switching ratio since the hot carriers, due to the phase transition-induced temperature change, primarily modulate the junction resistance. Second, a smaller overlap area helps to remove any trapped residue and air from the interface during annealing, which in turn helps to achieve closer proximity between $MoS_2$ and $TaSe_2$/$TaS_2$ heater, helping the $MoS_2$ layer to achieve a higher temperature effect at the junction during the switching. $I_M$ versus $V_T$ of device $D_b$ for selective $V_g$ values varying from 20 to 50 V (step size: 10 V) at 300 K for $V_T < 0$V is depicted in Figure 4a. Similarly, Figure 4b shows the $I_M$ versus $V_T$ for $V_T > 0$ V at $V_g$ equal to 0, 30, and 50 V. The corresponding current increment factors during the phase transition are plotted in Figure 4c showing a maximum value of ≈3 at $V_g = -10$ V for $V_T > 0$ V at 300 K which is 2 × higher in comparison to the current increment factor of device $D_a$.

At low temperature, we could further enhance the current jump as depicted in $I_M$ versus $V_T$ characteristics of device $D_b$ at 77 K (see Figure 4d,e for $V_T < 0$ V and $V_T > 0$ V, respectively) for different $V_g$ values. The corresponding current increment factors are plotted in Figure 4f for both $V_T < 0$ V and $V_T > 0$ V. We could enhance the $MoS_2$ current by a factor of ≈964 at $V_g = 10$ V for $V_T > 0$ V as represented in Figure 4f. As discussed earlier, such a huge jump can not solely arise from electrically

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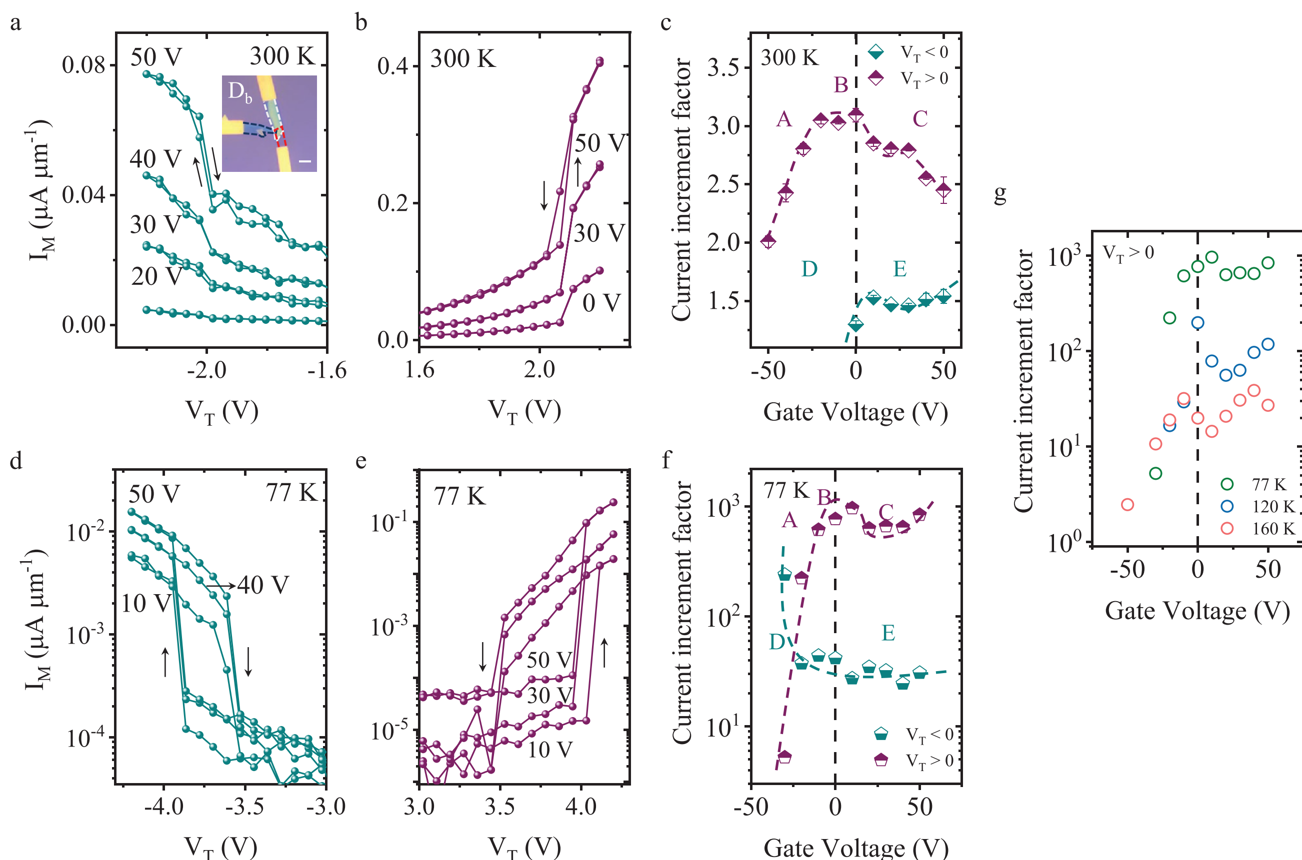


**Figure 4.** Giant current increment in triple layered junction. a,b) $I_M$ versus $V_T$ for selected $V_g$ at 300 K for $V_T < 0$ (in (a)) and $V_T > 0$ (in (b)) depicting abrupt current increment. Forward and reverse sweeps are indicated by black arrows. The inset of (a) shows the optical image of the fabricated triple layered T-junction ($D_b$) (scale bar: 5 μm). d,e) $I_M$ versus $V_T$ for selected $V_g$ at 77 K for $V_T < 0$ (in (d)) and $V_T > 0$ (in (e)) depicting abrupt current increment. c,f) Current increment factor as the function of $V_g$ at 300 K (in (c)) and 77 K (in (f)) extracted from (a,b) and (d,e), respectively. g) Current increment factor as a function of $V_g$ at 77, 120, and 160 K.

driven $TaS_2$ phase transition. And, we must invoke the corresponding sudden rise in the junction temperature due to the abrupt enhancement in current through $TaS_2/TaSe_2$ during the CDW phase transition of $TaS_2$. Figure 4g depicts the variation of the current increment factor as a function of $V_g$ at a base temperature of 77, 120, and 160 K for $V_T > 0$ V. Such a strong temperature dependence in the current increment factor suggests possible usage of the technique in sensing temperature.

In Figure 4f for $V_T > 0$ V, the current jump ratio at the phase transition exhibits a strong non-monotonic behavior with $V_g$. Also, the ratio shows an opposite trend for $V_T < 0$ V, particularly when $V_g < 0$ V. The origin of such behavior is explained in **Figure 5**. In the case of $V_T > 0$ V, that is, when $MoS_2$ injects electrons into $TaSe_2$, there are three different regions of device operation (namely A, B, and C as shown in Figure 4c,f) as schematically explained in Figure 5a. Note that, due to the high electrical conductivity of $TaSe_2$ in comparison to $TaS_2$ (in particular, at a low temperature), the floating voltage at the triple junction is small; hence the drop across the $MoS_2$ channel is also small (estimated to be <26 mV). Due to such a small effective drain voltage, the current through the $MoS_2$ channel strongly depends on the drain barrier as well in the different regimes of operation. In the current situation, where $TaSe_2$ acts as the drain contact for $V_T > 0$ V configuration, the drain barrier plays an even more important role. We recently found that due to van der Waals nature of the contact interface, $TaSe_2$ exhibits strong Fermi level depinning[23] with layered semiconductors. Accordingly, due to the relatively large work function of $TaSe_2$, the conduction band offset between $MoS_2$ and $TaSe_2$ is large. On the other hand, due to Fermi level pinning, Ni/$MoS_2$ junction has a relatively small Schottky barrier height.[24] That leads to a larger drain barrier compared to the source barrier at the small effective drain bias as schematically shown in Figure 5a, and hence the $TaSe_2/MoS_2$ interface controls the drain current.

In region A, that is, for $V_g \ll 0$ V, electrons do not see any barrier at the drain side and can quickly transfer into $TaSe_2$ (see top panel of Figure 5a). Thus, the current does not change much with the abrupt increase in temperature during the CDW phase transition. In region B, the electrons from the $MoS_2$ region require to overcome the drain barrier to be transferred to $TaSe_2$ (see middle panel of Figure 5a), and thus the current is a strong function of the local temperature at the drain barrier. The current induced Joule heating can increase the local temperature to ≈230 K for a base temperature of 77 K (see Figure S3, Supporting Information, for simulated results). The current jump ratio simulated for various barrier heights ($\phi_b$ varying


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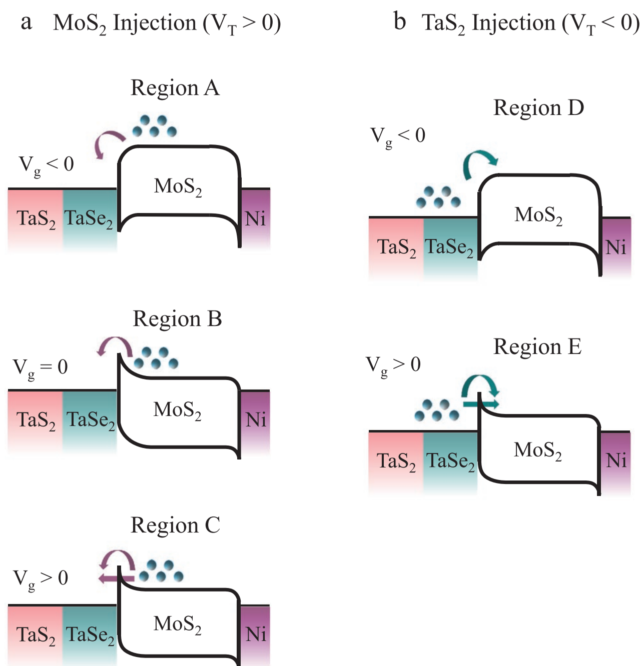


**Figure 5.** Thermionic switching behavior. a) Band alignment schematics for $V_T > 0$, that is, when $MoS_2$ injects electron into $TaSe_2$ through the drain barrier at $V_g < 0$ (in top panel), $V_g = 0$ (in middle panel), and $V_g > 0$ (in bottom panel) corresponding to region A, B, and C in Figure 4. b) Band diagram for $TaSe_2$ injection into $MoS_2$ through the source barrier ($V_T < 0$) for $V_g < 0$ (in top panel), and $V_g > 0$ (in bottom panel) illustrating region D and E from Figure 4c,f.

from 30 to 80 meV) by solving modified Richardson's equation[24] at temperatures of 120, 150, 180, 210, and 240 K with respect to 77 K is shown in Figure S5, Supporting Information. The simulation results clearly show that the current ratio before and after the phase transition can go as high as $10^4$ depending upon $\phi_b$. That justifies the high current increment factor at $V_g = 10$ V. Finally, in region C for $V_g \gg 10$ V, the band bending increases, and the electrons can tunnel through the Schottky drain barrier, as shown in the bottom panel of Figure 5a. Thus, the local temperature does not affect the current, reducing the current ratio before and after the phase transition. Beyond region C, at an even higher positive $V_g$, we observe an increment in the current increment factor, the origin of which is yet not very clear and could result from a $V_g$ dependent change in the relative resistance between the source and the drain barriers.

On the other hand, for $V_T < 0$ V, $TaSe_2$ acts as a source contact, and the electrons are injected from $TaSe_2$ to the $MoS_2$ channel. At high negative $V_g$, that is, region D, the carrier injection is determined by thermionic transport over the Schottky barrier height at $TaSe_2/MoS_2$ interface, as shown in the top panel of Figure 5b, and hence contributes to higher current jump. However, for $V_g > 0$ V (region E), the current increment ratio decreases monotonically as the carrier injection is dominated by the tunneling phenomenon schematically shown in the bottom panel of Figure 5b.

In similarity to device $D_a$, the $I_M$ versus $V_{T_s}$ characteristics of device $D_b$ exhibits current decrement for $V_{T_s}$ biasing at both 300 and 77 K (see Figure S6, Supporting Information). The corresponding $I_M$ versus $V_T$ (depicting current increment) and $I_M$ versus $V_{T_s}$ (depicting current decrement) characteristics for device $D_b$ at 120 and 160 K are outlined in Figures S7 and S8, Supporting Information, respectively. The current increment characteristics have been repeatedly observed in several devices, some of which are outlined in Figures S9 and S10, Supporting Information.

## 3. Conclusion

The technique proposed in this work demonstrates a unique way of significantly amplifying the resistance switching ratio typically obtained from a $TaS_2$ CDW phase transition. That is achieved by exploiting enhanced carrier injection through a Schottky barrier height by the abrupt increment in the local temperature during the phase transition. Accordingly, the technique can be applied to enhance the device performance in several applications where $TaS_2$ phase transition is used, for example, in detecting infrared photons and neuromorphic applications. In addition, the gate tunable sharp jump in current can be useful for sensing applications, such as temperature and current. On the other hand, the enhancement in the $MoS_2$ channel current during the CDW phase transition of $TaS_2$ provides an excellent probe to monitor the local temperature of $TaS_2$.

## 4. Experimental Section

*Triple Layered T-Junction Device Fabrication and Characterization*: 1T-$TaS_2$/2H-$TaSe_2$/2H-$MoS_2$ T-junction was fabricated in the following manner. First, the thin flakes of $MoS_2$ were mechanically exfoliated on a heavily doped Si substrate coated with 285 nm thick $SiO_2$ using polydimethylsiloxane (PDMS), followed by dry transfer of $TaSe_2$ and $TaS_2$ flakes, respectively. A rotational stage controlled the alignment during each layer transfer to form the T-junction. The complete exfoliation and dry transfer processes were done at room temperature. The substrate was then spin-coated with a high contrast positive resist—polymethyl methacrylate (PMMA) 950 C3 and softly baked for 2 min at 180 °C. Patterns were formed through electron beam lithography with an electron beam dose of 200 μC $cm^{-2}$, an electron beam current of 300 pA, and an acceleration voltage of 20 KV. The pattern development was carried out in 1: 3 MIBK/IPA developer solution followed by IPA wash and blow drying in $N_2$. Metal contacts were formed by blanket deposition of 10 nm Ni / 50 nm Au using a DC magnetron sputter coating system in the presence of Ar plasma at $6.5 \times 10^{-3}$ Torr. Excess metal lift-off was carried out by immersing the substrate in acetone for 15 – 30 min, followed by IPA wash for 30 s and blow drying in $N_2$. Buffered HF solution was used to etch the back oxide from the substrate, and highly conducting silver paste was used for the back gate contact.

The electrical measurements were carried out in a probe station with a base vacuum level of about $1.6 \times 10^{-3}$ Torr at room temperature and $6.45 \times 10^{-6}$ Torr at the low temperature with the supply of liquid $N_2$.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.


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## Conflict of Interest

The authors declare no conflict of interest.

## Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

## Keywords

1T-$TaS_2$, 2H-$MoS_2$, 2H-$TaSe_2$, charge density waves, current switching, negative differential resistance, phase transitions

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