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This Special Issue is focused on the material challenges for emerging nonvolatile memory technologies. Over the last few decades, several materials have been explored for memory applications. There is an urgent need for material innovations for developing emerging data storage technologies, driven by the inherent limitations of current computational systems, e.g., the "memory wall," and high power consumption. The "memory wall" problem of the current von-Neumann architecture is that the time to move and store data is orders of magnitude slower than the computation speed. The computational architecture includes several types of memories, such as the static random-access memory (SRAM), with a response time of ~1 ns and virtually unlimited endurance but with low areal density due to the six-transistor configuration, or the dynamic random-access memory (DRAM), with a response time of ~10 ns. The areal density of DRAM is higher than SRAM because of its one-transistor one-capacitor configuration. Storage class memory (SCM) is a new level in the hierarchy, being between main memory (DRAM) and storage memory and it is non-volatile. Although the response times of DRAM and SRAM are much higher than SCM, they are volatile and so do not retain information when powered down. The higher density, lower cost, and higher-speed SCM can function as a non-volatile DRAM.[1]

The starting point for the development of non-volatile memory (NVM) technology is to find a suitable material that shows two or more stable states of physical properties that can be switchable by external electrical, mechanical, thermal, magnetic, or other stimuli. Several switching mechanisms have been investigated significantly over the last two decades in various two-terminal devices, such as resistive random-access memory (RRAM), ferroelectric tunnel junction (FTJ), phase-change RAM (PCRAM), and spin-transfer torque-based magnetic random-access memory (STT-MRAM), with the promise of scalable, low-power operating, high-density non-volatile memory (NVM) solutions. Various material systems, ranging from metallic binary oxides, complex oxides, chalcogenides, nitrides, etc., mostly in thin-film form, have been explored for these devices. Initially, crossbar arrays have been proposed and experimentally tried for the fabrication of the high-density memory architecture. However, the crosstalk between the neighboring memory units during the write/read operation results in unwanted switching in these devices. To overcome this issue, one transistor–one resistor (1T–1R) and one selector–one resistor (1S–1R) structures have been investigated. For selector purposes, the ovonic threshold switching (OTS) or metal–insulator transition (MIT) characteristics of several chalcogenides and oxide materials have been explored.[2]

The growth of multilayer complex heterostructures is typically required for these memory devices, which is the foundation for the fabrication process. Mostly sputtering, chemical vapor deposition and atomic layer deposition (ALD) techniques have been used to grow these materials. Among these processes, ALD enables low temperature, uniform, large-area deposition of various materials. Controlling the thickness of the films down to a monolayer over the large-scale sample is possible with ALD. Integration of these devices with the complementary metal-oxide-semiconductor (CMOS) process is another key step.

A further critical consideration wherein the development of non-volatile memory can play a key role relates to the emergence of the Artificial Intelligence (AI) era, where a large amount of data needs to be processed to bring automation in smart systems in various fields, such as healthcare, automobile, manufacturing industry, advertising industry, and security applications. To keep pace with the ever-growing need for AI systems, fast access to vast amounts of data with low operation energy is required. However, the current computation architecture is not capable to cope with these needs due to the "memory wall" problem. Introducing high-speed, low-power, non-volatile memory closer to the process part would be a potential solution to tackle this issue. A new computing paradigm—beyond CMOS, such as in-memory and neuromorphic computing—would be a better approach to tackle this issue. The key advantage of using neuromorphic computing is its parallel data processing capability that enables adaptive learning, similar to the human brain, and hence can perform complex tasks, such as pattern recognition and real-time data analysis.

Among all new memory technologies, RRAM devices with multilevel states have been investigated for memory, neuromorphic computing, and synaptic device applications. In a typical RRAM device or memristor, resistive switching is accomplished by the electromigration of ions and defects, such as oxygen vacancies. The resistance levels of these devices depend upon the past and present applied external stimuli. It has been demonstrated that one can mimic the functionality of the biological synapses with such multilevel resistive states with spike-time-dependent plasticity and long-term synaptic potentiation/depression. Formulation and manipulation of defects in the material enables resistive switching behavior. In complex oxide systems, the formation of oxygen vacancies can disrupt the charge, spin, and orbital ordering of the materials and hence can modulate the physical properties, including resistive switching. Recently, the role of oxygen vacancies in the stabilization of the ferroelectric phase in ultrathin films of Zr-doped HfO_2 systems has also been demonstrated. In fact, one can achieve binary or even multiple resistive states by sandwiching such ultrathin films as a tunnel barrier between two metallic electrodes.

Changing the phase of the material from crystalline to amorphous or vice versa via electric current is another approach to achieve the nonvolatility in the resistive states of the devices. Such phase change materials (PCM) have also been well explored for non-volatile memory as well as neuromorphic computing applications. The fundamental idea underlying data storage in phase-change memory is the principle of change in resistance rather than charge. The typical phase change materials are chalcogenides, such as GeTe, GeS, GeSe, SiTe, Sb_2Te_3, and $Ge_2Sb_2Te_5$. Germanium Antimony Tellurium (GST) (usually $Ge_2Sb_2Te_5$ and $GeSb_2Te_4$) is a highly explored material for phase-change memory as it offers revolutionary properties that enable non-volatile storage. Electrical heating can cause this material to change "phases" between crystalline (c) and amorphous (a) states, which is employed for efficient data storage. Here, the crystalline phase represents the low resistance state (LRS) or ON state, and the amorphous phase represents the high resistance state (HRS) or OFF state. Besides the data storage application, phase change materials are also used as a selector in MRAM and PCRAM applications. For selector applications, the volatile ovonic threshold switching (OTS) characteristics of these materials are being used. Normally, under the electric field, the amorphous phase of these materials turns on/off the electric current, without notable phase transition. Although the PCRAM and RRAM have been well-explored, the device-to-device variability in these technologies is unfavorable for reliable data storage applications.

Among the new memory technologies, the spin-transfer, torque-based MRAM technology has emerged as a promising alternative non-volatile memory solution due to its low-error rate. However, the low endurance, difficulty in switching well below 10 ns, and high switching current issues are challenging aspects to be addressed before making STT-MRAM a standalone memory technology. Changing the device structure from a two-terminal STT to a three-terminal Spin–Orbit Torque (SOT) device resolves these issues, as unlike in STT-MRAM, read and write current paths are different in the SOT-MRAM device, and the current density to accomplish the SOT effect could be significantly lower than that of the STT effect. Additionally, the ultrafast switching of perpendicular magnetization is possible with the in-plane spin polarization carrying spin-currents in the SOT layer. Typically, the heavy metals (HMs) that show a spin Hall effect (SHE), such as Pt, W, Ta, and Hf, are being used as a SOT layer in SOT-MRAM devices. The charge-to-spin conversion efficiency, known as the spin-Hall angle (SHA), of the SOT material, is the key to realizing the energy-efficient SOT-MRAM devices. In addition to heavy metals, several other material systems, such as topological insulators, complex oxides, etc. have been explored for higher SHA. Beside the bulk SHE in the heavy metal and the interfacial spin–orbit coupling effect play a role in the generation of spin current in FM/HM bilayer structures. On the one hand, the magnitude of SHE decreases with decreasing the thickness of the HM below a certain thickness determined by the spin diffusion length; on the other hand, it increases due to the dominant interfacial spin–orbit coupling with decreasing HM thickness. Therefore, an optimal thickness of HM is required to achieve a higher SHE at the FM/HM interface in SOT-MRAM devices.

Magnetic tunnel junctions with perpendicular magnetic anisotropy (p-MTJ) are now primarily being used in MRAM technology for high density, low-power consuming non-volatile memory applications. Fabrication of the commercial memory products needs CMOS compatibility of the MRAM devices, especially in terms of the thermal budget for the back-end-of-line integration. Typically, HMs are being used as a seed or SOT layer in the electric current-driven STT and SOT MRAM devices. Among HMs, only Mo and beta-W can maintain the PMA in HM/CoFeB/MgO-based p-MTJ devices at 400 °C or higher temperature. Although STT and SOT have proven to be elegant ways of switching the MRAM devices, the higher power consumption due to the Joule heating effect caused

by the passage of electric current is still a major concern. To overcome this problem, electric field control of magnetism is found to be an alternative route to manipulate the resistance state of MRAM devices.

In this Special Issue, we compile a series of articles on emerging memory technologies, particularly on RRAM, PCRAM, and MRAM. These articles provide an overview of the ongoing research in these fields and constitute the guidelines for the development of novel materials and devices.

RRAM is categorized into two types based on the nature of the ions involved in the switching mechanism: oxygen vacancy-RAM (OxRAM) and conductive bridge RAM (CBRAM). To create a conductive bridge, CBRAM uses ionization of metal electrodes (for example, Ni, Ag, and Cu) unlike OxRAM where ionization of oxygen is taking place. This way, CBRAM has faster switching speed. However, CBRAM often suffers from switching instability. Thus, for improving switching stability, the insertion of a metal layer between the electrode and switching layer was discovered as the most feasible approach. Simanjuntak *et al.*[3] found that inserting Cr and Ti films below the Ag electrode creates ternary oxides, $CrZnO_x$ and $TiZnO_y$, that act as a barrier layer to restrict Ag species drift during switching and facilitate stable switching.

In addition to standard metal oxides (TiO_2, HfO_2, and Al_2O_3) with MIM structures, for RRAM applications, Lei *et al.*[4] created a unique stable hybrid Hf-based hydroquinone (Hf-HQ) film deposited using molecular layer deposition (MLD) for flexible hybrid RRAM devices. The resistive switching (RS) behavior of the hybrid device (Pt/Hf-HQ/Al_2O_3/TiN) was designed, and properties such as retention and durability have been thoroughly investigated. Unlike halide perovskite RRAM devices, which have a high ON/OFF ratio, these hybrid memory units offer electroforming-free RS behavior, with improved stability and repeatability.

In a similar manner, aside from standard oxide research, attention has shifted to SiO_2 and its associated suboxide (SiO_x), which provides several advantages in terms of processing, cost, manufacture, and compatibility with CMOS. It was proposed that the formation of voids, low-density areas, and/or redistribution of O create a columnar structure, which helps in the formation of conductive filaments (CFs). To realize the full potential of these devices, it is important to exploit the formation of column boundaries (CB). These boundaries are crucial for achieving good resistance switching characteristics in SiO_x (ReRAM) devices. Patel *et al.*[5] studied the formation and structure of columnar boundaries that arise due to SiO_x layers being templated by metal surface roughness. Here metal/SiO_x/metal stacks are created by sputter deposition, and to understand the nature of columnar structures in SiO_x and the interaction between metal electrodes and the SiO_x layer, high-resolution TEM (HRTEM), electron energy-loss spectroscopy (EELS), energy-dispersive x-ray spectroscopy (EDX), and density functional theory (DFT) modeling are used.

Another research upgrade for RRAM was to considerably increase its reliability and to fabricate sneak current-free crossbar array architecture (CAA) memory devices via controlling oxygen vacancies. Kim *et al.*[6] presented a simple Atomic Layer Deposition (ALD) technique for a novel RS material for RRAM devices: fluorine-doped titania (F: TiO_2). The Pt/F: TiO_2/Pt device demonstrated formingless bipolar RS and self-rectifying behavior via fluorine anion migration, dramatically lowering sneak current in crossbar array RRAM. They verified this experimentally with XPS, FT-IR, and Hall measurements in the presence of F anion passivated oxygen vacancies in the film.

Cox *et al.*[7] also took a step forward toward better designing of ReRAM devices by providing an elusive key to understanding and addressing the problem of ReRAM device reliability. They revealed that the device interacts with the ambient environmental conditions while in operation. Their findings demonstrated not just factual proof of moisture injection into devices, but also a direct link between the amount of oxygen injected from ambient moisture and the microstructure of the oxide layer. The authors developed an efficient secondary ion mass spectrometry (SIMS) *in situ* normalization approach for monitoring chemical changes between electrodes and switching layers. They demonstrated it for SiO_x devices, but the method is widely relevant to any device with a rough surface that can host oxygen exchange.

Furthermore, resistive switching (RS) emerged as an attractive alternative also for neuromorphic computing. Several materials, including titanium oxide, hafnium dioxide, tantalum oxide, and aluminum oxide, have already been proposed for the RS layer. Most of the devices are conductive filament (CF) memristors. However, CF-type memristors have certain drawbacks in neuromorphic computing due to their natural abrupt switching nature. Thus, for compatibility with a thin-film transistor (TFT), Pereira *et al.*[8] fabricated a a-Indium-gallium-zinc-oxide (a-IGZO) based memristor, such as Mo/a- IGZO/Ti/Mo, for a reduced oxygen concentration. These findings reveal the impact of RS device compatibility with thin-film transistors (TFT).

Proceeding further, in synaptic characteristics of memristor devices, analog and digital memristors have various circuit functionalities (operational speed, current level, voltage range, etc.). The research done by Simanjuntak *et al.*[9] gave not only an insight into establishing an equivalent synaptic response for dictating an analog and digital response of memristor devices but also provided a way for realizing convertible digital-analog memristors, which might open new possibilities in electronic circuits and systems. Their experimental data revealed that the maximum working current level of memristor devices controls their synaptic response.

De Araujo *et al.*[10] proposed a novel resistive switching device, i.e., the correlated electron-based RAM (CeRAM), to prevent the unpredictability of resistive memory produced by the stochastic filamentary activity. CeRAM is a unique resistive switching technology that may be utilized to allow analog neuromorphic computing and increased memory density, or as an extra CMOS process modification.

Furthermore, the electroforming process is followed by a significant oxygen release and temperature effects that damage the device's nanostructure and decouple the active zone from the rest of the device, making it difficult to integrate these systems in numerous device topologies. Thus, for better development of non-volatile memory and neuromorphic computing, Acevedo *et al.*[11] provide many methods for reducing damage while preserving the device's structural integrity, chemistry, and multi-mem behavior, which are required for memory or neuromorphic computer hardware. They produced oxidized $La_{1/2}Sr_{1/2}Mn_{1/2}Co_{1/2}\ O_{3-x}$ (LSCMO) thin films on

conducting Nb:$SrTiO_3$ (NSTO) substrates with out-of-plane (001) and (110) orientations using pulsed laser deposition (PLD), and conducted a thorough investigation of the electrical behavior of multi-mem NSTO/LSMCO/Pt devices, with varying crystallinities, out-of-plane orientation, and stimulation, which display a robust memristive behavior.

Besides RRAM, introducing an ultrathin ferroelectric film as a tunnel barrier between two metallic electrode layers is another way to achieve a large resistive switching in the devices. Although the tunnel electroresistance effect has been demonstrated with ultrathin perovskite-based ferroelectric tunnel junctions for more than 15 years, technological interest in this field has increased recently because of the discovery of ferroelectricity in CMOS process-friendly material, doped HfO_2 films. The tunnel electroresistance effect has also been demonstrated in ultrathin doped HfO_2 ferroelectric tunnel barriers. However, the electroresistance varies from device to device due to the presence of the grain boundaries in these ferroelectric films that provide conducting paths for the charge motions. To overcome this problem, Long *et al.*[12] used an ultrathin (~1 nm) $SrTiO_3$ film as a capping layer on a $Hf_{0.5}Zr_{0.5}O_2$ (HZO) film epitaxially grown on $SrTiO_3$ and $GdScO_3$ substrates, that led to more robust ferroelectric tunnel junctions with large endurance and higher yield.

Zhou *et al.*[13] used the Z-scan technique to explore the phase shift of GST material under a terahertz quantum cascade laser (QCL) emitting at around 2.5 THz. To evaluate the phase transition of GST, TEM, and X-ray diffraction (XRD) characterization were performed. Numerical simulations based on 3D finite elements and electromagnetic heating were performed to compute the temperature and transmission changes, in which both simulation and experiment verified that the a-GST film can be phase changed to c-GST under 1.5 mW terahertz power.

To extend the capacity of PCRAM, Sun *et al.*[14] focused on doping Sb_2Te_3 with Sc forming $Sc_{0.2}Sb_{1.8}Te_3$ (SST) that increases the SET speed up to ~0.7 ns. However, for embedded memory, thermal stability is not suitable for SST. Further indium-doped GST alloys were shown to have high thermal stability. They presented a thorough theoretical work on InTe based on *ab initio* simulations, with calculations performed using density functional theory (DFT) based on molecular dynamics. The time step was set to 2 fs. The electronic structure computations and chemical bonding investigations were performed utilizing the Vienna *Ab initio* Simulation Package (VASP) code and the Local Orbital Basis Suite. This study will serve as a springboard for further research on phase-change devices that use both heat and mechanical-induced transitions.

In addition to this, the use of GST in nanophotonic elements was experimentally demonstrated by Lazarenko *et al.*[15] Their work focuses on a numerical and experimental investigation of the attenuation coefficient dependency for the a-GST and c-GST lengths (100 nm–20 μm), on the silicon nitride rib waveguide at the telecom wavelength of 1550 nm, as well as the experimental identification of the GST cell range with dominant light scattering. The transmission spectra for the two constructed O-ring resonators (ORRs) before and after a-GST/SiO_2 and c-GST/SiO_2 synthesis were measured. They found that the most energy-efficient devices in this situation should have GST cell lengths of more than 2 μm. As a result, compromises must be made throughout the creation of nanophotonic devices, and each task must be approached differently.

Furthermore, a two-terminal GST ($Ge_2Sb_2Te_5$) based memristive device was built to implement synaptic functions by Go *et al.*[16] In their work, when using a memristive device with just nanopillars deposited, this newly constructed artificial synapse exhibits paired-pulse facilitation/depression (PPF/PPD) behavior as well as multistate and rapid long-term potentiation/depression LTP/LTD in a GST-based device, with more conductance states than previously described GST-based synapses. They demonstrated cell characteristics and electro-thermal simulations for RIMS (Rapid-operating-time, Intermediate bias-range, Multiple-states, Several-synaptic-functions) synapse utilizing this memristive device. As a result of this work, it will be possible to analyze both temporal and geographical data more effectively.

Although phase change materials have been studied significantly, the ovonic threshold switching (OTS) mechanism in these materials is not yet fully understood. The OTS characteristics of these materials are being used as a selector in several memory technologies, including MRAM and PCRAM. In view of this, Gu *et al.*[17] used first-principle calculations to provide an in-depth understanding of the structural and electronic property of a simple OTS material, the amorphous (a-) SiTe. Their study revealed how two identical materials, GeTe and GeSe, behave differently as GeTe is an ovonic memory switching (OMS) material rather than OTS material, unlike GeSe.

In STT-MRAM, the reduction of the barrier height (commonly known as delta) between two stable magnetization states leads to a lowering of the switching current but at the cost of poor retention. Therefore, finding the right balance is always challenging. To address this issue, recently the concept of double magnetic tunnel junctions (DMTJ) has been proposed as an alternative for energy-efficient STT switching, where the storage layer is sandwiched between two tunnel barriers with a hard bottom reference layer and a hard top polarizer layer. Interestingly, this device structure not only decreases the switching current but also enhances the data retention by increasing the PMA of the storage layer. However, getting sufficient PMA on the top polarizer, dealing with stray magnetic fields with two high PMA layers (top polarizer and bottom reference), and the difficulty to fabricate such DMTJ devices remain challenging. Hazen *et al.*[18] have solved these issues by introducing a simpler and thinner assisting layer, instead of the thick top polarizer layer in DMTJ, with the MgO capping layer. They have found the figure of merit defined by the ratio of thermal stability (delta) vs critical current, in their DMTJ devices to be nearly double that of single MTJ devices with a diameter 80–100 nm.

CMOS integration is another challenge in MRAM technology development. For STT devices and even for SOT devices, Ta has been widely used as a seed layer for PMA as well as a spin current source layer for SOT-MRAM. However, Ta has poor thermal stability at a temperature above 350 °C, and therefore its integration into the CMOS process is difficult. Although beta W is a superior material for SOT application in terms of efficiency and thermal stability, its growth is a challenging task. Therefore, a novel material that can replace beta W is needed for the CMOS integration of SOT-based MRAM devices. In view of this, Ranjan *et al.*[19] demonstrated a thermally stable PMA up to 425 °C in rhenium (Re) with an SHA of 0.065 ± 0.003 and SOT switching current density of around 1.36×10^{11} A/m^2. Besides the larger SHA, lower resistivity is sought

to reduce the Joule heating effect during the writing. Interestingly, the resistivity of the Re is nearly half compared to Ta and beta-W. Further exploration of the new materials may provide even better SOT material.

The interfacial spin–orbit coupling at the FM/HM interface has been explored significantly for achieving the large SHE. However, the role of the interface between the HM and substrate was overlooked. Some theoretical works have recently suggested a significant contribution of the insulator/HM interface to the SOT effect, particularly when the thickness of the HM is less than the spin diffusion length. The common substrates that are being used for SOT-MRAM are insulating materials such as amorphous SiO_x, single-crystalline $SrTiO_3$, MgO, etc., where the HM is sitting on the substrate. Therefore, besides the FM/HM interface, the interfacial spin–orbit coupling at HM/insulating substrate interface would be another approach to tuning the SOT effect. Recently, Choi *et al.*[20] have done such experiments with the Pt/substrate interface by investigating the dependence of Pt thickness on the SOT effect, where Co/Pt bilayers were grown on amorphous SiO_x and single-crystalline $SrTiO_3$ and $LaAlO_3$ substrates. Unlike the conventional bulk SHE, weaker thickness dependence of the SHE was found in the samples grown on single crystalline substrates, which suggests that the interfacial spin–orbit coupling at the HM/substrate interface can be exploited to develop efficient SOT based devices.

Fabricating a three-terminal SOT-MRAM device is challenging, particularly avoiding the side redeposition during the etching process that leads to the shutting effect in MTJ. Ren *et al.*[21] have addressed this issue by carefully optimizing the ion beam etching angle and time along with other device fabrication processes in three-terminal in-plane SOT devices. Besides this, with the insertion of thin Hf interlayers into the heterostructure, they have demonstrated the enhancement in thermal stability and reduction in the switching current density of the fabricated devices. As per the micromagnetic simulation, the insertion of thin Hf increases the magnetic anisotropy at one interface, while decreasing the strength of the Dzyaloshinskii–Moriya interaction on another interface, thereby decreasing the switching current density while enhancing the thermal stability.

In order to make energy-efficient spintronic devices by eliminating the Joule heating effect, the magnetoelectric coupling route has been explored with several systems for the last two decades. Wu and MacManus-Driscoll[22] have provided an overview of the recent developments in several magnetoelectric nanocomposite systems with future perspectives for magnetoelectric RAM (MERAM). They have covered the topic from basic mechanisms to materials and applications. Among several nanocomposite systems, the 3-1 type oxide composite films are promising candidates for low-power spintronics. They set out the challenges and directions for achieving high-performance MTJ-based MERAM from 3-1 composite systems and explained how and why the use of self-assembled triple 3-1 composite systems can enable a large converse magnetoelectric effect at room temperature without the application of magnetic field biasing.

Overall, this Special Issue covers the recent advances in RRAM, PCRAM, MRAM, and MERAM. The authors have demonstrated several novel ways of tackling the materials challenges for the development of emerging memory technologies and neuromorphic computing systems. We hope the contents of this issue will provide several new directions for materials research on non-volatile memory.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

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