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Out-of-plane interface dipoles and anti-hysteresis in graphene-strontium titanate hybrid transistor

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The out-of-plane electric polarization at the surface of $SrTiO_3$ (STO), an archetypal perovskite oxide, may stabilize new electronic states and/or host novel device functionality. This is particularly significant in proximity to atomically thin membranes, such as graphene, although a quantitative understanding of the polarization across graphene–STO interface remains experimentally elusive. Here, we report direct observation and measurement of a large intrinsic out-of-plane polarization at the interface of single-layer graphene and TiO_2-terminated STO (100) crystal. Using a unique temperature dependence of anti-hysteretic gate-transfer characteristics in dual-gated graphene-on-STO field-effect transistors, we estimate the polarization to be as large as ≈12 μC cm^{-2}, which is also supported by the density functional theory calculations and low-frequency noise measurements. The anti-hysteretic transfer characteristics is quantitatively shown to arise from an interplay of band bending at the STO surface and electrostatic potential due to interface polarization, which may be a generic feature in hybrid electronic devices from two-dimensional materials and perovskite oxides.

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INTRODUCTION

The rich and diverse phenomenology of perovskite oxides,[1–4] which includes electronic and structural phase transitions, colossal magnetoresistance to ferroelectricity and superconductivity, holds great promise for new concepts in device technology and material engineering. The crystal structure of $SrTiO_3$ (STO), a crucial member of the perovskite oxide family that forms the building block of complex oxide heterostructures,[5,6] is centrosymmetric and hence a paraelectric in the bulk. STO approaches an *incipient* ferroelectric state at low temperatures, but quantum fluctuations prohibit a long-range ferroelectric order to develop.[7] The quest for stabilizing ferroelectricity in STO has a long history, and it is now known that chemical doping,[8,9] nanostructuring,[10] manipulation of oxygen stoichiometry[11,12] or application of inhomogeneous deformation (flexoelectricity)[13] can cause spontaneous electric polarization in the bulk. However, the surface of a STO (100) crystal, in both TiO_2 and SrO terminations, can intrinsically host out-of-plane dipole moments due to inversion symmetry breaking at surface, where the Ti or the Sr ions are vertically displaced away from the corresponding oxygen planes. Although surface reconstruction in STO has been established with multiple spectroscopic[14–16] and surface topography[16,17] probes, a direct evaluation of the resulting electric polarization has been difficult. Experiments with piezoresponse force microscopy[17,18] and flexoelectric response[13] yield surface polarization of ~0.5–10 μC cm^{-2}, which is strongly influenced by local oxygen stoichiometry,[19,20] grain boundaries[20,21] or surface strain.[20] Apart from the natural relevance to in-built ferroelectricity, the importance of surface electrostatics in STO is paramount because it can directly impact charge transfer superconductivity,[6] oxide heterostructures[5,22,23] and two-dimensional (2D) electronics as active substrates.[24–26]

Hybrid field-effect transistors (FETs) from atomic membranes of layered solids such as graphene and molybdenum disulfide (MoS_2) on STO substrate aim to combine the high crystallinity and atomically clean interface to spectacular bulk dielectric properties of STO (dielectric constant $>10^4$ at low temperatures). It is however unclear if the out-of-plane polarization at the STO surface is stable in the presence of graphene, for example, against possible atomic reorganization and screening. Recent observations of (anti-)hysteretic gate-transfer characteristics at slow sweep rates in graphene FETs fabricated on STO(100) substrate[25,26] are attributed to "ferroelectric-like" electric polarization at the STO surface, which indeed bear close resemblance to transfer characteristics of graphene FET on ferroelectric substrates.[27–31] While this has been described as the effect of gate voltage-dependent dynamic trapping and detrapping of charge at the channel–substrate interface, identifying the microscopic origin of such interface states, and its connection to electric polarization at the surface, remains an outstanding experimental challenge.

Here we have probed the interface of graphene and STO by constructing dual-gated graphene-on-STO FETs, which allow direct calibration of the graphene–STO interface against the interface between graphene and hexagonal boron nitride (hBN), a conventional trap-free[32] well-characterized dielectric for graphene devices. While the transfer characteristics using hBN top gate shows no hysteresis, that using STO back gate becomes strongly anti-hysteretic at low temperature (≲200 K), which is quantitatively associated with in-built electric polarization at the graphene–STO

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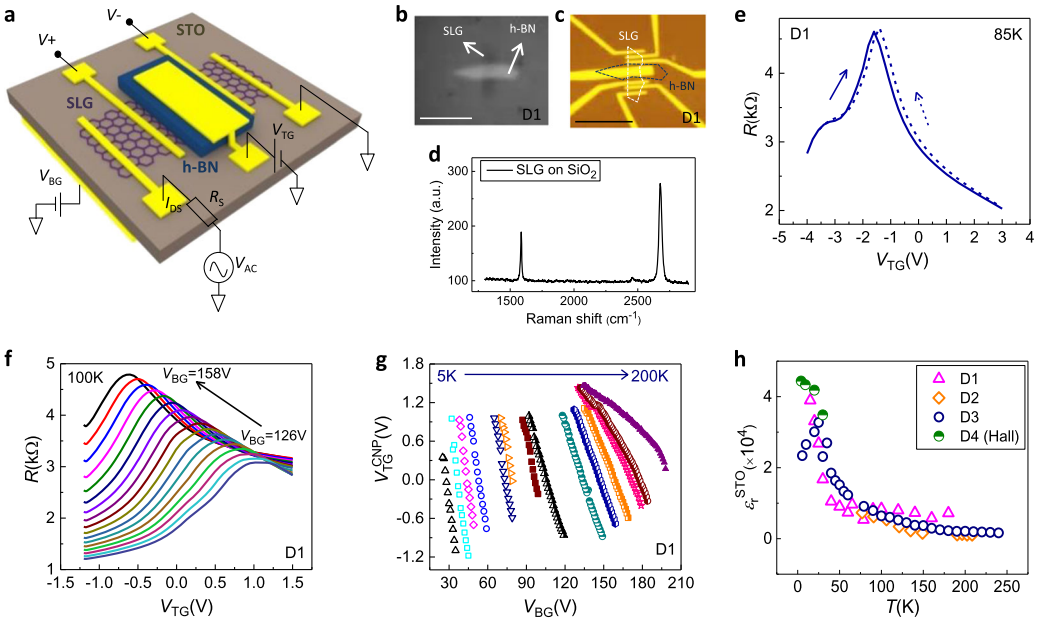


Fig. 1 Structure and electrical characterization of graphene–STO hybrid. **a** Schematic of a dual-gated single-layer graphene (SLG) transistor on STO substrate with STO and hBN as back and top gate dielectrics, respectively, together with the circuit diagram for electrical transport measurement. Optical microscope images of SLG-hBN stack **b** on the transfer tape before transferring on STO and **c** after fabricating dual-gated transistor on STO. Scale bars in both (**b**, **c**) are 25 μm. **d** Raman spectroscopy of graphene layer used to make the dual-gated transistor showing single-layer characteristics. **e** Transfer characteristics with respect to top gate voltage (V_{TG}) at 85 K. The solid and dashed lines depict the resistance of SLG channel with forward and reverse sweeps of top gate voltage respectively. **f** Transfer characteristics of device D1 with respect to V_{TG} at 100 K showing the shift of charge neutrality points (CNP) at different fixed V_{BG} from 126 V to 158 V. **g** The locus of the charge neutrality points (V_{TG}^{CNP}) with varying V_{BG} at different temperatures from 5 K to 200 K. **h** The dielectric constant of STO (ε_r^{STO}) with varying temperatures estimated from three different devices D1, D2 and D3. For device D4, ε_r^{STO} was measured from Hall measurement at low temperatures

interface. From detailed temperature dependence of the anti-hysteresis, and independently from noise measurements, we estimate out-of-plane polarization magnitude $P \sim 12\,\mu C\,cm^{-2}$, which also agrees with that obtained from density functional theory (DFT) calculations within a factor of two. We have also developed a phenomenological model for anti-hysteretic transfer characteristics using band reconstruction and electrostatic potential at the STO surface, which may be applicable to graphene FETs on other polarized substrates as well.

RESULTS AND DISCUSSION

Device fabrication and electrical measurement

The transport and 1/*f* noise measurements were carried out in a dual-gated single-layer graphene (SLG) field-effect transistor with hBN as the top gate and STO as the back gate dielectric. The schematic of a typical dual-gated SLG transistor with the electrical layout is shown in Fig. 1a. The TiO_2 surface termination of the 0.5 mm thick STO (100) substrate (from CrysTec GmbH) was achieved through chemical processes and annealing (Fig. S1 in Supplementary Information). The SLG and hBN flakes were exfoliated on SiO_2/Si^{++} substrates, and subsequently transferred onto the TiO_2−terminated surface of STO through van der Waals epitaxy[33,34] (see Methods for more details). The layer number of graphene was verified by Raman spectroscopy as shown in Fig. 1d. The absence of D peak at 1350 cm^{-1} in the Raman spectrum confirms a defect-free graphene channel. The metal contacts were patterned by e-beam lithography followed by thermal deposition of 5/50 nm of chromium/gold. The optical microscope image of the SLG/hBN heterostructure before transferring onto STO, and the dual-gated transistor after depositing contact pads, are shown in Fig. 1b, c, respectively. All measurements of resistance and noise were carried out using low-frequency AC technique[34–40] in four probe geometry under high vacuum condition (~10^{-5} torr). The carrier mobility of the graphene channel, similar for both electrons and holes, was found to be ~2000 $cm^2\,Vs^{-1}$ at 140 K which increases to ~7300 $cm^2\,Vs^{-1}$ at 10 K, in agreement with recent experimental report[24] (Fig. S2 in the Supplementary Information). The resistivity of the graphene channel increases with increasing temperature upto ~60 K beyond which it either saturates or decreases marginally (Fig. S3 in the Supplementary Information).

Measurement of dielectric constant of STO

The resistance of the dual-gated SLG transistor with varying top gate voltage (V_{TG}) shows conventional bell curve with a charge neutrality point (CNP) or Dirac point at $V_{TG} \approx -1.6$ V (Fig. 1e). The hysteresis in the top gate sweep is nearly negligible, as expected from trap-free interface of SLG and hBN.[32,41] The dual-gated geometry allows a direct measurement of the dielectric constant of STO (ε_r^{STO}) from the locus of the CNP in the (V_{TG}, V_{BG}) space, which balances the STO back gate capacitance with the known capacitance of hBN top gate. In Fig. 1f, the resistance (at $T = 100$ K) of the dual-gated SLG transistor is shown while sweeping V_{TG} at different fixed back gate voltages (V_{BG}). The CNP (V_{TG}^{CNP}) shifts expectedly to the left with increasing V_{BG}.[42,43] Plotting V_{TG}^{CNP} vs. V_{BG} (Fig. 1g) gives a straight line which can be fitted with the equation,

$$V_{TG}^{CNP} = -\frac{C_B}{C_T}V_{BG} - \frac{n_0 e}{C_T}, \quad (1)$$

where C_B and C_T are the capacitances of the back gate with STO as dielectric and the top gate with hBN as dielectric, respectively, n_0 is the intrinsic carrier density in graphene and e is the electronic charge. Since C_T ($=2.7 \times 10^{-3}$ F m^{-2}) is known from the thickness of hBN (≈13 nm, measured from atomic force microscopy), we obtain the dielectric constant $\varepsilon_r^{STO} = C_B d_{STO}/\varepsilon_0$ (d_{STO} being the

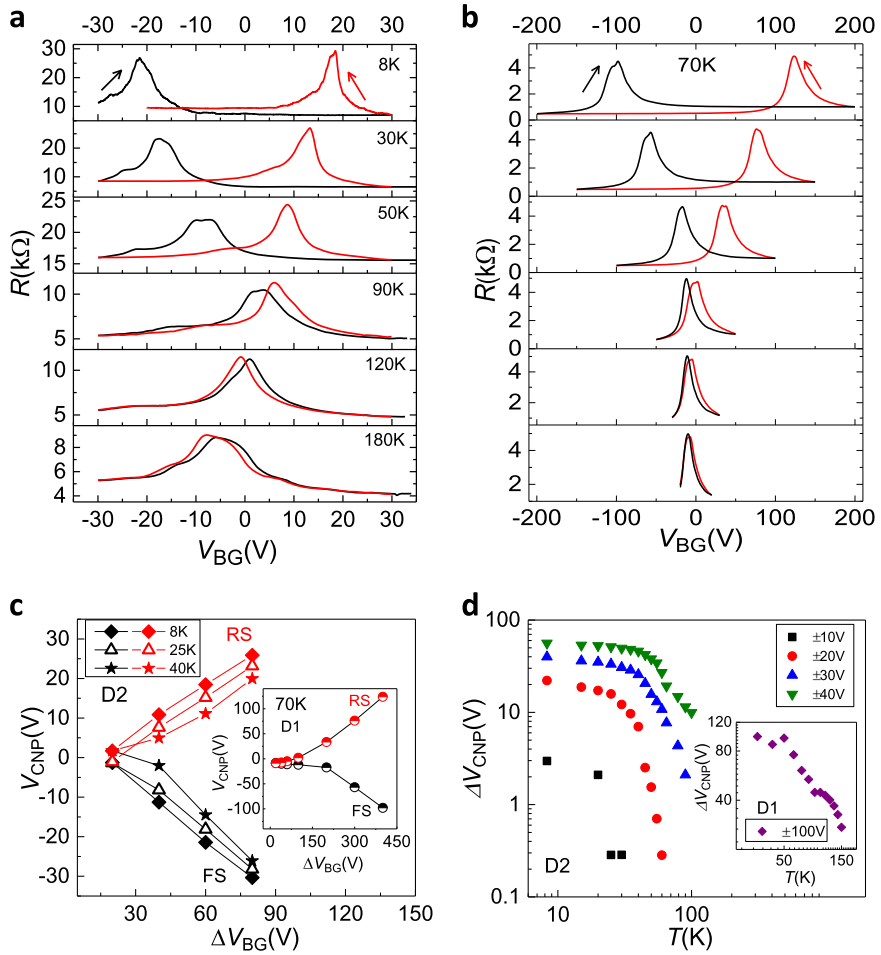


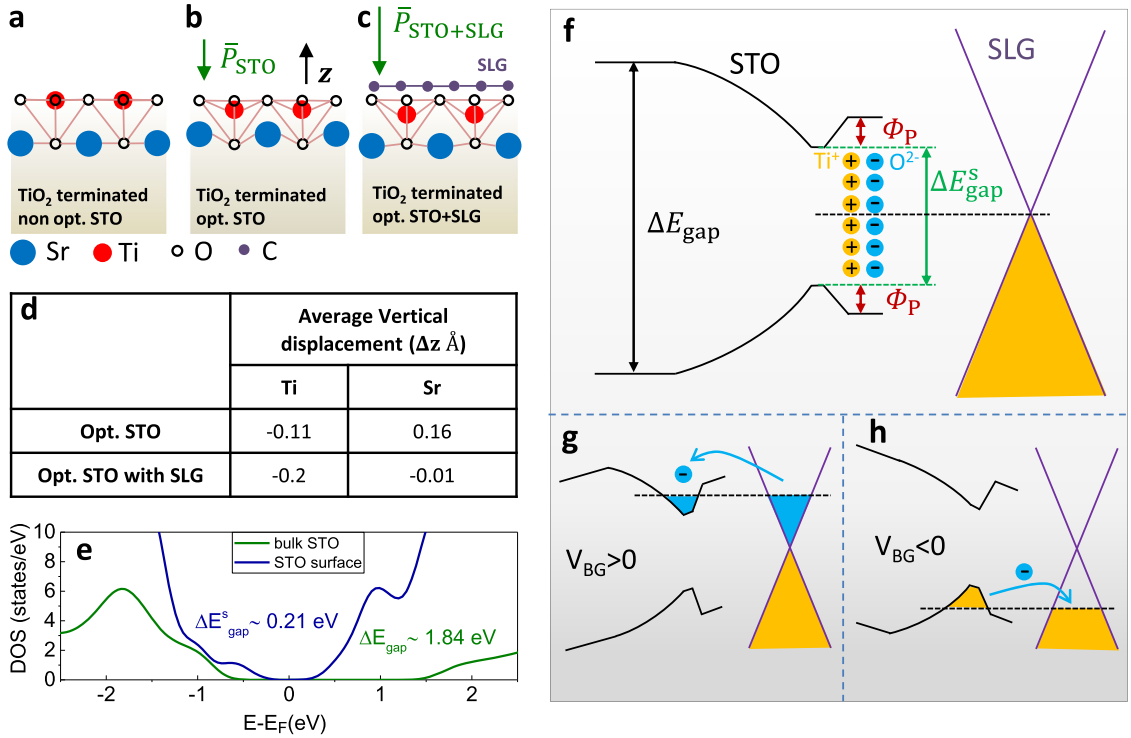
Fig. 2 Temperature and gate voltage range-dependent transfer characteristics. **a** Anti-hysteresis in transfer characteristics with respect to back gate voltage (V_{BG}) at different temperatures showing the decrease in anti-hysteresis with increasing temperature. **b** Anti-hysteresis in transfer characteristics with respect to V_{BG} at 70 K showing the decrease in anti-hysteresis with decreasing sweep range of V_{BG}. The arrows indicate the direction of V_{BG} sweep in (**a**, **b**). **c** The CNP of forward and reverse sweep directions as a function of overall sweep range of V_{BG} (ΔV_{BG}) at different temperatures for devices D2 and D1 (inset). **d** The difference in CNP of forward and reverse sweep directions of V_{BG} as a function of temperature at different sweep ranges for devices D2 and D1 (inset)

thickness of STO and ε_0 the vacuum permittivity) (also see Fig. S4 in the Supplementary Information). The magnitude of ε_r^{STO}, measured at different temperatures, as shown in Fig. 1h, are in agreement with previous reports[7,44–47] and matches well with the value of ε_r^{STO} estimated from Hall measurement at low temperatures. This agreement confirms that both graphene–hBN and graphene–STO interfaces in our device are atomically clean, and free of undesired adsorbates and chemical species.

Anti-hysteretic transfer characteristics

Unlike the top gate, sweeping of the back gate voltage V_{BG} in forward and reverse directions led to strong anti-hysteresis in the transfer characteristics. The extent of anti-hysteresis depends on both temperature and sweep range of V_{BG}. As shown in Fig. 2a, the anti-hysteresis decreases with increasing temperature and vanishes at the temperature range of 150–180 K whereas, it decreases with decreasing sweep range (Fig. 2b). See Fig. S5 in the Supplementary Information for results from different devices. Hysteretic transfer characteristics in graphene FET[48] on SiO_2 and other substrates[49–51] are commonly attributed to slow charge transfer in the presence of impurity states and absorbed water molecules. Although our experiment was performed under high vacuum condition, and the collapse of the anti-hysteretic transfer characteristics is observed at significantly low temperature (~180 K), the possibility of physi/chemisorption of OH^- and H^+ on individual atomic site[52] cannot be ruled out. However, the independence of the anti-hysteretic behaviour to the ramp rate in V_{BG} (Fig. S6 in the Supplementary Information) suggests a fundamentally different physical mechanism in our case.

The similarity of the transfer characteristics to that observed in the earlier studies of graphene transistors on STO substrate[25,26] and also in the single/multilayer graphene on ferroelectric substrates[27–31] strongly suggests that electric polarization at the surface gives rise to quantum confined states that trap, store and release charge from graphene periodically as V_{BG} is swept back and forth. The temperature and sweep range dependence provide crucial insight into the energy and confinement scale of these states. Figure 2c shows the CNPs (V_{CNP}) for varying sweep range ΔV_{BG} of the back gate. The symmetric positions of the CNPs about $V_{BG} = 0$ for the forward and reverse sweep directions eliminate oxygen vacancy-mediated anti-hysteretic transfer characteristics.[53] In all devices, the (anti-)hysteresis becomes undetectable for $\Delta V_{BG} \lesssim 20$ V, i.e., maximum $|V_{BG}| = 10$ V, which is insensitive to temperature (for $T \lesssim 200$ K). This indicates the energy of the localized trapping state (measured from the Dirac point), $E_t \sim E_F = \hbar v_F \sqrt{\pi C_B (V_{BG} - V_{CNP})/e} \sim 0.15$ eV, where v_F is the Fermi velocity. The inset of Fig. 2c confirms similar behaviour in a different device (D1).



d

	Average Vertical displacement (Δz Å)	
	Ti	Sr
Opt. STO	-0.11	0.16
Opt. STO with SLG	-0.2	-0.01

Fig. 3 Calculation of surface band renormalization and out-of-plane dipole moment at the graphene-STO interface. Schematic representation of atomic displacements in [001] (*z*-direction)-oriented TiO_2 terminated STO substrate under different conditions: **a** non-optimized, **b** optimized and **c** optimized with single-layer graphene (SLG) on top, as obtained in DFT calculations in the absence of any external electric field. The displacements of Ti atoms in the topmost TiO_2 layer and Sr atoms in the next SrO layer are shown explicitly. The surface polarizations of STO with and without graphene are denoted as $\bar{P}_{STO+SLG}$ and $\bar{P}_{STO}$, respectively. **d** Average vertical displacements (Δz) of Ti and Sr atoms at the surface of bare STO and STO with SLG calculated from DFT. **e** Density of states (DOS) of STO derived from DFT calculation showing the energy band gap of the surface (ΔE^s_{gap}) and bulk (ΔE_{gap}). **f** Energy band diagram of STO, SLG and their interface showing the trapped states with potential energy barrier, Φ_P appeared due to the presence of surface dipoles. The energy band diagram of the same at **g** $V_{BG} > 0$ and **h** $V_{BG} < 0$

The temperature dependence of the hysteresis (Fig. 2a) provides an estimate of the energy barrier to charge exchange between the substrate (STO) and graphene. To quantify this, we have plotted the difference in CNP (ΔV_{CNP}) for the forward and the reverse sweep directions in Fig. 2d as a function of temperature. For large sweep range $\Delta V_{BG} \gtrsim 100$ V, the anti-hysteresis in both D1 (inset) and D2 vanishes at $\approx 150 - 200$ K, suggesting a confinement energy scale $\Phi_P \simeq 0.02$ eV. At lower ΔV_{BG}, the hysteretic behaviour vanishes at lower *T*, possibly due to lower magnitude of effective polarization due to remnant domains.

The temperature-dependent anti-hysteretic behaviour can arise from two possible mechanisms. First, the structural transition to the tetragonal phase at low temperatures is known to form domains in the near-surface region, causing rumpling of the surface. This may potentially cause trap states of possibly both structural (domain) and electrostatic (dipole moments) origin. Although the tetragonal domains have been observed to persist up to ~105 K, the temperature dependence of resistance in our case seems to indicate the structural transition to be limited below ~60 K (Fig. S3 in supplementary information). The structural origin is further unlikely because the temperature scale of disappearance of the anti-hysteresis is found to be strongly sweep range dependent, being ~30 K and >200 K (extrapolated) for sweep ranges of ±10 and ±40 V, respectively, in the same device (D2, Fig. 2d). Second, an alternative origin of the hysteretic behaviour can be traced to electrostatically confined trap states arising due to formation of surface dipoles. Our DFT calculations at the graphene–STO interface indicate a possible origin of such surface dipole moments which can be attributed to the movement of Ti and Sr atoms at the surface of STO (Fig. 3a–d). The DFT calculation was performed to estimate the surface polarization, following the formalism adopted by Vanderbilt et al.[54] considering slab geometries of paraelectric/ferroelectric bulk compounds.

Two key aspects of the DFT calculations can be summarized as below (see Fig. S8 and associated discussions in the Supplementary Information for more details). First, the vertical displacement (Δz, shown in Fig. 3d) of Ti atoms in TiO_2 layer and Sr atoms in SrO layer result in a formation of out-of-plane dipole moment on the surface of STO. The surface dipole moment of bare STO ($\bar{P}_{STO} = -13.89\ \mu C\,cm^{-2}$, in agreement with ref. [54]) is significantly enhanced to $\bar{P}_{STO+SLG} = -34.90\ \mu C\,cm^{-2}$ in the presence of graphene. This result is obtained by assuming an epitaxial registration between graphene and STO (model-1). Calculations were also carried out considering model-2, where the lattice parameters of graphene were kept intact. See Supplementary Information section for details. The polarization ($\bar{P}_{STO+SLG}$) calculated for model-1 and model-2 turned out to be −34.9 and $-24\ \mu C\,cm^{-2}$, respectively. Thus, the polarization computed from model-2 geometry gives better agreement to experimental value and that obtained from simple phenomenological model. Such enhancement is presumably caused by the rumpling of the surface TiO_2 layer in the presence of graphene, as observed in DFT optimized structure. Second, the band gap at the STO surface $\Delta E^s_{gap} \sim 0.21$ eV is considerably smaller than the band gap of bulk STO $\Delta E_{gap} \sim 1.84$ eV (Fig. 3e). Notwithstanding the intrinsic underestimation of band gap in DFT due to over-screening problem,[55] this indicates a gradual bending of the bulk bands to surface,[56] as shown in the schematic of Fig. 3f.

The competing effects of band bending and electrostatic energy due to polarization at the surface can be combined to

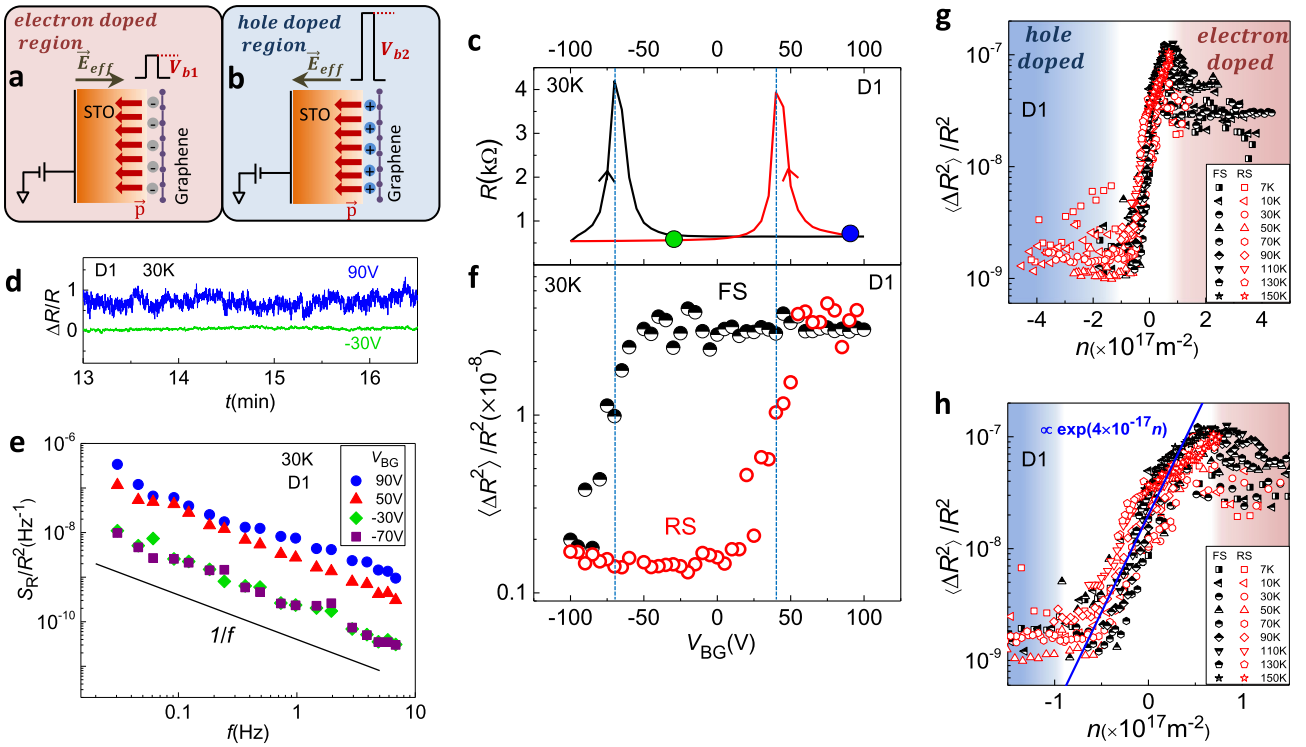


Fig. 4 Low-frequency 1/*f* noise. Schematics of the potential energy barrier of STO surface, **a** V_{b1} at electron-doped region with positive effective electric field ($\vec{E}_{eff}$) and **b** V_{b2} at hole-doped region with negative $\vec{E}_{eff}$ showing $V_{b2} > V_{b1}$, where $\vec{p}$ represents the interface dipole moment. **c** The anti-hysteresis in the transfer characteristics of device D1 at 30 K. **d** The time series of resistance fluctuations at $V_{BG} = 90$ V and −30 V, showing higher noise for $V_{BG} = 90$ V. **e** Power spectral density (S_R/R^2) of the resistance fluctuations showing 1/*f* noise characteristics. **f** Normalized 1/*f* noise ($\langle \Delta R^2 \rangle / R^2$) of SLG on STO with forward sweep (FS) and reverse sweep (RS) of V_{BG} at 30 K, showing a very large magnitude on the right side of the charge neutrality point (CNP) and almost two order of magnitude lower value on the left side of CNP for both FS and RS directions of V_{BG}. **g** Normalized 1/*f* noise ($\langle \Delta R^2 \rangle / R^2$) vs. carrier density (*n*) of the SLG channel at different temperatures from 7 K to 150 K showing a bistable feature in the electron-doped (red background) and hole-doped (blue background) regions for both FS and RS directions of V_{BG}. **h** The exponential fitting (blue line) of the noise magnitude near CNP which provides the magnitude of interfacial polarization

develop a phenomenological model for the observed anti-hysteretic behavior (Fig. 3f–h). A quantum well may be formed by the decrease in the band gap and the increase in the electrostatic potential $\approx \Delta z P^2 A_{cell}/2\varepsilon_0\varepsilon_r$ at the surface due to the dipolar field, where A_{cell} is the area of the TiO_2 unit cell. Equating the latter to the confinement scale $\Phi_P \approx 0.02$ eV, and assuming air gap between Ti and O atoms ($\varepsilon_r = 1$) at the surface, we get $P \approx 13$ μC cm^{-2}, which is similar to that obtained from DFT for bare STO, but smaller than expected from graphene–STO hybrid. DFT is well known to overestimate the polarization value even as much as by an order of magnitude, as observed in bulk materials.[57] Thus, we consider the agreement between DFT and the value obtained experimentally to be reasonable. The expected trap layer energy $E_t \approx \Delta E^s_{gap}/2$, where $\Delta E^s_{gap} \approx 0.21$ eV (Fig. 3e) is the surface band gap, is also close to that (~0.15 eV) estimated experimentally, although the underestimation of the band gap in DFT limits the accuracy of such a comparison.

Figure 3g, h describes the anti-hysteresis process schematically. As the sweep range of V_{BG} (ΔV_{BG}) increases beyond E_t, more charge carriers (electrons or holes) get trapped at the interface quantum well which increase the screening of V_{BG} leading to an increase in anti-hysteresis (Fig. 2c). At higher temperature $\gtrsim$200 K, the anti-hysteresis decreases as thermal energy of the trapped charge carriers becomes too large to remain confined by Φ_P.

Unconventional low-frequency 1/*f* noise

In addition to the transport measurement, the low-frequency 1/*f* noise in the channel resistance is also sensitive to the interface dipoles. We assume trapping–detrapping noise to be the dominant mechanism for resistnce fluctuation, which is the case for graphene FETs on conventional substrates.[37] In the presence of out-of-plane polarization *P* at STO surface, the interfacial potential barrier that determines the trapping–detrapping rate of charge across the interface, and hence the 1/*f* noise, is modified by the local effective electric field ($\vec{E}_{eff}$) (Fig. 4a, b). The typical time dependence of resistance fluctuations of the graphene channel is shown in Fig. 4d for two representative V_{BG}, with a 1/*f*-like power spectral density (S_R/R^2) (Fig. 4e). The details of the noise measurement technique[58,59] are discussed in the Methods section and Supplementary Information. Figure 4c, f correlates the variation in noise magnitude with V_{BG} (Fig. 4f) with the anti-hysteretic behavior in the channel resistance *R* (Fig. 4c). We find that $\left\langle (\Delta R)^2 \right\rangle / R^2$ (obtained by integrating S_R/R^2 over the experimental frequency range) displays a strong (anti-)hysteretic two-state behaviour as a function of V_{BG}. The top gate dependence of noise in the same graphene channel is non-hysteretic and exhibits conventional 'V'-shaped behavior[37,60] (Fig. S7 in the Supplementary Information section), confirming that the anti-hysteretic behaviour is due to surface electrical polarization on STO. Remarkably, the V_{BG} dependence of $\left\langle (\Delta R)^2 \right\rangle / R^2$ collapses on a single trace as function of density *n*, irrespective of the sweep directions or temperature (Fig. 4g). Since $n = |\vec{E}_{eff}|\varepsilon_0/e$, the monotonic change in noise across the Dirac point ($\vec{E}_{eff} = 0$) indicates an unconventional microscopic origin that depends on the *direction* of $\vec{E}_{eff}$, rather than just its magnitude.

When the STO surface is spontaneously polarized, the interface potential barrier $V_b \approx E_t - \vec{p}.\vec{E}_{eff}$ naturally leads to correlated

number-mobility fluctuation noise in the graphene channel[37,38] that is sensitive to the direction of $\vec{\mathbf{E}}_{\mathbf{eff}}$ with respect to the dipole moment $\vec{\mathbf{p}}$ at the surface. Here, $E_t\left(\approx \Delta E^s_{gap}/2 \sim 0.1\,\mathrm{eV}\right)$ is the zero-field surface barrier for electron exchange. When the characteristic trapping time scale $\tau(=\tau_0 exp[2ad])$ is distributed as $\sim 1/\tau$,[61] where $a = \sqrt{\frac{2m^*_e V_b}{\hbar^2}}$, and d are the tunnelling wave vector and the distance between the channel and surface states of STO substrate, respectively, one obtains

$$\left(S_R/R^2\right) \propto exp\left(\frac{d\sqrt{2m^*_e}}{\hbar}\frac{\vec{\mathbf{p}}.\vec{\mathbf{E}}_{\mathbf{eff}}}{\sqrt{E_t}}\right). \quad (2)$$

As shown in Fig. 4h, from the exponential fitting of the experimental $1/f$ noise magnitude with Eq. 2, we obtain $\vec{\mathbf{p}} \approx 3\times 10^{-30}\,\mathrm{C\,m}$ by assuming $d \approx 3 \pm 0.5\,\mathrm{nm}$ for the experimental bandwidth. Here, m^*_e is the effective mass of the electron in STO.[62] Estimation of surface polarization through slab calculation[14] yields $P \approx 10\ \mu\mathrm{C\,cm^{-2}}$, which is in good agreement to that obtained from the T dependence of anti-hysteresis (Fig. 2a).

In conclusion, we have shown that the dipole field at the surface of STO, created due to the off-centric movement of atoms at the TiO_2-terminated surface, strongly impacts both transfer characteristics and low-frequency noise in the graphene-STO hybrid FETs. The key observation of temperature and back gate voltage sweep range-dependent anti-hysteretic transfer characteristics in both resistance and noise suggest formation of trap states at the STO surface due to band renormalization and electrostatic confinement. We quantitatively estimate surface polarization $P \sim 12\ \mu\mathrm{C\,cm^{-2}}$, which is in good agreement with DFT calculated polarization at graphene/STO interface. Our experiment will be useful in characterizing and exploiting interfaces of graphene and polarizable materials.

METHODS

TiO_2 surface termination of STO

The STO substrates were held with a teflon holder and ultrasonicated in ethanol, deionized (DI) water, buffered hydrofluoric acid and then again in DI water for 30 min in each of them. After cleaning, the STO substrates were placed in a tube furnace and annealed for 2.5 h in an oxygen flow of $300\,\mathrm{cc\,min^{-1}}$ at 960 °C. Then, the substrates were cooled down to room temperature naturally which generates TiO_2 terminated surface[63,64] on STO.

Device fabrication and measurements

Graphene and hBN layers were first exfoliated on SiO_2 substrate by conventional micromechanical exfoliation. We used a drop of EL9 (baked at 80 °C for 2 h) placed on a transparent plastic sheet to lift suitable layers of graphene and hBN with appropriate orientation and sequence from SiO_2 substrate at ~60 °C. For this, we have used a custom-made transfer set-up consisting of an optical microscope-based high-precision mechanical micromanipulator. Subsequently, the stack of 2D heterostructure attached to the EL9 was transferred on to STO surface at $T > 100$ °C, and the EL9 was dissolved away with acetone to obtain the required heterostructure. Since the EL9 does not come into contact with the graphene/STO or graphene/hBN interfaces at any stage of the fabrication process, the method leads to highly clean van der Waals interfaces.

Transport and noise measurements were performed using a lock-in amplifier while biasing the device in the ohmic regime. The $1/f$ noise in the graphene channel on STO was measured by calculating the Fourier transform of the auto-correlation function of resistance fluctuations, $\Delta R(t)(=R(t) - \langle R\rangle)$, where $\langle R\rangle$ is the resistance averaged over the experimental time period. We simultaneously measured the time series data for both in-phase and out-of-phase component of the channel resistance, which give total noise and background noise respectively. By subtracting the background noise from the total noise, we get the sample noise. See the Supplementary Information section for details.

DFT calculations

DFT calculations were performed within the framework of plane-wave basis set as implemented in VASP[65,66] with projector augmented-wave potential.[67,68] For details please see Supplementary Information section.

Data availability

The data regarding experimental and theoretical matter that support the findings of this study are available from A.S. (email: aninditas@iisc.ac.in) and T.S.D. (email: tanusri@boson.bose.res.in), respectively, upon reasonable request.

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AUTHOR CONTRIBUTIONS

A.S., D.N., T.P., R.R., A.R., M.M., T.B., T.S.-D. and A.G. designed the experiments. R.R. prepared the TiO_2 terminated STO substrate. A.S. and T.P. fabricated the devices and performed the measurements. D.N. and T.S.-D. performed the DFT calculations. A.S., D.N., T.S.-D. and A.G. analysed the data and discussed the results.

ADDITIONAL INFORMATION

Supplementary information accompanies the paper on the *npj 2D Materials and Applications* website (https://doi.org/10.1038/s41699-018-0055-5).

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