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Research Article

Emulation of Synaptic Plasticity on a Cobalt-Based Synaptic Transistor for Neuromorphic Computing

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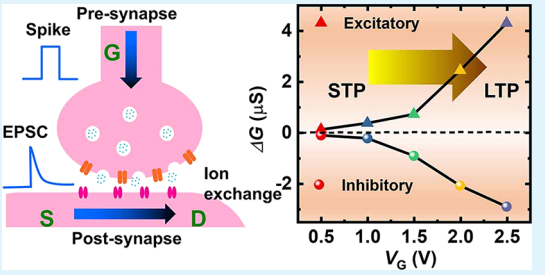
ABSTRACT: Neuromorphic computing (NC), which emulates neural activities of the human brain, is considered for the low-power implementation of artificial intelligence. Toward realizing NC, fabrication, and investigations of hardware elements—such as synaptic devices and neurons—are crucial. Electrolyte gating has been widely used for conductance modulation by massive carrier injections and has proven to be an effective way of emulating biological synapses. Synaptic devices, in the form of synaptic transistors, have been studied using various materials. Despite the remarkable progress, the study of metallic channel-based synaptic transistors remains massively unexplored. Here, we demonstrated a three-terminal electrolyte gating-modulated synaptic transistor based on a metallic cobalt thin film to emulate biological synapses. We have realized gating-controlled, non-volatile, and distinct multilevel conductance states in the proposed device. The essential synaptic functions demonstrating both short-term and long-term plasticity have been emulated in the synaptic device. A transition from short-term to long-term memory has been realized by tuning the gate pulse parameters, such as amplitude and duration. The crucial cognitive behavior, including learning, forgetting, and re-learning, has been emulated, showing a resemblance to the human brain. Beyond that, dynamic filtering behavior has been experimentally implemented in the synaptic device. These results provide an insight into the design of metallic channel-based synaptic transistors for NC.



KEYWORDS: *synaptic transistor, metallic channel, multilevel states, synaptic plasticity, neuromorphic computing*

INTRODUCTION

The human brain is a highly efficient biological computing system that can solve complex problems with an ultralow power consumption of ≈20 W.[1,2] The densely packed neural network of the human brain consists of ~10^{11} neurons interconnected by ~10^{15} synapses. Benefitting from this unique structure, the human brain can process information efficiently with massive parallelism, ultralow power consumption, high energy efficiency, self-learning, and fault tolerance. Compared to the human brain, conventional digital computers face the limitation of energy inefficiency and the significant challenge of the von Newman bottleneck due to physically separated computing and memory units.[3] Inspired by the outstanding performance of the human brain, researchers are looking for hardware implementation of brain-inspired computing. In this connection, the designing of electronic devices emulating synaptic and neuron functions is highly demanded for building neuromorphic systems.

To achieve these goals, several two-terminal synaptic devices have been widely investigated, especially by exploiting the functionalities such as phase-change memory,[4,5] atomic switch,[6,7] spintronics devices,[8,9] and memristors.[10−13] In two-terminal devices, the learning is usually achieved by feedback from the post neuron, and the signal transmission is highly depressed during the learning operation.[14,15] Therefore, complete emulation of the synapse is limited as learning and signal transmission could not be performed simultaneously. Compared to two-terminal devices, in three-terminal synaptic devices, the learning operation and signal transmission process are realized simultaneously through the gate terminal and channel, respectively, resulting in complete emulation of a synapse.

Recently, three-terminal synaptic transistors have been proposed by electrolyte gating and have proven to be an effective way of emulating biological synapses. Over the last few years, various materials, such as organic materials,[16−20] carbon nanomaterials,[21] metal oxides,[22−25] and 2D materials,[26−28] have been potentially explored as synaptic transistors. Despite remarkable progress in electrolyte-gated synaptic transistors, the study of metallic channel-based synaptic transistors remains massively unexplored. Several reports illustrate the modification of the electrical properties of

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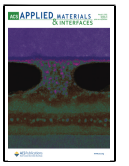

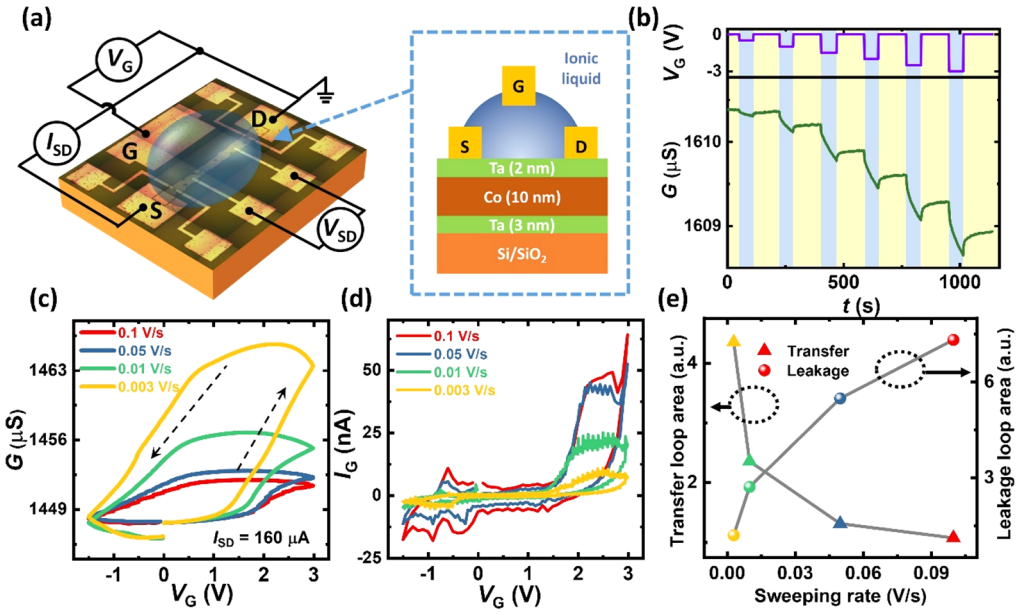

Figure 1. (a) Schematic diagram of the three-terminal cobalt-based synaptic transistor. (b) Non-volatile and distinct multilevel conductance states realized by applying a series of negative gate voltage pulses of different amplitudes (in sequence of V_G = −0.5, −1, −1.5, −2, and −2.5 V) and of the same duration (t_p = 60 s), spaced apart by 120 s. The source−drain current I_{SD} was maintained at 160 μA. (c) Channel conductance vs gate voltage curves measured at different sweeping rates of V_G (0.1, 0.05, 0.01, and 0.003 V/s) (I_{SD} = 160 μA). (d) Corresponding leakage current at different sweeping rates. (e) Area under the channel conductance vs gate voltage loop (Δ) and area under the leakage current loop (O)—as a function of the sweeping rate of V_G.

metallic thin films utilizing electrolyte gating due to massive carrier injection.[29−31]

In this regard, metallic cobalt thin films are of substantial academic interest and industrial applications due to their intriguing magnetic, electrical, physical, and mechanical properties.[32−35] Cobalt thin films have widely been employed for technological applications, such as magnetic information storage,[38] integrated circuitry devices,[36,37] and sensor systems.[39] Compared to other metallic systems, such as gold and platinum, cobalt has an exciting spin degree of freedom that can be tuned to enhance the device performance and could be interesting to future spin-based neuromorphic computing (NC).[40] The aroused research interest toward spin devices in the field of NC[7,8] makes cobalt unique as a synaptic device.

In this study, we reported a three-terminal electrolyte gating-modulated synaptic transistor based on a metallic cobalt thin film to emulate biological synapses. This is the first investigation of a synaptic transistor using a metallic (and ferromagnetic) channel. We have successfully imitated the essential synaptic functions, including excitatory/inhibitory postsynaptic conductance (E/IPSC), paired-pulse facilitation/depression (PPF/D), and long-term potentiation/depression (LTP/D) in the proposed device. The transition from short-term memory (STM) to long-term memory (LTM) has been realized by tuning the gate pulse parameters, such as amplitude and duration. Moreover, the essential psychological behaviors of learning, forgetting, and re-learning of the human brain have been mimicked. Beyond them, both high-pass/low-pass filtering behaviors have been experimentally implemented by changing the gate voltage polarity in a single synaptic device.

RESULTS AND DISCUSSION

For the three-terminal cobalt-based synaptic transistor, the channel consists of Ta (3 nm)/Co (10 nm)/Ta (2 nm) stack on a thermally oxidized silicon substrate. The bottom Ta layer was used as a buffer layer between the substrate and Co to increase the adhesion. The top Ta layer was used as a capping layer to protect cobalt from being oxidized by the atmosphere, while the lower resistance of the thicker Co layer enables the passage of almost all current across it.[41−43] The channel was fabricated using standard photolithography and a subsequent lift-off process. The coplanar gate electrode consisted of Ta (5 nm)/Cu (90 nm)/Ta (5 nm) and was patterned using photolithography and deposited via sputtering. Further details of device fabrication can be found in the Experimental Details section. The current−voltage relationship of the device showed linear behavior, ensuring good Ohmic contacts under the electrodes (Figure S1b, Supporting Information).[40]

As received ionic liquid (IL), 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (EMIM-TFSI) was used as the gate dielectric for the present study. The IL has a high capacitance value of 2.5 μF/cm^2 at 70 Hz, as evident from the $C \sim f$ measurement, shown in the Supporting Information (Figure S1a). A small drop (50 μL) of IL was dropped on the device covering the channel and a more significant part of the gate electrode.

The schematic diagram of the three-terminal cobalt-based synaptic transistor (with electrical connection) and the channel multilayer stack are shown in Figure 1a. A small direct current (I_{SD} = 160 μA) was applied across the source (S) and the drain (D) electrode to measure the channel conductance. Such a smaller I_{SD} was chosen to reduce the side gating effect (potential drop across source and drain) and avoid joule heating. The gate voltage (V_G) was applied directly on the gate electrode (G), and the drain terminal was grounded throughout the measurement. All the electrical measurements were carried out in a vacuum of 10^{-3} mbar to avoid ambient humidity.

For the electrolyte-gated cobalt-based synaptic transistor, the variation of channel conductance as a function of gate

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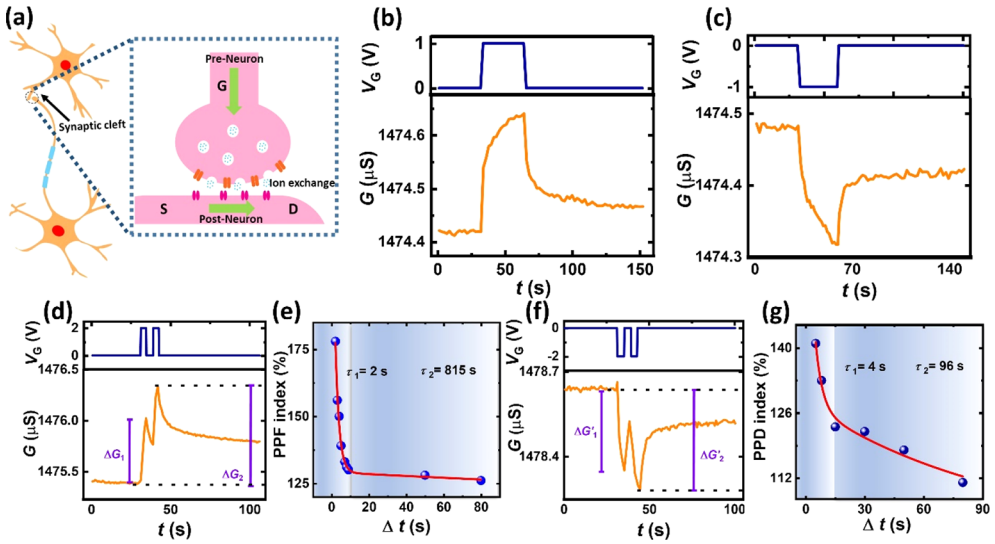

Figure 2. (a) Schematic illustration of signal transmission across the biological synapse, the functional connection between two adjoining neurons. (b) EPSC triggered by a positive gate pulse (1 V, 30 s), I_{SD} = 160 μA. (c) IPSC triggered by a negative gate pulse (−1 V, 30 s), I_{SD} = 160 μA. (d) PPF is exhibited by applying a pair of identical positive gate pulses (2 V, 5 s), 2 s apart. ΔG_1 and ΔG_2 are relative modulations evoked by to first and second pulse, respectively. (e) PPF index is plotted as a function of time interval (Δt) between pulses. (f) PPD behavior is exhibited by applying a pair of identical negative gate pulses (−2 V, 5 s), 2 s apart. $\Delta G_{1'}$ and $\Delta G_{2'}$ are the relative modulation caused by the first and second pulse, respectively. (g) PPD index is plotted as a function of time interval (Δt) between pulses.

voltage was measured by sweeping the V_G from 0 to 3 V, then from 3 to −1.5 V, and finally back to 0 V, as shown in Figure 1c. A giant anticlockwise hysteresis loop in the channel conductance versus the gate voltage curves indicates the non-volatile and reversible change of channel conductance, suitable for emulation of synaptic properties. The leakage current I_G was monitored simultaneously, as shown in Figure 1d. As the IL is ionically conducting and electrically insulating, I_G was negligible. I_G (∼nA) was orders of magnitude smaller than the input current (∼160 μA), indicating that conductance modulation was unaffected by the leakage current.

The study of IL gating is widespread for dramatic conductance modulation by massive carrier injection.[31,44] The working mechanism of the electrolyte-gated synaptic transistor can be explained as the combined outcome of electrostatic effect and electrochemical doping. Owing to the electrostatic effect, under a positive/negative gate voltage, the cations/anions in the electrolyte accumulate at the interface between the channel and the electrolyte, forming an electric double layer acting as a nanocapacitor. The strong electric field causes accumulation/depletion of electrons in the channel during positive/negative gating, resulting in increased/decreased channel conductance. The electrostatic effect is responsible for the volatile change. Unlike the case in semiconductors, the penetration depth of the electric field in metals is limited due to the short screening length, typically causing a lower conductance modulation.

The IL contains traces of water, which undergoes hydrolysis splitting and releases protons and hydroxyl ions above a threshold (V_T).[45] In the cobalt-based synaptic transistor, we suggest that the higher channel conductance modulation is related closely to the electrochemical doping of the channel involving proton diffusion.[28,46−50] Depending on the polarity of gate voltage, the ions, which is typically proton, can be reversibly injected into or extracted out of the channel by electrochemical doping.[50,51] The electrochemical doping effect is responsive to the non-volatile changes of channel conductance. In contrast, the proton is extracted from the channel under a negative gating, decreasing the channel conductance and restoring it to the initial value. The schematic illustration of the electrostatic effect and the electrochemical doping process of the channel is shown in the Supporting Information, Figure S4.

The channel conductance versus gate voltage curves were measured by sweeping V_G at different rates (0.1, 0.05, 0.01, and 0.003 V/s) as shown in Figure 1c, and the corresponding leakage current was monitored (Figure 1d). The results are summarized in Figure 1e, indicating that the area under the channel conductance versus the gate voltage curves increases inversely (left), and the leakage current curve increases directly (right) as a function of the sweeping rate. It was observed that the slowest (fastest) sweeping rate results in a giant (tiny) channel conductance versus gate voltage loop. At a slower sweeping rate, the device is given more time to respond to the changing gate voltage, resulting in more proton-related electrochemical doping, hence causing a larger change in channel conductance.

Multilevel, non-volatile conductance states are crucial for the emulation of synaptic functionalities and analog computation. By applying a series of negative gate voltage pulses of different amplitudes, in a sequence of 0.5, −1, −1.5, −2, and −2.5 V, the non-volatile and distinct multilevel conductance states were realized in the synaptic device, Figure 1b. Each gate pulse has t_p = 60 s and is spaced apart by 120 s. A constant I_{SD} = 160 μA was applied to measure the channel conductance. The channel conductance decreased during negative gating (more decrement at higher amplitude) while retained the same state at zero gating, exhibiting non-volatile nature. The retention of a separate state is shown in Figure S5, showing excellent retention for at least 3 × 10^3 s. The observed multilevel behavior is mainly due to the controlled interfacial electrochemical doping of the channel under programmed gate voltages.[52] The above results demonstrate multiple distinct, non-volatile conductance states and show that the memory is

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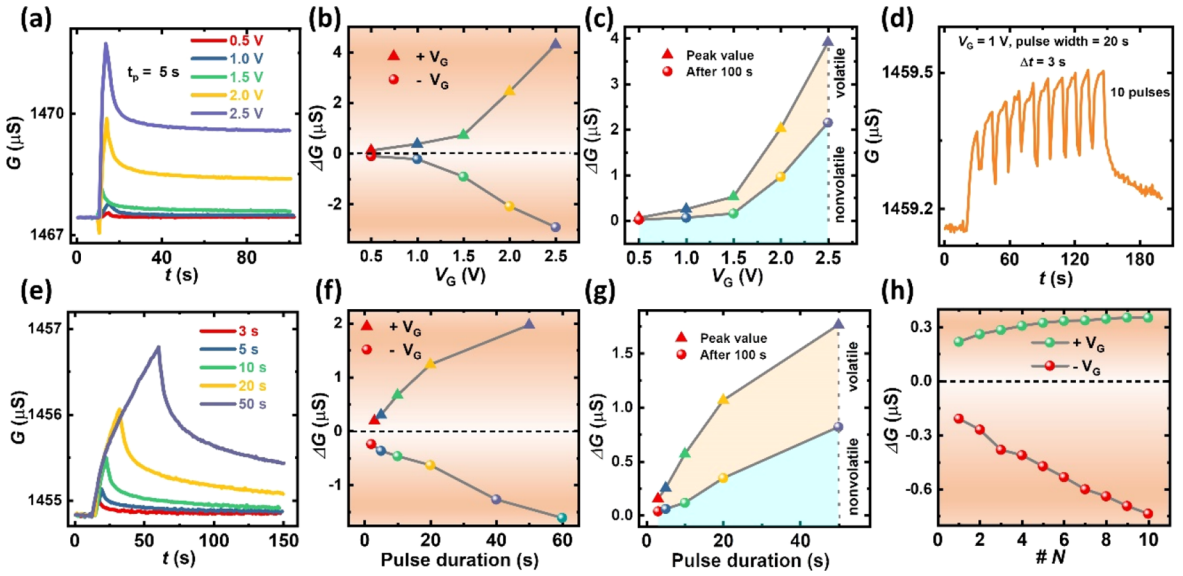

Figure 3. (a) EPSC triggered by gate pulses of the same duration (t_p = 5 s) and different amplitudes (0.5, 1.0, 1.5, 2.0, and 2.5 V), I_{SD} = 160 μA. (b) Gate amplitude-dependent channel conductance modulation in both positive and negative polarity. (c) Gate amplitude-dependent conductance modulation measured immediately (▲) and after 100 s (●) of pulse removal, demonstrating the transition from STM to LTM. (d) EPSC triggered by a series of 10 consecutive gate pulses (1 V, 10 s), I_{SD} = 160 μA. (e) EPSC triggered by gate pulses of the same amplitude (V_G = 2 V) and different durations (3, 5, 10, 20, and 60 s), I_{SD} = 160 μA. (f) Gate pulse duration-dependent channel conductance modulation in both positive and negative polarity. (g) Gate pulse duration-dependent conductance modulation measured immediately (▲) and after 100 s (●) of pulse removal, showing a transition from STM to LTM. (h) Gate pulse number-dependent channel conductance modulation in both positive and negative polarity.

suitable for multilevel memory applications with good retention. Furthermore, the parameters such as retention, number of states, and read/write speed need to be further optimized for actual implementation in NC.

Figure 2a shows the schematic diagram of signal transmission across a synapse, the functional connection between two adjoining neurons. The signal transmission across synapses starts with the firing of an action potential on the presynaptic neuron. The presynaptic neuron releases neurotransmitters that diffuse across the synaptic cleft and docks with the receptor of the postsynaptic neuron. This triggers a potential drop across the postsynaptic membrane called the postsynaptic potential (PSP). The PSP amplitude depends on the connection strength of the adjoining neurons, termed as synaptic weight. Synaptic plasticity is the ability of a synapse to change its synaptic weight in response to external stimuli; it is considered as the basis for learning and memory of the human brain.[53] It is broadly classified into short-term plasticity (STP) and long-term plasticity depending on the retention time of the synaptic weight.

In a cobalt-based synaptic transistor, gating-controlled channel conductance modulation resembles a change in synaptic weight in the biological synapse. The channel conductance and gate voltage are analogous to synaptic weight and action potential, respectively. The mobile ions play the role of neurotransmitters. The PSP results in a change in the channel conductance termed as postsynaptic conductance (PSC).[54] If the PSC is excitatory, it is termed as excitatory PSC (EPSC), and if inhibitory, it is termed as IPSC. A typical EPSC is demonstrated in Figure 2b by firing a short positive gate pulse (1 V, 5 s) on the gate electrode. A small source−drain current (I_{SD} = 160 μA) was applied to monitor the channel conductance.

During gating, the channel conductance was raised to the peak and gradually decayed to the resting state. Analogously, a typical IPSC is demonstrated in Figure 2c by firing a short negative gate pulse (−1 V, 5 s). The channel conductance decreased to the lowest value with gating and gradually recovered to the resting state. Before gating, the anions ($TFSI^-$) and cations ($EMIM^+$) were distributed randomly in the IL. During gating, the ions get accumulated at the channel/IL interface and provide additional charge carriers in the channel, resulting in channel conductance modulation. However, the ions diffuse back to the equilibrium state after gating, restoring the channel conductance to the initial value. EPSC and IPSC are complementary functions that underlie successful signal transmission across the synapse.

STP is defined as strengthening or weakening the synaptic weight for a shorter time, ranging from a few milliseconds to minutes.[17] In the human brain, STP is used in various computations, working memory, and STM. PPF is a vital form of STP. This is well studied for decoding temporal information in auditory and visual signals.[53] PPF depicts a phenomenon where a pair of identical presynaptic pulses are applied in rapid succession; the conductance modulation evoked by the second pulse is higher than the first one.

The PPF behavior was investigated in our cobalt synaptic transistor by applying a pair of identical pulses (2 V, 10 s) with Δt = 2 s, as shown in Figure 2d. It is seen that the conductance modulation evoked by the second pulse (ΔG_2) is higher than the first one (ΔG_1) relative to the base value (V_G = 0). The higher value of ΔG_2 was due to the addition of residual ions (by the first pulse) to the ions accumulated by the second pulse when the second pulse was fired much before the ion relaxation. The PPF index is defined as $\Delta G_2/\Delta G_1 \times 100\%$ and was measured by varying the time interval (Δt) between pulses and shown in Figure 2e. We have obtained the highest PPF

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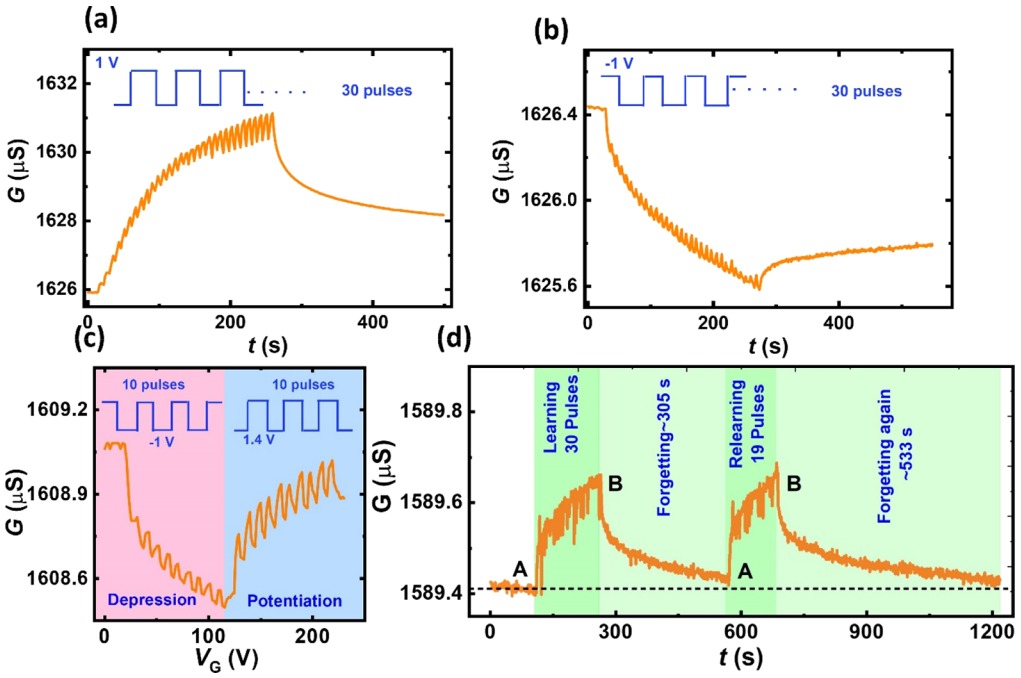

Figure 4. (a) LTP—channel conductance vs time stimulated by 30 consecutive positive gate pulses (1 V, 5 s) spaced apart by 2 s, I_{SD} = 160 μA. (b) LTD channel conductance vs time stimulated by 30 consecutive negative gate pulses (−1 V, 5 s) spaced apart by 2 s, I_{SD} = 160 μA. (c) Demonstrating depression (D) and potentiation (P) of synaptic weight by applying 10 consecutive negative gate pulses (−1 V, 5 s), Δt = 2 s for D, and 10 consecutive positive pulses (1.4 V, 5 s), Δt = 2 s for P. (d) Emulation of psychological behavior, learning, forgetting, and re-learning in the cobalt-based synaptic transistor.

index (170%) at the smallest time interval (2 s) attributed to more residual ions. The PPF index variation with Δt was fitted to the standard PPF equation,[55] defined as

$$\mathrm{PPF} = 100 + C_1 \cdot \exp\left(-\frac{\Delta t}{\tau_1}\right) + C_2 \cdot \exp\left(-\frac{\Delta t}{\tau_2}\right) \quad (1)$$

where C_1 and C_2 are the amplitudes of initial facilitation and τ_1 and τ_2 are the relaxation time constants of different phases. The PPF index undergoes a double-exponential decay, corresponding to a rapid decay (τ_1 = 2 s) and slow decay (τ_2 = 815 s). In contrast, paired-pulse depression (PPD) was demonstrated in the cobalt synaptic transistor by applying a pair of negative pulses (−2 V, 10 s) with Δt = 2 s, where ΔG_2 was higher than ΔG_1, Figure 2f. The variation of PPD index with Δt was fitted with eq 1 and showed a rapid (τ_1 = 4 s) and slow (τ_2 = 96 s) phase decay (Figure 2g). Such PPF and PPD behavior in cobalt-based synaptic transistors are pretty similar to the STP behavior in biological synapses. However, the decay time constants are larger than the biological synapses due to the slow diffusion of ions in the device.

The human memory system mainly consists of two forms of memory called STM and LTM. The schematic diagram of the multistore model of the human memory system is shown in Figure S6. Different memory types are associated with different states of synaptic plasticity: STM is associated with STP, while LTM is associated with long-term plasticity.[56] A transition from STP to LTP (and hence from STM to LTM) has been demonstrated in cobalt-based synaptic transistors by variation of gate pulse, amplitude, duration, and number.[57]

Synaptic plasticity can be tuned by varying the gate pulse amplitude. Figure 3a shows the EPSC triggered by a series of positive gate pulses of the same duration (t_p = 5 s) and different amplitudes (0.5, 1.0, 1.5, 2.0, and 2.5 V). I_{SD} = 160 μA was applied to monitor the channel conductance. The EPSC peak and retention have increased systematically with increasing gate pulse amplitude. In contrast, IPSC triggered by negative gate pulses of the same duration (t_p = 5 s) and different amplitudes (−0.5, −1.0, −1.5, −2.0, and −2.5 V) is shown in the Supporting Information (Figure S7a). The conductance modulation (ΔG) evoked by a gate pulse is defined as the difference between the base (at V_G = 0) and the peak value. ΔG increased monotonously with gate pulse amplitude in both gate polarities due to stronger electrochemical doping at higher gate amplitude, demonstrating the transition from STP to LTP (Figure 3b). As shown in Figure 3c, the conductance modulation was measured immediately at a peak value and after 100 s of pulse removal, defining the total change and non-volatile change of channel conductance, respectively.[28] The significant increment of non-volatile part with increasing gate amplitude indicates a transition from STM to LTM (Figure 3c).

Pulse duration plays a significant role in synaptic plasticity. Figure 3e shows EPSC triggered by gate pulses of the same amplitude (V_G = 2 V) and different durations (3, 5, 10, 20, and 50 s). The EPSC peak and state retention have the highest value for the most extended pulse duration. In contrast, the IPSC triggered by negative gate pulses of different durations is shown in Supporting Information (Figure S7b). The conductance modulation (ΔG) is summarized as a function of pulse duration in Figure 3f, showing linear dependence for both gate polarities. This demonstrates a transition to LTP due to prolonged electrochemical doping for a longer pulse duration. It is to be noted that repeated electrical measurements cause sample degradation by repeated intercalation/extraction of ions, resulting in lower conductance modulation. The conductance modulation was measured at peak (total change) and after 100 s (non-volatile change) of pulse removal

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and plotted as a function of pulse duration (Figure 3g). It shows that the non-volatile part increases (decreasing) with the increase (decrease) of pulse duration, showing a transition from STM to LTM.

Synaptic plasticity can also be tuned by gate pulse number. Here, we have applied 10 consecutive positive gate pulses (1 V, 10 s) spaced apart by 3 s on the gate electrode and monitored the EPSC, as shown in Figure 3d. The channel conductance increased monotonously with each consecutive pulse. The conductance modulation (ΔG) at each pulse was measured with respect to the base value ($V_G = 0$). In contrast, the IPSC was monitored by applying 10 consecutive negative gate pulses (−1 V, 10 s) with Δt = 3 s, as shown in Figure S7c. ΔG increased significantly with pulse number, indicating a transition trend from STP to LTP (Figure 3h). This concludes that, at higher pulse amplitude, duration, and the number of pulses, ΔG is higher due to more electrochemical proton doping, resulting in a transition from STP to LTP, hence from STM to LTM.

Long-term plasticity is widely considered as the basis for learning and memory in the human brain.[53] This is defined as the persistent modification of the synaptic weight that usually lasts from hours to years.[58] Long-term plasticity is emulated in the cobalt-based synaptic transistor via LTP and long-term depression (LTD). LTP was comprehended by applying 30 consecutive positive gate pulses (1 V, 5 s) spaced apart by 2 s on the gate terminal.

A small direct current, I_{SD} = 160 μA, was applied to measure the channel conductance. The series of positive gate pulses have significantly facilitated the channel conductance. However, after pulse removal, the channel conductance decayed initially and remained at a higher conducting state for a longer time (till we measure), showing its long-term effect (Figure 4a). In contrast, LTD was realized by applying 30 consecutive negative gate pulses (−1 V, 5 s), spaced apart by 2 s, resulting in a drastic decrement of channel conductance. Furthermore, the conductance remained at a lower conducting state for a longer time (till we measure) after pulse removal, shown in Figure 4b. In Figure 4c, the channel conductance was decreased by applying 10 consecutive negative gate pulses (−1 V, 5 s) with Δt = 2 s. Again, 10 consecutive positive gate pulses (1.4 V, 5 s), with Δt = 2 s, were applied to bring it back to the initial state. Three cycles of potentiation and depression of synaptic weight have been simulated in Figure S8 (Supporting Information), showing the repeatability of the synaptic device.

This shows that the cobalt synaptic transistor can imitate essential long-term plasticity functions, and the mechanism can be explained as follows. During LTP, the channel conductance was increased monotonously with subsequent gate pulses due to the intercalation of more protons into the channel. However, the proton remains inside the channel even after gating, resulting in a long-term change of channel conductance. During LTD, the channel conductance was decreased monotonously by extracting protons from the channel with subsequent negative pulses.

We have successfully imitated the psychological learning, re-learning, and forgetting behaviors of the human brain in the cobalt synaptic transistor.[19,59] It was demonstrated by applying a series of positive gate voltage pulses. As shown in Figure 4d, by applying 30 consecutive positive gate pulses (1 V, 5 s), the channel conductance was increased from a lower conducting state (A) to a higher conducting state (B), considered as learning. After learning, the system spontaneously decays to state A in 305 s, considered as forgetting. Again, 19 consecutive positive gate pulses were applied on the gate electrode to change the channel conductance from state A to state B for re-learning. It is noteworthy that only 19 pulses were used to realize re-learning compared to 30 pulses for the learning. After re-learning, the system decays spontaneously to state A in 533 s. This implies that for re-learning, we need lesser effort, and re-learning makes the forgetting process slower. Hence, it is easier to remember a forgotten memory than remembering a fresh memory in the proposed synaptic transistor, similar to the human brain.

The cobalt-based synaptic transistors can perform as a dynamic filter for information transmission.[53] The short-term facilitation/depression phenomenon contributes to high-/low-pass filtering behavior. The schematic illustration of the filtering behavior of the cobalt synaptic transistor is shown in Figure S9. To demonstrate high-pass filtering behavior, the EPSC evoked by positive stimulus trains of different frequencies is shown in Figure 5a. I_{SD} = 160 μA was applied across the source and drain to measure channel conductance. Each stimulus train comprises five gate pulses (1 V, 2 s). EPSC response was increased substantially for higher frequency. The amplitude gain is defined as the ratio A_5/A_1, where A_1 and A_5 are the increments of channel conductance relative to the base value (at $V_G = 0$), after the first and fifth pulse, respectively (Figure 5b inset). As shown in Figure 5b, the amplitude gain increased with increasing frequency, illustrating that the device can easily pass the high-frequency signals. This presents the high-pass filtering behavior of the proposed transistor for sophisticated information processing.

On the other hand, Figure 5d shows the IPSC evoked by negative stimulus trains (−1 V, 2 s) of different frequencies to demonstrate low-pass filtering behavior. The IPSC response

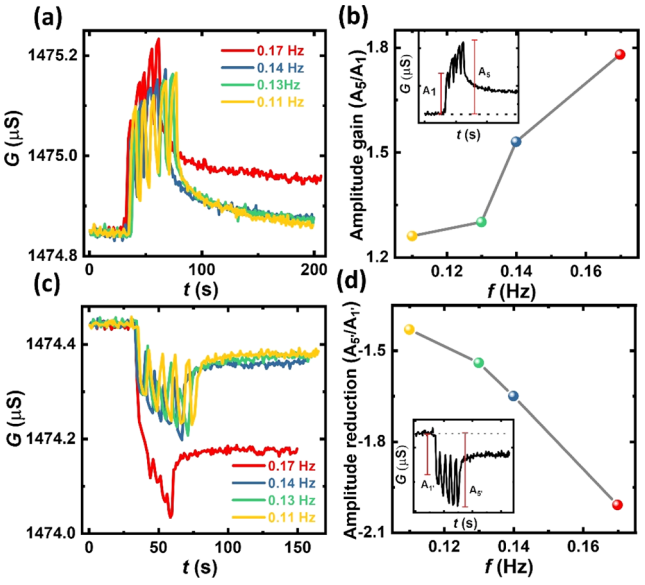

Figure 5. (a) EPSC response to stimulus train (1 V, 2 s) fired at different frequencies. (b) Amplitude gain (A_5/A_1) as a function of frequency, acting as a high-pass filter. The inset shows A_1 and A_5 as the conductance modulation evoked by the first and fifth pulse, respectively. (c) IPSC response to stimulus trains (−1 V, 2 s) fired at different frequencies. (d) Amplitude reduction ($A_{5'}/A_{1'}$) as a function of frequency, acting as a low-pass filter.

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was increased (downward) significantly for a higher frequency. The amplitude reduction is defined as the ratio $A_{5'}/A_{1'}$, where $A_{1'}$ and $A_{5'}$ are channel conductance decrements after the first and fifth pulse, respectively (Figure 5e inset). The amplitude reduction increases (downward) with frequency, emulating the low-pass filtering behavior (Figure 5e). All the stimulus train consists of pulses of the same voltage and width, whereas the spacing between them is varied. Due to the lower spacing between the pulses at higher frequencies, the ions do not get enough time for relaxation, leading to more conductance modulation. Hence, both high- and low-pass filtering behaviors were successfully mimicked in the same device by changing the gate polarity, which is crucial for selective communication.[18,60,61]

CONCLUSIONS

In summary, we have systematically studied a three-terminal electrolyte-gated synaptic transistor based on a metallic cobalt thin film for the first time. We have obtained a giant channel conductance versus gate voltage loop at the slowest sweeping rate of gate voltage, showing a non-volatile and reversible change of channel conductance. Distinct multilevel and non-volatile conductance states have been realized by applying a series of gate pulses of different amplitudes. We have emulated several essential synaptic functions, including EPSC/IPSC, PPF/D, and LTP/D, in the proposed synaptic device. Furthermore, a transition from STM to LTM has been realized by tuning the gate pulse parameters such as amplitude and duration. Moreover, the essential psychological behaviors of learning, forgetting, and re-learning of the human brain have been mimicked. Beyond that, both high- and low-pass filtering behaviors have been experimentally implemented by changing the gate voltage polarity in the same synaptic device. This work highlights the potential application of a metallic cobalt thin-film-based synaptic transistor in the emerging NC field.

EXPERIMENTAL DETAILS

Device Fabrication. The channel having a dimension of 1000 μm (L) × 200 μm (W) was fabricated using standard photolithography and a subsequent lift-off process. The Ta (3 nm)/Co (10 nm)/Ta (2 nm) multilayer stack was deposited on a thermally oxidized silicon substrate using DC magnetron sputtering. An Ar pressure of 2 mTorr and a DC power of 50 W were used during the deposition process. The three-terminal coplanar (source, drain, and gate electrode lie on the same plane) electrode was defined using photolithography. The electrode consisting of Ta (5 nm)/Cu (90 nm)/Ta (5 nm) stack was deposited using DC magnetron sputtering. After device fabrication, a small drop (~diameter of 400−500 μm, volume ~ 50 μL) of as-received EMIM-TFSI ≥ 98% (HPLC) IL from Sigma-Aldrich was dropped on the device covering the channel and gate electrode. This makes the device ready for further measurements.

Electrical Measurements. All the electrical measurements were performed at room temperature using LakeShore Janis ST300 compact cryostats. A vacuum of 10^{-3} mbar was maintained to protect the IL from ambient and to reduce noise during data collection. Yokogawa GS20 DC voltage/current source and Keithley 2000 multimeter were used to supply I_{SD} and measure channel conductance, respectively. Meanwhile, a Keithley 6517B electrometer was used to apply gate voltage pulses. The frequency-dependent capacitance measurement of the IL was carried out using GWINSTEK LCR-8105G.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.1c19916.

Capacitance ~ frequency measurement of the gate electrolyte, current−voltage relationship of the device, AFM image of the channel, channel conductance and leakage current as a function of V_G at different I_{SD} values, schematic illustration of the working mechanism of the synaptic transistor, retention of the state, multilevel memory model of the human brain, IPSC response for gate pulses of different amplitudes, durations and series of pulses, three cycles of potentiation and depression of synaptic weight, schematics of high- and low-pass filtering behavior, energy consumption of the device, and in-plane and out-of-plane magnetic measurements of the channel (PDF)

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Notes

The authors declare no competing financial interest.

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