Low Voltage CMOS op-amp with Rail-to-Rail Input/Output Swing.

S V Gopalaiah and A P Shivaprasad
Electrical Communication Engineering Department
Indian Institute of Science
Bangalore-560012.
svg@ece.iisc.ernet.in aps@ece.iisc.ernet.in

Abstract*—As the supply voltage to a standard CMOS op-amp is reduced, the input common mode range and the output swing get reduced drastically. Special biasing circuits have to be used to raise them up to rail-to-rail supply voltage. Three low voltage op-amps with new biasing circuits have been proposed in this paper and their performance evaluated. The op-amp design is focused on dynamic range and high drive capability.*

I. Introduction

The importance of mixed mode integrated circuits using low supply voltage is enormously growing in recent past [1] [2] [3]. The large component density scaling particularly in VLSI demands lower power consumption in CMOS technology which is a key factor in modern portable equipments. This increases the battery life and also, the packaging density and circuit reliability. The trend has also been towards high precision with reduced supply voltage. The power consumption can be minimized through the reduction in supply voltage. The latest trends suggest that supply voltages can go down to 1.2 V and may be less even [5], [6]. Hence, the traditional CMOS concepts cannot be used with very low supply circuits unless process technology with low threshold voltage is developed, the design of standard CMOS analogue / mixed circuits with a threshold voltage of less than 0.7V opens up a great research interest.

The fundamental building block of any analogue/mixed signal circuit is the Operational Amplifier (op-amp) [7] [8]. With the reduction of supply voltage, the CM input voltage range of conventional CMOS differential amplifier becomes narrower and lies in the region between $V_{SS} + V_T + 2V_{Dsat}$ (i.e, V_A and V_{DD}) as shown in Fig. 1 [7], where V_{SS} ,V_{DD} are negative and positive supply voltages respectively, V_T is the threshold voltage of CMOS device and V_{Dsat} is the saturation voltage of the transistor.

The decrease in Input Common Mode Range(ICMR) imposes a serious restriction over which the input signal can be applied. If the applied input signal falls in the forbidden region, it will not be amplified properly. It is clear from Fig. 1 that the maximum input signal levels at the input of the differential pair for proper amplification must lie in the region around a DC ($\frac{V_{DD}+V_A}{2}$), where V_A is the minimum

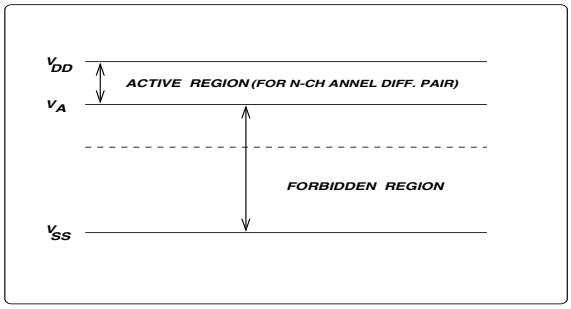

Fig. 1. Operation zone of low supply CMOS op-amp.

permissible CM voltage level of the differential amplifier. It is also clear that an input signal with zero DC falls in the forbidden region and therefore is not suitable for amplification.
To extend ICMR in low voltage CMOS op-amp, a voltage multiplier technique has been proposed recently [10], but circuit design complex. Here we propose, a simple capacitor switching circuit which moves the input signal from the forbidden region to the active region of the differential amplifier. Also, at the output stage a modified class-AB biasing circuit is proposed to obtain maximum swing by employing source follower and common source gain stage combination.

The rest of the paper has been organized as follows, In section II, a Switched Capacitor Circuit(SCC) to increase the Input Common Mode Range (ICMR) to rail-to-rail voltage at the input and a new floating bias circuit at the output of an op-amp to give rail-to-rail swing have been described. In section III, three complete op-amps with a floating bias is discussed. Section IV gives performances of the proposed op-amps and conclusions are drawn in section V.

II. Circuit Description and Operation

A. The differential input stage

The input differential stage of the low voltage op-amp accepts common mode input only over a limited range i.e., from V_A to V_{DD} (Fig. 1). But, the requirement is to

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spread this CM input range to rail-to-rail voltage, i.e., over the entire range from V_{SS} to V_{DD}. In order to achieve this, an ICMR enhancer circuit called Switched Capacitor Circuit (SCC) is introduced at the input of op-amp. The transfer characteristic of SCC is shown in Fig. 2 and is described by a straight line equation [9].

$$V_{out} = mV_{in} - (m-1)V_{DD} \quad (1)$$

where m=$\frac{(V_{DD}-V_A)}{(V_{DD}-V_{SS})}$ (slope of the curve) and V_A= 0.2 V, a minimum CM voltage level of the differential amplifier, V_{SS} = - 0.6 V and V_{DD} = + 0.6 V. The transfer function (Eq. 1)(Fig. 2) of the SCC to be introduced, becomes,

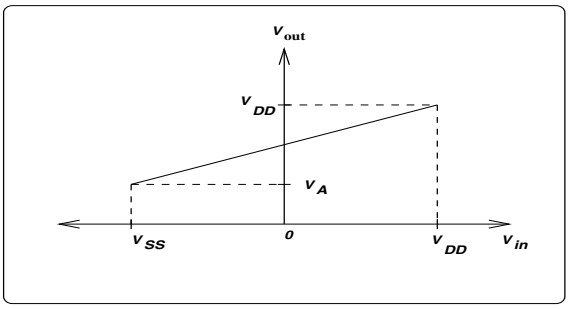

Fig. 2. Transfer characteristic of SCC.

$$V_{out} = \frac{V_{in}}{3} + \frac{2V_{DD}}{3} \quad (2)$$

B. SCC Implementation

The SCC has two identical circuits shown in schematic (Fig. 3) which are connected to the inputs of the differential pair of op-amp (V_{in}^+ and V_{in}^-). The SCC generates two identical parallel paths (P and Q) to supply signal continuously during complementary clock phase $\phi 1$ and $\phi 2$ to the input of the differential pair. The circuit comprises of capacitors C1 to C4 where C2= 2C1 and C4= 2C3 and switches S1-S8. The switches S1 to S4 are driven by the clock $\phi 1$ and S5 to S8 by the clock $\phi 2$. During $\phi 1$, switches S1 to S4 are closed, the capacitors C1 and C2 perform the voltage division operation while C3 and C4 get discharged through S3 and S4. During $\phi 2$, the switches S5 to S8 are closed, the capacitors C3 and C4 share the charges to perform voltage division operation while C1 and C2 get discharged through S5 and S6. Hence, it is clear that SCC attenuates the signal by 3 and introduces a DC component equal to $\frac{2V_{DD}}{3}$. Thus, the proposed circuit implements Eq.(2). Thus, SCC accepts the input signal and moves it to the active region of the basic op-amp (Fig.1) and realizes the level shifting operation to cover the entire CM range.

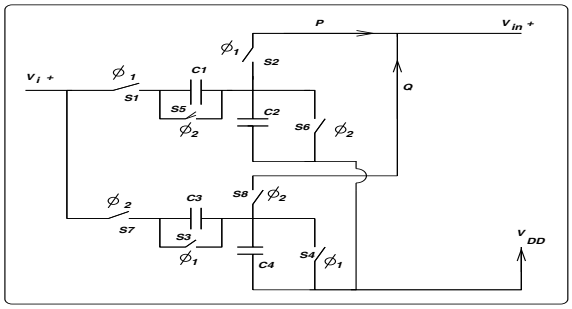

Fig. 3. Schematic of SCC.

C. The output stage

It is well known that, if the supply voltage to a class-AB CMOS amplifier is reduced below the sum of two threshold voltages of NMOS and PMOS, both the transistors go to the cut off state under quiescent condition. This reduces the dynamic range and increases output distortion. In order to overcome this problem and to achieve rail-to-rail output swing, the output stage is driven by two floating biases (Fig. 4) which prevent the output transistors going to cut off state at the quiescent operating condition. It is also clear that, in any low power op-amp circuit design low output impedance is desirable but classical source follower configurations are not allowed in low voltage applications as the dynamic range gets reduced considerably. Most of the class-AB output stages have high output impedance as they employ common source configuration. As a result, the output swing gets reduced. Ideally, the source follower and common source gain stages are combined to achieve low output impedance [11]. The amplifier describe in this paper, is a combination of source follower and common source gain stage to achieve a class-AB operation with low output impedance, high drive capability while still producing rail-to-rail output swing.

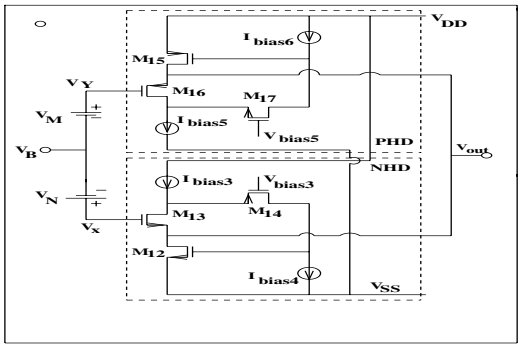

Fig. 4. Output stage with floating biases .

The floating bias scheme shown in the Fig. 4 where V_M and V_N are used to generate two separate dual in phase

signals to drive the output transistors M_{13} and M_{16}. The output stage consists of Positive Half Driver (PHD) capable of sourcing large amount of current and Negative Half Driver (NHD) capable of sinking large amount of current. The transistors M_{15} in PHD and M_{12} in NHD are connected in a common source configuration allowing output to swing to rail-to-rail supply voltage in a low voltage class-AB output stage. However, the output is also connected to source followers. Both NHD and PHD circuits are closed loop feedback networks. The two feedback loops lower the effective output resistance of the output stage. The NHD and PHD are symmetrical to each other.

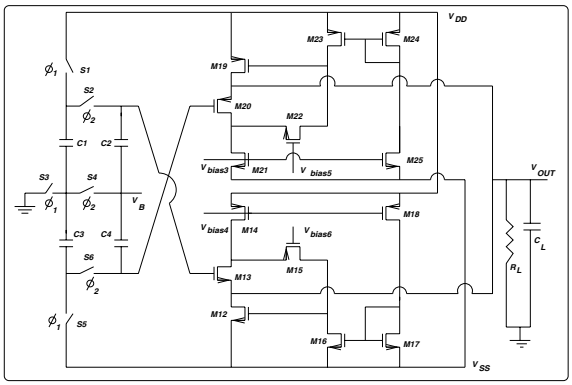

Fig. 5. Class-AB output stage with NHD, PHD implementation.

In the circuit design, I_{bias3} is designated to be greater than I_{bias4}. The current difference I_{bias3}-I_{bias4} flows through the transistors M_{13} and M_{12}. Unlike most class-AB output stages, the gate of M_{12} is controlled indirectly through the feedback loop comprising of M_{13} and M_{14}. The operation of the feedback loop is explained below. If we consider a fast transient decrease in voltage at V_B, the decrease results in steering of I_{bias3} into M_{14} thereby increasing the voltage at the gate of M_{12} which in turn cause M_{12} to sink additional current. Subsequently V_{out} is lowered until the gate source voltage of M_{13} reaches steady state. The overall result, with respect to the forward gain is that the driver circuit behaves like a source follower configuration, but the basic difference of this scheme is that the output impedance is much lower than that of a classical source follower. The outputs of PHD and NHD are connected together to form the op-amp output. The practical implementation of this circuit is shown in Fig. 5. The floating biases V_M and V_N are implemented by using switched capacitor technique.

III. The op-amp Schemes

The complete op-amps are shown in Figs. 6-8 and consists of three main stages viz., input, intermediate and the output stages. The input stage is a folded mirror type differential amplifier with an SCC whereas the output stages are class-AB and class-A types with floating bias architectures. As the output nodes of the input and intermediate stage are high impedance nodes, they introduce two low frequency poles. The load resistance R_L at the output node introduces a high frequency pole which is well beyond the unity-gain-bandwidth (UGB) of the op-amp. The R-C Miller compensation R_{C1} and C_{C1} is used to provide frequency stability to the op-amp. As the poles and zeros of SCC are well beyond the unity-gain-bandwidth (UGB) of the op-amps, it does not introduce any additional poles and zeros within the UGB of the op-amp. The bandwidth of the op-amp is determined by the pole of the input differential stage which is the dominant pole of the op-amp. The scheme I (Fig. 6), consists of three stages, input, intermediate and output stage. Two common source transistors M16, M17 are used to provide rail-to-rail output swing. The circuit shows four low frequency poles at the output of each gain stages. Three capacitors are connected to achieve a single low frequency pole at the output of the input stage and to move the other poles to frequencies higher than the UGB. R_{c1} R_{c2} and R_{c3} transform right half plane zeros into high frequency left half plane zeros. The scheme II, has a back to back source follower configuration operating in class-A mode two floating biases are implemented by using Switched Capacitor (SC) network. Two output transistors M12, M13 are connected in source follower configuration (Class-A). The limitation of this scheme is that it needs slightly more supply voltage compared with the previous scheme. The SC network composed of capacitors C1 to C4 (C1=C2 and C3=C4) and MOS switches S1 to S6 are used for performing dynamic biasing[13]. The switches are controlled by complementary clock phase $\phi 1$ and $\phi 2$. During $\phi 1$ the switches S1, S3, S5 are ON , C1 and C3 get charged. During clock phase $\phi 2$ switches S2, S4, S6 are ON resulting in charge sharing between C1, C2 and C3, C4.

In scheme III, the complete three stage op-amp with block diagram of NHD and PHD output stages is shown in Fig. 8. The transistors M_1 to M_{11} constitute the differential stage and intermediate stage. The SC network is used to properly bias the output drivers. V_x and V_y are the inputs to NHD and PHD respectively which form the output stage of op-amp. This output stage has an extremely low output resistance. Therefore the frequency of the pole formed by parasitic impedance at the output node is much higher than GBW of the op-amp. There are only two low frequency poles. A capacitor C_{c1} is connected between the output of the differential stage and output of the intermediate stage to achieve a single low frequency pole at the output of the input stage and to move the other pole to a frequency higher than the UGB. The resistor R_{c1} is connected to transform right half plane zero into high frequency left half plane zero. The op-amps thus designed have low output impedance, high drive capability and rail-to-rail output swing. This has been

achieved with a small increase in supply voltage and layout area. This scheme has both source follower and common source configuration combined in the same circuit operating in a true class-AB mode to achieve low output resistance as well as rail-to-rail swing.

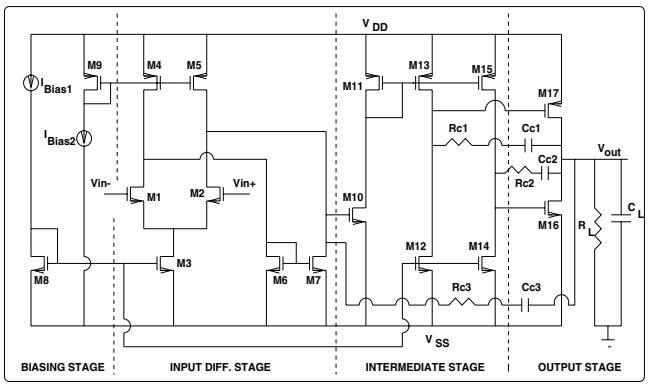

Fig. 6. Operational amplifier:Scheme 1

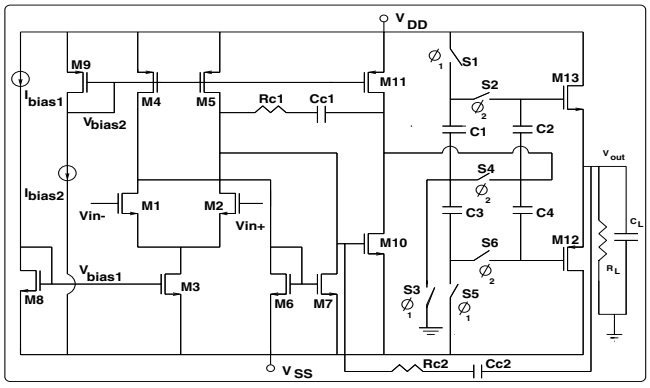

Fig. 7. Operational amplifier: Scheme 2

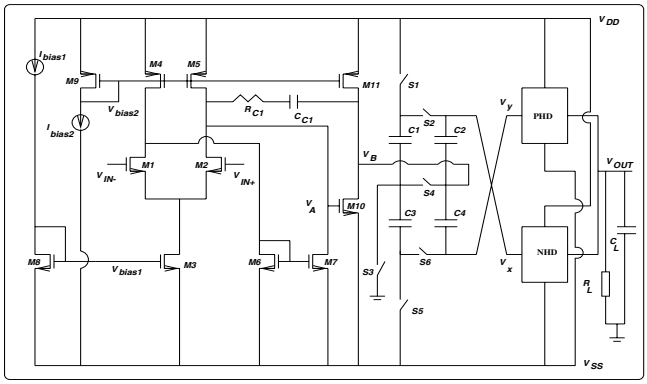

Fig. 8. Operational amplifier: Scheme 3

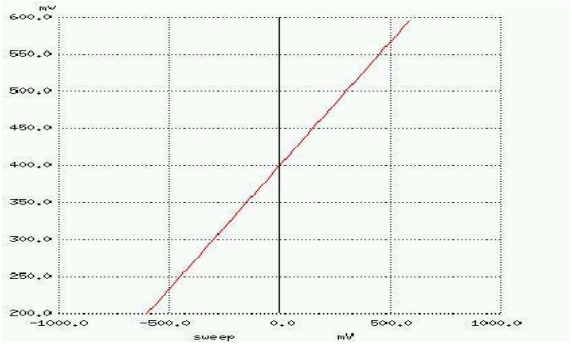

Fig. 9. DC transfer characteristic of SCC.

IV. **Simulation study**

Simulation study has been carried out by using SPICE with BSIM3v3 transistor model. A standard 0.5μm CMOS process with a nominal threshold voltage of around 0.7 V for both N and P channel transistors is considered. The supply voltages are set to $\pm$0.6 V and $\pm$0.75 V as indicated. The Table I gives the simulated performances. The clock is set to a frequency of 100kHz [4]. The DC transfer characteristic of SCC obtained (Fig. 9), shows that the input CM range of $\pm$0.6 V is converted at the output to a range of 200 mV (V_A) to 600 mV (V_{DD}) as designed. The transfer curve for the complete op-amps under unit follower configuration is shown in Fig. 10. From the figures, it may be noted that addition of SCC at the input of the differential stage extends the input CM range to 0.6 V.

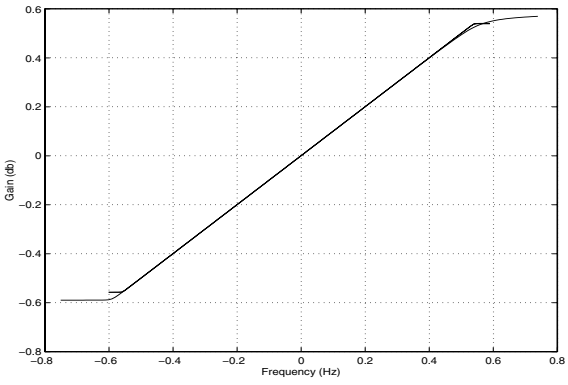

Fig. 10. DC transfer characteristics of op-amps under unity follower.

TABLE I

MEASURED MAIN PERFORMANCES

(At R_L=1k, C_L=10pf)

Parameters	Sch.1	Sch.2	Sch.3
A_{ol}	81 dB	71 dB	71 dB
GBW	1.2MHz	1.67MHz	1.67MHz
Phase margin	81.5 deg	81 deg	74 deg
CMRR	85.6dB	88dB	88dB
THD	-76 dB	-75 dB	-74 dB
Supply voltage	±0.6V	±0.75V	±0.75V
Output swing	±0.54V	±0.6V	±0.49V
Power dissi.	157.2 μw	196.8 μw	816 μw

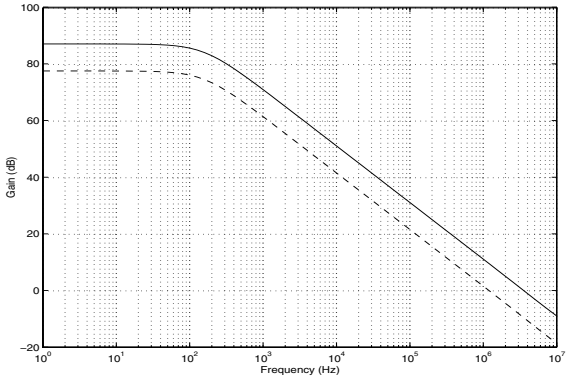

Fig. 11. Frequency response of scheme I with SCC.

Figs. 11-13 shows the frequency response of the complete op-amps. The frequency responses of the op-amps also shows that there is only one dominant pole within the GBW (Gain Band Width) and this ensures that the circuits are stable [14].

V. Conclusion

In this paper, a SCC, and a new floating bias for extending input CM voltage range and the output swing to rail-to-rail supply respectively are described . A detailed study on the working of op-amp with the proposed input/output circuit is carried out using CMOS devices with a dual supply of ±0.6 V and ±0.75 V. The introduction of SCC and floating bias at the output enhances the ICMR and output swing respectively. This requires an additional chip area but the circuit is stable and suitable for achieving large output swing. Further, the distortion, output swing and CMMR are evaluated and found to be in close agreement with other op-amps reported in the literature.

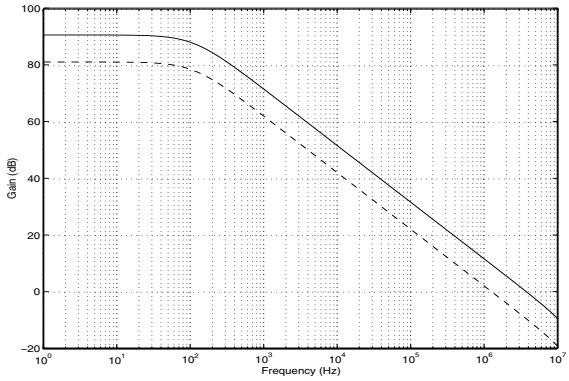

Fig. 12. Frequency response of scheme II with SCC.

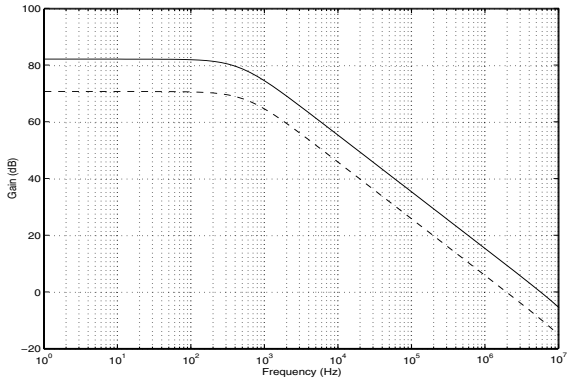

Fig. 13. Frequency response of scheme III with SCC.

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