SIMULATION OF ALL-DIGITAL DPSK MODEMS AND SYNCHRONIZERS

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Abstract: Bit error rate (BER), effects of synchronizer performance on demodulator, performance of demodulator under impulsive noise, Block error rate (BKER) are some of the important aspects of a Modem. To obtain quantitative data on all these aspects by mathematical analysis is usually very difficult. Hence, computer simulation is used to study Modems. This enables us to evaluate different circuit configurations, to understand their relative performances and to choose appropriate schemes for hardware realization of the Modem.

In this paper various aspects of a computer program for simulating a DPSK Modem and the results of the simulation are presented. It is shown that the simulation is, indeed, very flexible and a useful tool in designing Modems.

1. Introduction:

For realizing single chip or chip set Modems it is important to realize modulators, demodulators, symbol synchronizers and other interface circuits in all-digital form. This calls for obtaining new configurations for these circuits based on processing of the various signals, as far as possible, digitally. Of the many modulation schemes used, DPSK is an important scheme used in many Modems. Several configurations, leading to all-digital realizations, have been suggested for various parts of the DPSK Modem [1, 2]. Mathematical analysis to obtain bit error rates (BER) of many of these schemes leads to complicated mathematical expressions of limited validity [3, 4].

In this context computer simulation of the Modems becomes very attractive. This technique may be used to study the Modem and obtain the BER performance, synchronizer performance and effects of synchronizer on BER of the Modem etc. The simulation also may be used to verify the mathematical analysis of the Modem circuits.

In this paper simulation of all-digital DPSK Modem and synchronizers and the the results thereof, are presented. It is shown that such a simulation simplifies selection of appropriate schemes for realization of Modem circuitry.

2. Modular program for simulation of DPSK Modems:

Fig. 1 shows the block schematic of the DPSK Modem used for simulation. Here, the modulator, various filters, demodulator, synchronizer are realized using only digital circuits [1]. Moreover, data generation, noise generation, error analysis etc. are also to be realized by the simulation program.

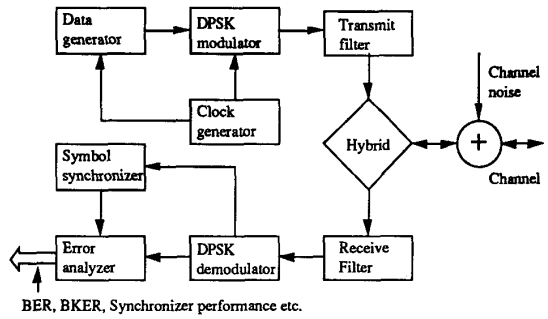

Fig. 1: DPSK Modem block diagram used for simulation

The following conditions are used for the simulation:

Bit rate: 200 bits/sec.

Carrier frequency: 800 Hz., 2 level DPSK modulated with differential phase shifts of 0 and π radians for data 0 and 1, respectively.

Clock used for sampling the polarity signal: 128 X 200 Hz (25, 600 Hz).

Filter for the DPSK receiver: Bandwidth: 200 Hz centred around 800 Hz (ideal band-pass assumed), realized as a 128 tap transversal filter.

Noise source: Gaussian distribution, filtered with the above ideal band pass filter.

Number of bits used for simulation at each SNR: 10, 000

The program is modular following the classical top-down approach. It is flexible enough to introduce other modulation, demodulation and synchronizer schemes into the simulation program. Fig. 2 shows the hierarchy chart of the program.

The program, written in FORTRAN 77, functions as follows: All activities of the Modem are considered to take place at discrete time instants $n.t_s$, where n is a running integer and t_s is the sampling time, with $f_s = \frac{1}{t_s}$, as the sampling frequency. f_s is also referred to as the master clock frequency. This is the frequency with which all other waveforms are derived in the Modem. The system simulation takes place at each clock pulse of this master clock. One transversal through the main program corresponds to one clock tick of the master clock. Each data bit processed through the simulation program requires a large number of this master clock ticks (128 ticks for the conditions given above). At the end of the program execution, the main program prints various quantities of interest, in a suitable format.

Passage of 10, 000 data bits through the program to simulate the Modem at a given signal to noise ratio (SNR) is considered an optimum value. A smaller number of data bits will not yield reliable performance data and a larger number of data bits requires an excessive computation time.

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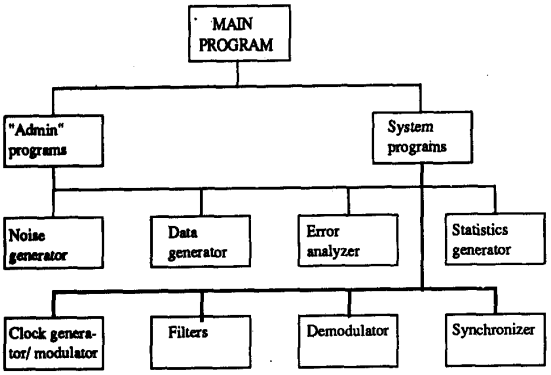

Fig.2: Hierarchy chart for DPSK Modem simulation

3. Program modules

The various modules in fig. 2 are described in this section.

3.1.The main routine

This routine consists of initialization of various program modules followed by a sequence of subroutine calls to the appropriate modules. The pseudo-code of the main routine is given below:

BEGIN DPSK Modem simulation

Initialize f_s, f_c (carrier frequency), f_b (data bit rate), range of SNR for simulation, no. of bits to be processed per SNR value.

CALL filter coefficient calculation routine

REPEAT

Initialize modulator, data generator, clock generator error rate and statistics collectors

REPEAT

CALL clock pulse generation routine

IF symbol clock is high CALL data generator routine

CALL DPSK modulator routine

CALL Noise generator and adder routine

CALL Filter routine

CALL DPSK demodulator routine

CALL Synchronizer routine

UNTIL all bits are processed

CALL Error count routine

CALL Statistics computation routine

PRINT simulation results for the current SNR

UNTIL simulation is carried out for all SNRs

END DPSK Modem simulation

Some of the important modules of the program are described below:

3.2. DPSK modulator:

For the 2-level DPSK signal the modulated signal is given by:

$s(t) = A.\ Cos\ (2\pi.f_c.t + \phi_i + d_k.\ \pi)$, where ϕ_i is an arbitrary initial phase of the carrier, d_k is the data bit (0 or 1).

This signal is generated by modulating a square wave at the carrier frequency and filtering it later by a transversal filter.

3.3: Receive Filter:

The SNR at the input of the demodulator is defined by the band-pass characteristics of the receive band-pass filter (BPF) and the inter-symbol-interference (ISI) is also controlled by it. Ideally, the receive BPF is assumed to be centred around the carrier frequency and to have a band width equal to the data bit rate with infinite amplitude fall-offs at the band edges. This filter can be approximately implemented and simulated by different methods. A transversal filter scheme is followed in this paper. Fig. 3 shows the BPF characteristics required.

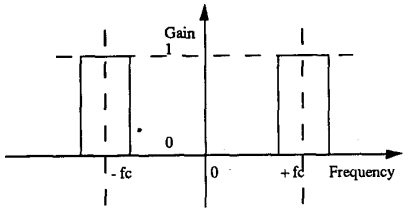

Fig. 3: Receive BPF characteristics

It can be shown that its impulse response of the filter of fig. 3, h(t), is given by the following expression [5].

$$h(t) = 2.f_b.\ Cos\ (2\pi.f_c.t).\frac{Sin\ (\pi.f_b.t)}{\pi.f_b.t} \qquad (4)$$

As time is discretized for simulation, at k th instant of time (4) can be written as,

$$h(k.t_s) = 2.f_b.\ Cos\ (2\pi.f_c.k.t_s).\frac{Sin\ (\pi.f_b.k.t_s)}{\pi.f_b.k.t_s}\ ,\ \text{but as}\ f_s = \frac{1}{t_s}$$

$$h(k.t_s) = \frac{2.f_s}{\pi.k}. \text{Cos}\ (2\pi.k.\frac{fc}{fs}). \text{Sin}\ (\pi.k.\frac{fb}{fs}) \qquad (5)$$

r(t), the output obtained by filtering s(t) with the above filter can be written in time domain as the following convolution integral:

$$r(t) = \int_{-\infty}^{+\infty} h(\tau).\ s(t - \tau)\ d\tau,$$ for discretized time this becomes:

$$r(k.\ t_s) = \sum_{p\ =\ -\infty}^{+\infty} s\{(k-p).t_s\}.h(p.ts).t_s \qquad (6)$$

This can be approximately implemented as a transversal filter, shown in fig. 4. This implementation, which calls for calculation of filter coefficients h(p.ts) and evaluation of (6) is used in the Modem simulation.

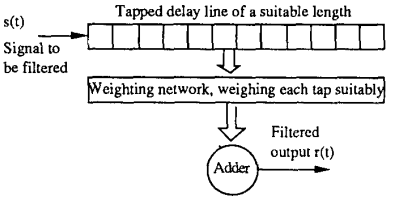

Fig. 4: Transversal filter

The closeness of the simulated filter to the ideal is determined by the number of taps used for the delay line. 128 taps are used in the simulation, which was found to be sufficient to simulate the ideal filter without unduly increasing the simulation time.

3.4: DPSK demodulator and Synchronizer:

DPSK demodulators used for simulation are described in [1], while synchronizers used are described in [6]. Various combinations of the modulator, demodulator and synchronizer are simulated to test their relative performance.

3.5: Error analyzer and Statistics collector:

This module counts the error occuring while the data bits are passed through the Modem. It compares the transmitted data with the received data on a bit-by-bit basis, by introducing the necessary delay to the transmitted data to take into account the demodulator delay.

At the end of the data run for any SNR, the statistics collector computes the symbol clock jitter, its probability density function (PDF) etc.

4. Simulation results:

The simulation program was run for values of SNR from -4 to 6 dB in steps of 2 dB. For control purposes, the program is also run for the ideal DPSK demodulator with ideal synchronization. Results of the simulation are shown in fig. 5.

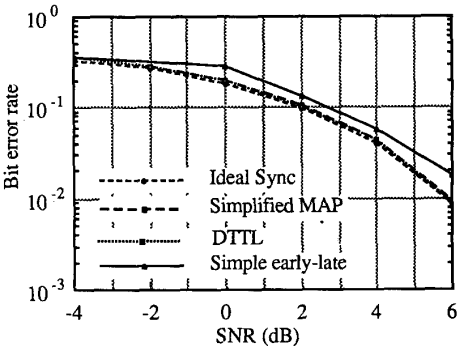

Fig. 5: BER Vs. SNR (simulation results)

Fig. 5 shows the BER degradation of the integrate-and-dump DPSK demodulator due to various synchronizers. From this it is clear that the simplified MAP and DTTL synchronizers perform much better than the simple early-late synchronizer.

5. Conclusions:

Computer simulation is a powerful technique to analyze complex circuitry used in Modems. In situations like the all-digital approach, mathematical analysis of the system is so complex that the simulation is about the only reasonable technique to analyze the system.

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