Circuits, Pebbling and Expressibility

(Extended Abstract)

V. Vinay* H. Venkateswaran† C.E. Veni Madhavan‡

1 Introduction

We give characterizations of nondeterministic complexity classes such as NP and PSPACE and the classes in the polynomial time hierarchy in the two-person pebble game model [VT89]. These characterizations motivate the definitions of these classes using first-order sentences extending the results in [Im82]. It is shown that the role-switches resource in the pebble games closely model the levels of the polynomial hierarchy. These characterizations are made possible by explicitly considering circuit-size in the pebbling characterizations and the size of the underlying universe in the first-order characterizations.

A dual interpreted game to model parallel computations was defined in [VT89]. They used this game to obtain characterizations of parallel complexity classes such as LOGCFL and AC^1. This paper carries this work further to obtain characterizations of the class NP and the classes in the polynomial-time hierarchy in the game model. A resource called *role-switches* was used in the dual game [VT89] to capture the difference between computations in the classes LOGCFL and AC^1. Subsequently, Borodin et al. [BCDRT89] showed that constant number of role-switches do not help when the underlying circuits have polynomial size. We show that role-switches model the alternating time hierarchy more accurately and thus their collapse implies the collapse of hierarchies such as the polynomial time hierarchy. Specifically, we show that the k-th level of the polynomial-time hierarchy uses $k-1$ role-switches. In this respect, it is very similar to a recent result in [JK88] that shows that for all $k \geq 1$, the k-th level of the polynomial-time hierarchy coincides with the $(k+1)$-st level of a certain alternating auxiliary pushdown hierarchy. To get our results, we generalize the dual game to consider both the size and the fan-in of the circuits on which the game is played. This makes it possible to extend the pebble game to exponential size circuits and unbounded fan-in circuits. The extended game provides a unified framework in which the earlier pebble game characterizations of the classes LOGCFL and AC^1 [VT89] and the new characterizations can be expressed.

We give a uniform first-order sentence characterization of NP and PSPACE. These are definitions over an exponential universe. The characterization of PSPACE here when compared with the one in [Im82] shows an interesting tradeoff between the size of the underlying universe and the size of a sentence. One of the objectives of this work was to explore the relationship between two-person pebble games and expressibility using first order sentences. These results suggest that the number of variables correspond to the number of pebbles and the size of the formula corresponds to pebbling time (rounds).

This work was motivated by the semi-unbounded fan-in circuit characterization of NP in [Ve88]. The results here illustrate the importance of the notion of semi-unboundedness. Semi-unbounded fan-in circuits (exponential fan-in for OR gates and polynomial fan-in for AND gates) of constant depth characterize NP whereas unbounded fan-in circuits of constant depth characterize classes in PH. Thus semi-unboundedness captures an essential difference between the computations in NP and PH. It is interesting to note that the circuit characterization of PH is one of the first uniform circuit characterizations of this very important complexity hierarchy. It may also be noted that the classes defined by constant depth semi-unbounded fan-in circuits (polyno-

*Department of Computer Science and Automation, Indian Institute of Science, Bangalore 560012, India.

†School of Information and Computer Science, Georgia Institute of Technology, Atlanta, Georgia 30332-0280. Most of this work was done while this author was at the Indian Institute of Science, Bangalore, India, on leave from the Georgia Institute of Technology.

‡Department of Computer Science and Automation, Indian Institute of Science, Bangalore 560012, India.

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mial fan-in *OR* gates and $\log n$ fan-in *AND* gates) and unbounded fan-in circuits (polynomial fan-in for both *OR* and *AND* gates) at the low-level are known to be different.

One of the contributions of this paper is that it shows the robustness of all the complexity classes which have very similar definitions in the models that we have considered, namely, Boolean circuits, pebble games and logic. They isolate some model-independent abstract properties that the computations in these classes seem to possess.

2 Game Characterizations

In this section, we present the characterizations of the class NP and the polynomial-time hierarchy using the dual interpreted game model of [VT89]. The game characterizations use uniform Boolean circuit definitions of NP and PH.

2.1 Definitions

Σ_k-Unbounded fan-in Boolean circuits: This is a family of unbounded fan-in circuits in which the output is an unbounded fan-in *OR* gate and along any path, from any circuit input to the output gate, no more than $k-1$ unbounded alternations occur. (Note that the gates that do not have unbounded fan-in have constant fan-in.) For $k = 1$, such a family of circuits will be called *semi-unbounded fan-in circuits.* We will assume that any circuit in this family can be divided into k distinct layers such that a gate v is in layer p iff the maximum number of unbounded alternations along any path from the output gate to v is $p-1$.

A family of **Π_k-Unbounded fan-in Boolean circuits** is defined in a dual fashion.

We will assume that the circuit families considered are all *U_D-uniform* [Ru81]. See the paper by Ruzzo [Ru81] for a definition of this uniformity notion.

Let SemiUnbounded USIZE,DEPTH $(Z(n), D(n))$ denote the class of languages accepted by a uniform family of semi-unbounded fan-in circuits with size $O(Z(n))$ and depth $O(D(n))$. The classes Unbounded USIZE,DEPTH $(Z(n), D(n))$ are defined similarly. We will also be interested in unbounded fan-in circuit families in which the *AND* gates have polynomial fan-in. Let Unbounded USIZE,DEPTH,AND $(Z(n), D(n), f(n))$ denote the class of languages accepted by a uniform family of unbounded fan-in circuits with size $O(Z(n))$, depth $O(D(n))$ and, in which, all *AND* gates have fan-in at most $f(n)$.

2.2 The dual interpreted two-person pebble game

This game, introduced in [VT89], is played by two players called *Player 0* and *Player 1* on the vertices of a *bounded fan-in* Boolean circuit G_n together with its input x. The objective of Player 0 (Player 1) is to establish that the output of the circuit evaluates to 0 (1). Thus, a pebble placement or challenge on a gate v by Player 0 (Player 1) corresponds to asserting that v evaluates to 0 (1). At any point, one of the players takes on the role of the Challenger and the other that of the Pebbler. The role of a player is automatically determined as part of the circuit information as follows. The gates in G_n are partitioned into two sets, those of "challenge type" 0 and those of "challenge type" 1. A challenge placed on a gate of challenge type 0 (challenge type 1) causes Player 0 (Player 1) to be the Challenger in the next round. It is assumed that this additional bit per vertex is available as part of the circuit description.

A challenge by Player 0 (Player 1) will be referred to as a 0-challenge (1-challenge). Similarly, a pebble placed by Player 0 (Player 1) will be referred to as a 0-pebble (1-pebble).

Rules: The initial challenge is on the output gate. The game proceeds in rounds with a round consisting of the following three parts. (a) If the game is not over at the currently challenged vertex u according to the conditions below, then Player 0 is the Challenger for this round if u is of challenge type 0 and the Pebbler otherwise. (b) In the *pebbling move*, the Pebbler picks up zero or more of its own pebbles from vertices already pebbled and places pebbles on any nonempty set of vertices. (c) In the *challenging move*, the Challenger either rechallenges the currently challenged vertex, or challenges one of the vertices that acquired a pebble in the current round.

Player 1 wins the game if, immediately following the Challenger's move, the current challenged vertex is an input with value 1, or an *OR* gate at least one of whose immediate predecessors is 1-pebbled, or an *AND* gate all of whose immediate predecessors are 1-pebbled. Player 0 wins if, immediately following the Challenger's move, the current challenged vertex is

an input with value 0, or an *OR* gate all of whose immediate predecessors are 0-pebbled, or an *AND* gate at least one of whose immediate predecessors is 0-pebbled. The winner in an infinite play of the game is the player who has been the Pebbler for only finitely many rounds.

Resources: The four resources of interest in a play of this game are: *space, time, rounds,* and *role switches.*

The game on a circuit G_n with input $x \in L$ of length n is said to use space $p(n)$ (time $t(n)$, rounds $r(n)$, role switches $s(n)$ resp.) if and only if there is a strategy for Player 1 such that, for all plays by Player 0, Player 1 wins using at most $p(n)$ 1-pebbles ($t(n)$ 1-pebble placements, $r(n)$ rounds in which Player 1 is the Pebbler, $s(n)$ role switches between pebbling and challenging roles resp.). Resources when $x \notin L$ are defined by interchanging Player 0 and Player 1. A circuit G_n with input x is said to be *pebbleable* in space $p(n)$,time $t(n)$, rounds $r(n)$, role switches $s(n)$ if the winner has a winning strategy using no more than $p(n)$ pebbles, $t(n)$ pebble placements, $r(n)$ alternations between the players and $s(n)$ role-switches between the pebbling and challenging roles. Note that only the winner's resources are counted.

2.3 Extensions to the dual interpreted game

We now consider extensions of the dual interpreted game to facilitate playing the game on Bolean circuits that have exponential size and/or unbounded fan-in.

To extend the game to exponential size circuits, we introduce a purely syntactic parameter called *weight.* For our results here, the weight of a pebble is $O(\log Z(n))$, where $Z(n)$ is the size of the circuit on which the pebble game is played. This helps to distinguish between complexity classes which have otherwise the same pebbling resource characteristics.

For playing the dual interpreted game on unbounded fan-in circuits, we will first introduce a simple rule about challenge types of gates that is sufficient for the purposes of this paper.

Rule (*): Any unbounded fan-in *OR* (*AND*) gate is of challenge type 0 (1).

The modifications needed to extend the game to unbounded fan-in Boolean circuits are reflected in the way resources are counted. For this purpose, we consider two possibilities. One possibility is to use rule (**) below. This is motivated by the observation that a gate with fan-in f can be regarded, for our purposes, as a bounded fan-in circuit of depth $\log f$.

Rule (**): If the game is lost at an unbounded fan-in gate, the pebbler of that round is charged $\log\log f$ rounds and time, where f is the fan-in of that gate.

The other possibility is to not use this rule. In other words, the resources for playing the game on bounded fan-in Boolean circuits and unbounded fan-in Boolean circuits are treated the same way. We will refer to this as the *unit-cost* game model.

These two variations on counting resources lead to two different pebble game characterizations of NP and PH.

2.4 The Characterization Results

Let $\Sigma(\Pi)-\text{PB,RND,SW,WT}(p(n), r(n), s(n), w(n))$ be the class of languages L accepted by a uniform family $\{G_n\}$ of Boolean circuits of size $2^{O(w(n))}$, wherein Player 1 (Player 0) begins the game as the Pebbler, and such that G_n is pebbleable in $p(n)$ pebbles, $r(n)$ rounds, and $s(n)$ role switches.

Let
$U\Sigma\ (U\Pi)-\text{PB,RND,SW,WT}(p(n), r(n), s(n), w(n))$ be the class of languages L accepted by a uniform family $\{G_n\}$ of Boolean circuits of size $2^{O(w(n))}$, wherein Player 1 (Player 0) begins the game as the Pebbler, and such that G_n is pebbleable in $p(n)$ pebbles, $r(n)$ rounds and $s(n)$ role switches in the unit-cost model.

Note: The classes are defined in terms of rounds rather than time. This seems more natural when non-constant pebbles are used. In the case when constant pebbles are used, it is easy to see that the number of rounds and the time differ only by a constant factor.

We drop the $\Sigma(\Pi)$ prefix if either player can begin the game as the Pebbler.

Theorem 1 below follows from corollaries 5, 7, 10, 12, 14 and 15 below.

Theorem 1 *1.*
$\text{NP} = \Sigma-\text{PB,RND,SW,WT}(O(1), \log n, 0, n^{O(1)})$.

2. $\text{NP} =$
$U\Sigma-\text{PB,RND,SW,WT}(n^{O(1)}, O(1), 0, n^{O(1)})$.

3. $\Sigma_k^p =$
$\Sigma-\text{PB,RND,SW,WT}(O(1), \log n, k-1, n^{O(1)})$.

4. $\text{LOGCFL} =$
$\Sigma-\text{PB,RND,SW,WT}(O(1), O(\log n), 0, O(\log n))$.

5. AC^1 =
Σ –
PB,RND,SW,WT$(O(1), O(\log n), O(\log n), O(\log n))$.

The pebbling characterization of PH in theorem 1 above should be contrasted with the results in [BCDRT89] where they show that constant role-switches may not help when polynomial size circuits are considered.

It is interesting to look at other classes defined by uniform families of exponential circuits that are not constant depth. Thus, for instance, we can define NAC^1 to be the class of languages recognized by alternating Turing machines in polynomial space and alternation depth $O(\log n)$. By a result of Cook and Ruzzo [Co85], this class is equivalent to the class of languages accepted by uniform families of unbounded fan-in circuits of size $2^{n^{O(1)}}$ and depth $O(\log n)$. This class which is contained in PSPACE is interesting because it contains NP and is closed under complement. A pebbling characterization of NAC^1 is given in theorem 2 below whose proof follows from corollaries 12 and 14.

Theorem 2
NAC^1 = PB,RND,SW,WT$(O(1), \log n, \log n, n^{O(1)})$.

Finally, a pebbling characterization of PSPACE is given in theorem 3 below whose proof follows from corollaries 5 and 14.

Theorem 3 PSPACE = PB,WT$(O(1), n^{O(1)})$.

2.5 Pebbling Semi-Unbounded Fan-in Circuits

Pebble games on semi-unbounded fan-in circuits are interesting because many natural complexity classes have definitions using semi-unbounded fan-in circuits [Ve87, Ve88]:

Facts:
LOGCFL = SemiUnbounded USIZE,DEPTH $(n^{O(1)}, \log n)$.

NP = SemiUnbounded USIZE,DEPTH $(2^{n^{O(1)}}, \log n)$.
NP =
Unbounded USIZE,DEPTH,AND $(2^{n^{O(1)}}, O(1), n^{O(1)})$.
P = SemiUnbounded USIZE,DEPTH $(n^{O(1)}, n^{O(1)})$.
PSPACE =
SemiUnbounded USIZE,DEPTH $(2^{n^{O(1)}}, n^{O(1)})$.

Considering a general semi-unbounded fan-in circuit family of size $Z(n)$ and depth $D(n)$, we have the following result:

Theorem 4
SemiUnbounded USIZE,DEPTH $(Z(n), D(n)) \subseteq$
Σ – PB,RND,SW,WT
$(O(1), \max(\log\log Z(n), D(n)), 0, \log Z(n))$.

Proof Sketch: We use the following definition of NP: SemiUnbounded USIZE,DEPTH $(2^{n^{O(1)}}, \log n)$. All gates in the circuit have challenge type 0. Let the circuit evaluate to 1 on the given input. Consider a depth-first pebbling of a proof in the circuit. Since the *AND* gates are bounded, by Rule (**), the time taken by Player 1 to pebble the circuit would be no more than $\max(\log\log Z(n), D(n))$ using a constant number of pebbles. If the circuit evaluates to 0, the Player 0 wins without using any resources. □

Considering unbounded fan-in circuits in which the *OR* gates are restricted to have bounded fan-in, it is straightforward to prove a dual version of theorem 4 above. So, we have the following corollaries:

Corollary 5 *1.* LOGCFL $\subseteq$
Σ – PB,RND,SW,WT$(O(1), O(\log n), 0, O(\log n))$.

2. NP $\subseteq$
Σ – PB,RND,SW,WT$(O(1), O(\log n), 0, n^{O(1)})$.

3. CONP $\subseteq$
Π – PB,RND,SW,WT$(O(1), O(\log n), 0, n^{O(1)})$.

4. PSPACE $\subseteq$
Σ – PB,RND,SW,WT$(O(1), n^{O(1)}, 0, n^{O(1)})$.

5. P $\subseteq$
Σ – PB,RND,SW,WT$(O(1), n^{O(1)}, 0, O(\log n))$.

To obtain an alternative pebbleing characterization of NP, we have the following theorem:

Theorem 6
Unbounded USIZE,DEPTH,AND $(Z(n), D(n), f(n)) \subseteq$
UΣ – PB,RND,SW,WT$(f(n), D(n), 0, \log Z(n))$.

Proof Sketch: The proof is similar to that of theorem 4, when the following definition of NP is used:
Unbounded USIZE,DEPTH,AND $(2^{n^{O(1)}}, O(1), n^{O(1)})$,
All gates in the circuit have challenge type 0. Let the circuit evaluate to 1 on the given input. Consider a depth-first pebbling of a proof in the circuit. Player 1 can win the game using at most $f(n)$ pebbles in $D(n)$ rounds since the *AND* gates have fan-in at most $f(n)$. If the circuit evaluates to 0, the Player 0 wins without using any resources. □

This theorem yields the following corollary:

Corollary 7 NP $\subseteq$
$U\Sigma$ – PB,RND,SW,WT$(n^{O(1)}, O(1), 0, n^{O(1)})$.

To obtain a pebbling characterization of the polynomial-time hierarchy, we begin with a uniform Boolean circuit characterization of the polynomial-time hierarchy.

Theorem 8 Σ_k^P =
Σ_k – Unbounded USIZE,DEPTH $(2^{n^{O(1)}}, \log n)$.

Proof Sketch: Let L be a language in Σ_2^P and M be an NP machine with an NP oracle that accepts L. We will assume that M makes an oracle query only once along a computation path. Using the circuit characterization of NP in terms of uniform Σ_1-Unbounded fan-in circuits and CONP in terms of Π_1-Unbounded fan-in circuits, we can combine them to obtain a two-layered circuit that simulates M.

In the other direction, a uniform Σ_2-Unbounded fan-in circuit of size $2^{n^{O(1)}}$ and depth $O(\log n)$ can be evaluated by an NP machine M with an NP oracle as follows: M existentially guesses a proof in the circuit till it reaches an unbounded *AND* gate at which point it will simulate a CONP machine to verify that this *AND* gate is accepting.□

The resources for playing the pebble game on the circuits defining PH is given by the following theorem:

Theorem 9
Σ_k – Unbounded USIZE,DEPTH $(Z(n), D(n))$ $\subseteq$
Σ – PB,RND,SW,WT
$(O(1), \max(\log\log Z(n), D(n)), k-1, \log Z(n))$.

Proof sketch: It is clear that only odd (even) numbered layers have unbounded fan-in *OR*(*AND*, respectively) gates. Since all gates in the odd (even) numbered layers are assigned challenge type 0 (challenge type 1, resp.), the game can be confined to one layer using $O(1)$ pebbles and $k-1$ role-switches. Since any one layer is a semi-unbounded fan-in circuit or its dual, the result follows.□

Corollary 10 Σ_k^P $\subseteq$
Σ – PB,RND,SW,WT$(O(1), O(\log n), k-1, n^{O(1)})$.

2.6 Pebbling Unbounded Fan-in Circuits

Considering unbounded fan-in circuits, we can prove the following analog of theorem 4:

Theorem 11
Unbounded USIZE,DEPTH $(Z(n), D(n))$ $\subseteq$
Σ – PB,RND,SW,WT
$(O(1), \max(\log\log Z(n), D(n)), D(n), \log Z(n))$.

The following two corollaries of this theorem are now immediate:

Corollary 12 *1.* AC^1 $\subseteq$
Σ –
PB,RND,SW,WT$(O(1), O(\log n), O(\log n), O(\log n))$.

2. NAC^1 $\subseteq$
Σ –
PB,RND,SW,WT$(O(1), O(\log n), O(\log n), n^{O(1)})$.

2.7 Simulating the Game by an Alternating Turing Machine

The following theorem, which gives the resources used by an alternating Turing machine to simulate the game, generalizes theorem 11 in [VT89] and can be proved by slightly modifying the proof of that theorem.

Theorem 13 If L is accepted by a uniform family $\{G_n\}$ of bounded fan-in circuits of size $Z(n)$ such that G_n is pebbleable in p pebbles, t time, and r rounds in the dual game, then L is accepted by an alternating Turing machine within space $O(p \cdot w(n))$, time $O(\max(t \cdot w(n), w(n) \cdot \log w(n))$ and alternations $O(\max(r, \log w(n))$. Here, $w(n)$ is taken to be $\log Z(n)$. If, in addition, Player 1 is always the Pebbler, then L is accepted within space $O(p \cdot w(n))$ and tree-size $\max(w^2(n), p^{O(r)})$.

Proof Sketch: The proof is analaogous to that of theorem 11 in [VT89]. Recall now that the direct connection language of the circuits involved can be recognized in time $O(w(n))$ by a deterministic Turing machine, since the circuits are U_D-uniform. But, this can be simulated by an alternating Turing machine with space $O(w(n))$, time $O(w(n) \cdot \log w(n))$, alternations $O(\log w(n))$ and tree-size $O(w^2(n))$.□

The following corollaries now follow from known relationships.

Corollary 14 *1.*
Σ – PB,RND,SW,WT$(O(1), O(\log n), 0, O(\log n))$
$\subseteq$ LOGCFL.

2. Σ – PB,RND,SW,WT$(O(1), O(\log n), 0, n^{O(1)})$
$\subseteq$ NP.

3. $\mathrm{U}\Sigma$ – PB,RND,SW,WT$(n^{O(1)}, O(1), 0, n^{O(1)})$ $\subseteq$ NP.

4. Π – PB,RND,SW,WT$(O(1), O(\log n), 0, n^{O(1)})$ $\subseteq$ CONP.

5. Σ – PB,RND,SW,WT$(O(1), O(\log n), O(\log n), O(\log n))$ $\subseteq$ AC^1.

6. Σ – PB,RND,SW,WT$(O(1), O(\log n), O(\log n), n^{O(1)})$ $\subseteq$ NAC^1.

The simulation of a $k-1$ role switch game in exponential size circuits by a Σ_k^P machine is captured by the following corollary.

Corollary 15 Σ – PB,RND,SW,WT$(O(1), O(\log n), k-1, n^{O(1)})$ $\subseteq$ Σ_k^P.

Proof sketch: We show this for $k = 2$. An NP machine can simulate the game until a role-switch occurs. When the role switch does occur, Player 0 becomes the Pebbler and there are no more role switches. The outcome of the game, given its current configuration, can thus be determined by an NP oracle.□

Remarks: It is straightforward to give a pebbling characterization of the polynomial-time hierarchy in the unit-cost game model analogous to such a characterization of the class NP (see theorem 1). Such a characterization is possible because PH can be characterized as Unbounded USIZE,DEPTH $(2^{n^{O(1)}}, O(1))$. It is also not too difficult to define uniform AC^0 in the pebble game model. The details will appear in the full version of this paper.

3 Logic Characterizations

The main result in this section is the characterization of NP using first order sentences. In [Im82], two resources on first order sentences, namely variables and size were introduced to obtain characterizations of simultaneous resource bounded classes. In [Im81, Im82, Im87], it is assumed that all variables carry no more than $\log n$ bits of information. Motivated by the results in the previous section, we introduce variables which carry $w(n) \geq \log n$ bits of information.

We also define uniformity for first order sentences by introducing the notion of a direct connection language analogous to those for Boolean circuits [Ru81]. All the symbols in the formula are indexed and since a variable may occur in more than one place, the index distinguishes them. Note that not more than $\log Z(n)$ bits are necessary to index a formula with at most $Z(n)$ symbols. Queries such as, "Is variable v at position p universally quantified?" can all be answered by the uniformity machine. In the case where constant number of variables are used, the syntactic uniformity from [Im82] can also be used.

3.1 The Characterization results

Let VAR,SIZE,WT$(V(n), Z(n), W(n))$ denote a sequence of uniform first order sentences $\{F_n\}$ where F_n has $V(n)$ variables, $O(Z(n))$ symbols and the quantifiers range over a universe whose cardinality is $2^{O(W(n))}$. Let VAR,SIZE,WT $(B\forall)(V(n), Z(n), W(n))$ be defined as above except that now the universal quantifiers range over a Boolean universe.

We prove the following theorems whose proofs follow from corollaries 18, 20 and 22.

Theorem 16 *1.* NP = VAR,SIZE,WT $(B\forall)(O(1), O(\log n), n^{O(1)})$.

2. PSPACE = VAR,SIZE,WT$(O(1), n^{O(1)}, n^{O(1)})$.

The characterization of PSPACE by Immerman [Im82], when phrased using the weight resource would be VAR,SIZE,WT$(O(1), 2^{n^{O(1)}}, \log n)$. Thus these two characterizations of PSPACE provide a weight-size tradeoff.

The characterization results above will be proved by relating first order expressibility to alternating Turing machine resources.

Theorem 17 For $W(n) \geq \log n$, $S(n) \geq \log n$, ASPACE,TREESIZE$(S(n), Z(n))$ $\subseteq$ VAR,SIZE,WT $(B\forall)(O(\frac{S(n)}{W(n)}), \frac{S(n)}{W(n)} \cdot \log Z(n), W(n))$.

Proof: The proof is adapted from the second inclusion in theorem B.1 of [Im82] with modifications needed to accomodate the weight resource. The space used by the machine is $S(n)$ and every variable contains $W(n)$ bits of information. Hence, no more than $O(\frac{S(n)}{W(n)})$ variables are needed to code any configuration. The size of the sentences will be $O(\frac{S(n)}{W(n)} \cdot \log Z(n))$. □

Corollary 18 *1.* LOGCFL $\subseteq$ VAR,SIZE,WT $(B\forall)(O(1), O(\log n), O(\log n))$.

2. NP $\subseteq$ VAR,SIZE,WT $(B\forall)((O(1), O(\log n), n^{O(1)})$.

To characterize PSPACE we consider the relationship between first order expressibility and time bounded alternating Turing machines. In one direction, we have the following theorem. We omit the easy proof.

Theorem 19 For $W(n) \geq \log n$, $S(n) \geq \log n$,

ASPACE,TIME$((,S)(n), T(n)) \subseteq$ VAR,SIZE,WT$(O(\frac{S(n)}{W(n)}), T(n), W(n))$.

Corollary 20 *1.* P $\subseteq$ VAR,SIZE,WT$(O(1), n^{O(1)}, O(\log n))$.

2. PSPACE $\subseteq$ VAR,SIZE,WT$(O(1), n^{O(1)}, n^{O(1)})$.

The containments in the other direction follow from the theorem below whose proof is omitted from this extended abstract.

Theorem 21 If L is expressible by a uniform family of senetences $\{F_n\}$ that uses $V(n)$ variables, $T(n)$ size and $W(n)$ weight, then L is accepted by an alternating Turing machine within space $O(V(n) \cdot W(n))$ and time $O(T(n) \cdot W(n))$. If, in addition, the universal quanifiers are Boolean, then L is accepted by such a machine with treesize $c^{T(n)}$ for some constant c.

Corollary 22 *1.* VAR,SIZE,WT $(B\forall)(O(1), O(\log n), O(\log n))$ $\subseteq$ LOGCFL.

2. VAR,SIZE,WT $(B\forall)(O(1), O(\log n), n^{O(1)})$ $\subseteq$ NP.

3. VAR,SIZE,WT$(O(1), n^{O(1)}, O(\log n))$ $\subseteq$ P.

4. VAR,SIZE,WT$((O(1), n^{O(1)}, n^{O(1)})$ $\subseteq$ PSPACE.

4 Open Problems

We will conclude by stating some open problems.

- Do role switches in two-person pebble games help? It is known that for certain polynomial size circuit hierarchies constant number of role switches do not help. But, our characterization of PH in terms of role switches suggest that taking weight into consideration may alter this situation. It would also be quite interesting to identify circuits for natural problems for which role switches help.
- The circuit characterization of complexity classes suggests the definition of new classes. We defined one such class NAC^1 that seemed like a good analog of AC^1. An interesting question here is to identify natural complete problems for this and other such classes. In this connection, it is worth mentioning that Chandra and Tompa [CT88] have shown that a class of short two-person games are complete for AC^1. These problems may suggest similar problems complete for NAC^1.
- Semi-unboundedness versus unboundedness: Semi-unboundedness seems like a useful concept to capture the computations in many natural complexity classes [Ve88]. An important question in this area concerns the relationship between this notion and that of unboundedness. For instance, in the uniform Boolean circuit model, this may shed light on the relationship between NP and PH.
- First order expressibility versus second order expressibility: It is well known that NP is identical with the class of second order existential formulas [Fa74]. What is the link between the first order characterization of NP in this paper and second order formulas?
- Tradeoffs between weight and size: We have exhibited a weight and size tradeoff in the first order characterizations of PSPACE. What are some general tradeoff relations between weight and size?

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