ALL-DIGITAL SYNCHRONIZERS FOR DPSK DEMODULATORS

H.S. Jamadagni, B.S. Sonde, A.V. Shah[1]

Abstract:

Bit synchronization is an important operation used at the receiving end of synchronous communication systems for providing a reference bit clock to the receiver; this reference marks the instants at which transition in data bits occur at the transmitting end. In some DPSK demodulator realizations, like the integrate-and-dump scheme, the bit clock is essential for data recovery itself. But in most demodulators the bit clock is required just for "cleaning up" the demodulated data and to provide an output with uniform data widths. Generally this is done by sampling the demodulator output (called the "raw data") with another clock, which is in phase opposition with respect to the bit clock. Instants at which the bit clock transitions have to occur at the receiver and which are not a prwri known to the receiver, are usually estimated based on transitions of the received data. Such estimators are commonly realized as phase locked loops (PLL) with data transitions as reference input. In the presence of noise in the communication channel, transitions of bit clock waveform produced by the receiver synchronizer do not occur at exactly uniform intervals, but will have a random fluctuation, called the jitter, associated with them. Hence, cleaning up the demodulator output with the bit clock introduces some additional errors into the demodulated data and thus degrades the bit-error rate (BER) performance of the demodulator.

In this paper, Maimurn-A Posteriori (MAP) and Data Transition Tracking Loop (DTTL) synchronizers are developed for the DPSK scheme. In their original form, these synchronizers require substantial hardware for their realization. By some simplifications, hardware complexity is considerably reduced and simplified "all-digital" MAP and DlTL synchronizers are suggested. The hardware needed to realize these schemes is not significantly more than that required for the simple early-late scheme, Results of computer simulation studies on all-digital MAP and DlTL synchronizers are given. They not only indicate that the degradation in the BER perjormance of the demodulator due to these synchronizers is about 02 dB, as compared to 1 to 2 dB for the simple early-late scheme, but also that the MAP and DlTL schemes have much lower jitter. Results of an experimental study on microprocessor-based hardware realizations of the synchronizers are given. The circuits developed are suitable for the realization of a digital IC for synchronization as well as in DPSK Modems.

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1. Introduction:

Bit synchronization is an important operation used at the receiving end of a synchronous communication system for providing a reference bit clock to the receiver. This bit clock marks the instants at which transition in data bits occur at the transmitting end. Differential Phase Shift Keying (DPSK) is currently used in many commercial synchronous Modems and the bit synchronization circuit is a substantial part of them. In some DPSK demodulator realizations, like the integrate-and-dump (IAD) scheme shown in Fig. 1, the bit clock is essential for data recovery itself. But in most demodulators the bit clock is required for just cleaning up the demodulated data and to provide an output with uniform data widths. As shown in Fig. 1, this is generally done by sampling the demodulator output (called the "raw data") with another clock, which is in phase opposition with the bit clock. The timing relationships in the demodulator and the synchronizer are shown in Fig. 2.

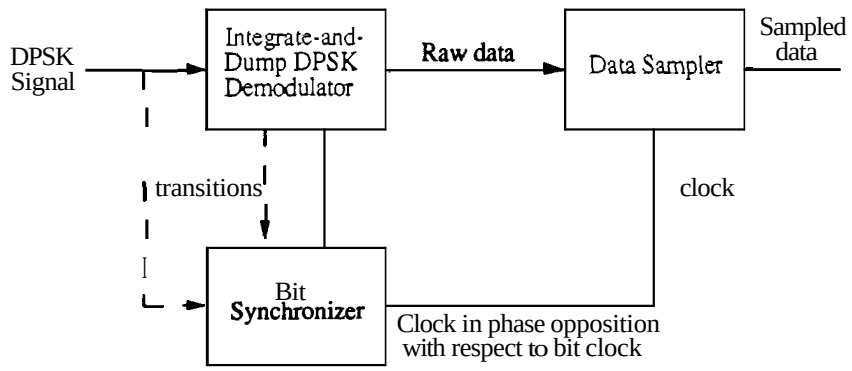

Fig. 1: DPSK demodulator and bit synchronizer

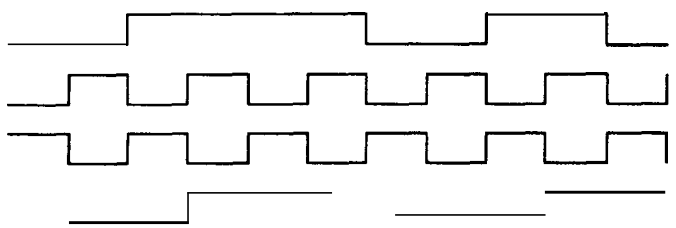

Fig. 2: Synchronizer waveforms

Although many Modems are now available in a single chip or a chip set form, the

synchronization used in them is not indicated [1, 2]. We presume that simple early-late synchronization or variations thereof are used [9]. Moreover, no data is given on demodulator **BER** degradation due to these synchronizers and on jitter performance.

In the following sections, the MAP estimator topology is used to develop synchronizer schemes for the **DPSK** scheme. These schemes *are* further simplified so as to yield practical, easy to realize, all-digital synchronization circuits. It is shown that these simple schemes perform nearly as well as the ideal MAP scheme, the **BER** performance degradation due to them being about 0.2 dB. It is also shown that the hardware required for their realization is not substantially more than that for the simple early-late synchronizer.

Let ε be the modulation instants, unknown to the receiver, repeating at every bit clock interval T sec. Given the data bearing **DPSK** signal $v(t)$, the synchronization problem is to estimate ε based on $v(t)$. The estimated value of ε, denoted by ε', must be as close to ε as possible. However, when the data bearing **DPSK** signal is corrupted by noise, ε' differs from ε by an amount $(\varepsilon-\varepsilon')$. This is the error in estimation of ε and it should be minimized.

In Maximum A Posteriori **(MAP)** estimation, ε is considered to be a random variable taking a value in the range $\frac{-T}{2}$ to $\frac{+T}{2}$ and its probability density function **(PDF)** is assumed to be conditioned **on** $v(t)$. Then, estimating ε involves choosing ε' such that, this conditional **PDF** is maximized, which in turn minimizes the error $(\varepsilon-\varepsilon')$[3]. In Maximum Likelihood (ML) estimation, ε is assumed to be an unknown constant in the range $\frac{-T}{2}$ to $\frac{+T}{2}$ and ε is then estimated, again **based** on $v(t)$. If ε is assumed to be uniformly distributed in the range $\frac{\pm T}{2}$, then MAP and ML estimation techniques lead to the same estimator topology [4].

2. MAP **estimator** for the **DPSK scheme:**

Fig. 3 shows the received **DPSK** signal $v(t)$ over a duration of τ sec., during which estimation of ε is carried out. τ is called the estimation time and is assumed to be an integral multiple of T (τ = NT, N **an** integer). Here, $v(t)$ is assumed to be made up of sinusoidal waveshapes, with instantaneous differential phase modulations every T sec. For simplicity of analysis only 2-level modulation is assumed. The instant at which the estimation is **started** is the reference time 0. For estimating ε, the signal is observed from that instant onwards for τ seconds.

Signal $v(t)$ to the synchronizer can be written as, $v(t) = s(t\,;\varepsilon) + z(t)$ (1)

where, s(t ; ε) is the **DPSK** signal component and z(t) is the noise component. The noise introduced by the channel is assumed to be white Gaussian. z(t) is the channel noise filtered at the receiver with a band pass filter with a band width of **B Hz.,** where **B** is the bit rate (in bits per **sec., BPS).** z(t) is assumed to have a **zero** mean and a variance of σ_z^2.

Let N+1 bits, numbered 0 to N be observed for estimating the bit clock. (From fig. 3, it is to be noted that out of (N + 1) bits that **are** actually observed during the **period** τ, the 0 th and the N th bits **are** only partially observed and hence yield only partial information for estimating ε). Then the k th interval of the input signal is given by:

$(k - 1)T + \varepsilon < t \leq k.T + \varepsilon$ and $0 < t \leq N.T$, **as** $\tau = NT$.

For the k **th** interval, the **DPSK** signal can be written **as,**

$$s(t ; k, \varepsilon) = g\{t - (k-1).T - \varepsilon\}. \text{Cos}\{\omega_c (t - \varepsilon) + \phi_{nk}\} \qquad (2)$$

Here, ϕ_{nk} is the differential phase modulation during the **k** *interval. $g\{t - (k-1).T - \varepsilon\}$ is the base-band pulse waveform defined in the interval $(k - 1).T + \varepsilon < t < k.T + \varepsilon$: The base-band waveform **has** the desired wave shape in this interval and is **zero** elsewhere.

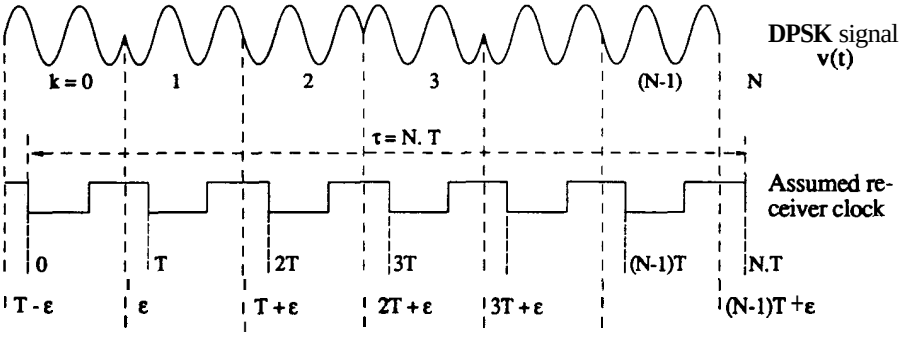

Fig. 3. **DPSK** signal **used** for estimation of ε

(2) can **be** further written **as,**

$$s(t ; k, \varepsilon) = g\{t - (k-1).T - \varepsilon\}. (\text{Cos}\{\omega_c (t - \varepsilon)\}. \text{Cos}\,\phi_{nk} - \text{Sin}\{\omega_c (t - \varepsilon)\}. \text{Sin}\,\phi_{nk})$$

For a 2-level **DPSK** signal ϕ_{nk} is either 0 or π radians. Hence,

$$s(t ; k, \varepsilon) = g\{t - (k-1).T - \varepsilon\}. (\text{Cos}\{\omega_c (t - \varepsilon)\}). \text{Cos}\,\phi_{nk})$$

Let $a(k) = \cos \phi_{nk}$ (+ 1 for $\phi_{nk} = 0$ and - 1 for $\phi_{nk} = \pi$ radians) and let the modified base-band pulse waveform be defined by:

$$h(t - (k-1).T - \varepsilon) = g\{t - (k-1).T - \varepsilon\}. \cos\{\omega_c (t - \varepsilon)\}$$

Then, $s(t ; k, \varepsilon) = a(k). h(t - (k-1).T - \varepsilon)$ (3)

Using (3) in (1), $v(t) = \left\{ \sum_{k=0}^{N} s(t ; k, \varepsilon) \right\} + z(t)$ (4)

As noted earlier, a MAP estimator chooses ε' in such a manner that the PDF of ε, conditioned on the input signal $v(t)$ ($p(\varepsilon / v(t))$ is maximized. It is shown in [3] that a choice of ε' which maximizes the following function will maximize the conditional PDF $p(\varepsilon / v(t))$.

$$\lambda(v(t), \varepsilon) = \sum_{k=0}^{N} \ln \cosh \left(\frac{1}{} \int_{(k-1)T+\varepsilon}^{kT+\varepsilon} v(t).h(t-(k-1)T-\varepsilon).\, dt \right) \quad (5)$$

This leads to the following algorithm for estimating ε: For different values of ε, compute the quantity given by (5). Select that ε, which gives the highest $\lambda(v(t), \varepsilon)$. An implementation of this algorithm is shown in fig. 4.

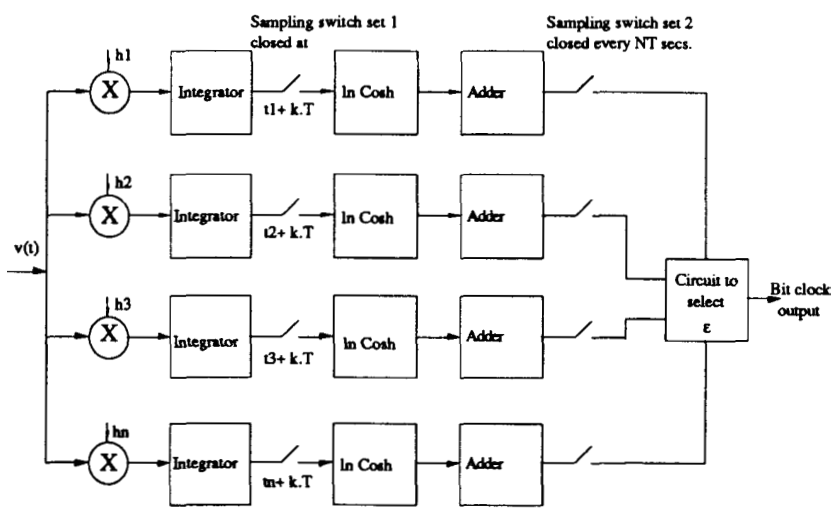

Fig. 4: Ideal *MAP* synchronizer block diagram [3]

In each branch of the above diagram, $\lambda(v(t), \varepsilon)$ is computed for a specific ε. If n branches are used, then ε for each path takes values $0, \pm\frac{T}{2n}, \pm\frac{2T}{2n}$, ...and $\frac{T}{2}$. The circuit to select the appropriate ε compares outputs of all the branches and selects that ε which corresponds to the branch producing a maximum output. The approach used in fig. 4 may be referred to as an "open loop" approach. A closed loop synchronizer with feed back is derived below.

2.1 A closed loop MAP synchronizer:

In a closed loop synchronizer, maximizing $\lambda(v(t), \varepsilon)$ is achieved by forcing $\frac{\partial(\lambda(v(t),\varepsilon))}{\partial\varepsilon}$ to zero and ensuring $\frac{\partial^2(\lambda(v(t),\varepsilon))}{\partial^2\varepsilon}$ to be negative. This leads to the following condition to be satisfied for maximizing the conditional PDF $p(\varepsilon/ v(t))$: (from the general results in [3] as applied to the case of DPSK in [8])

$$\sum_{k=0}^{N} \left\{ \frac{1}{\sigma_z^2} \int_{(k-1)T+\varepsilon}^{kT+\varepsilon} v(t).\frac{\partial h(t-(k-1)T-\varepsilon)}{\partial t}.\, dt. \right\} . \left\{ \tanh\left(\frac{1}{\sigma_z^2} \int_{(k-1)T+\varepsilon}^{kT+\varepsilon} v(t).h(t-(k-1)T-\varepsilon).\, dt \right) \right\} = 0 \quad (6)$$

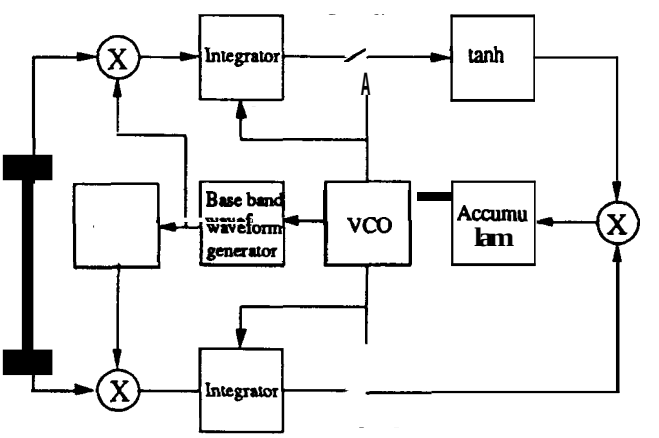

Fig. 5: A closed loop MAP synchronizer [3]

A realization of (6) is shown in fig. 5. Here, the receiver bit clock is derived from a voltage controlled oscillator (VCO) whose phase is varied by evaluating and using a quantity represented by the left hand side of (6) as the feedback signal. The VCO adjusts ε progressively in such a manner that $\frac{\partial(\lambda(v(t),\varepsilon))}{\partial\varepsilon}$ goes to zero. Also, it is important to ensure

that $\frac{\partial^2(\lambda(v(t),\varepsilon))}{\partial^2\varepsilon}$ is negative (< 0) when the above condition is reached. This is done as follows: For any estimate of ε other than its optimal value ε', $\frac{\partial(\lambda(v(t),\varepsilon))}{\partial\varepsilon}$ will be either positive or negative depending upon $\varepsilon < \varepsilon'$ or $\varepsilon > \varepsilon'$, respectively. A correction of VCO in the proper direction is forced by making the sign of the feedback signal depend on the sign of $\frac{\partial(\lambda(v(t),\varepsilon))}{\partial\varepsilon}$

A scheme similar to fig. 5 has been implemented directly for the case of PCM signal [5]. Such implementations show that a considerable hardware is required for realization of the ideal MAP scheme and that all-digital realizations are generally difficult. In the next section modifications are introduced to the ideal scheme to realize a simplified MAP synchronizer.

3: Simplified MAP synchronizer for the DPSK scheme:

A simplified MAP synchronizer is shown in fig. 6; here the following simplifications have been introduced with respect to fig. 5.

a) the input signal is digitized and only its polarity is considered for further processing,

b) the base-band waveform generator is replaced by a polarity-coincidence DPSK demodulator, consisting of a shift register delay line, an EXOR gate and a "continuous integrator" [6], (As shown in Appendix, this constitutes an equivalent replacement than a simplification.)

c) the differentiator is replaced by a subtractor and

d) the tanh function is replaced by its sign.

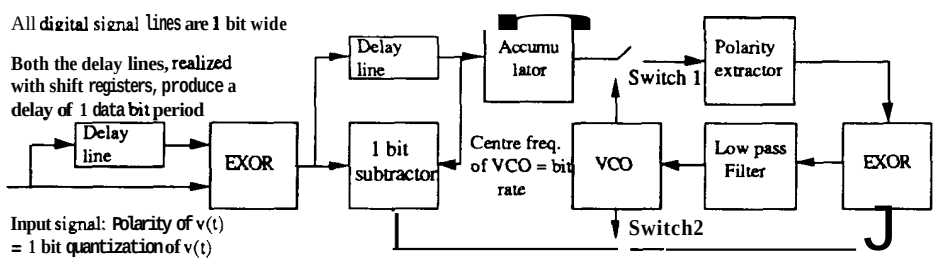

Fig. 6: Simplified MAP synchronizer for the DPSK scheme

Section 4 gives simulation results showing that the BER performance degradation of the DPSK demodulator, due to the simplifications (a) - (d) is negligible.

3.1: The Data Transition Tracking Loop (DTTL):

The DTTL, which is another form of the MAP synchronizer, is described in [7]. In this scheme, two timing generators are used to integrate the input signal "along" the data and "across" the data transitions. The outputs of these integrators are then used to drive a VCO to achieve the required synchronization. In the original form the DTTL also requires substantial hardware for its realization. Simplifications similar to the ones given above lead to a reasonably simple all-digital synchronizer for the DPSK scheme. This simplified scheme is shown in fig. 7.

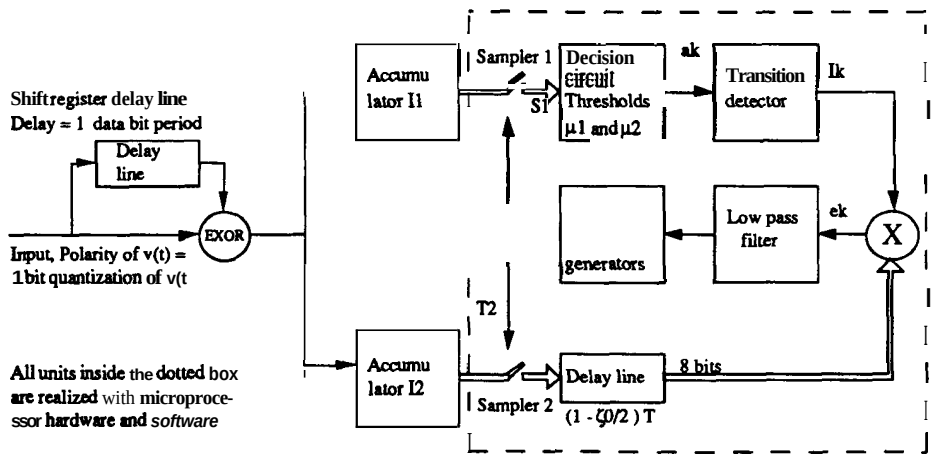

Fig. 7: Simplified DTTL synchronizer

In the scheme shown in fig. 7, output of the polarity coincidence DPSK demodulator is fed to two accumulators (integrators) which integrate "along" the data and "across" the data transitions respectively. ζ_0 is a parameter defining the period over which the "across-the-transition" integrator I_2 integrates. These integrators are reset at the appropriate instants by the timing generators. The sampled outputs of these integrators. after suitable processing as shown in fig. 7, are multiplied. The multiplied output is filtered and used to drive the VCO, the output of which generates the required timing waveforms to operate the sampling switches as well as the integrators. The waveforms associated with this circuit are shown in fig. 8.

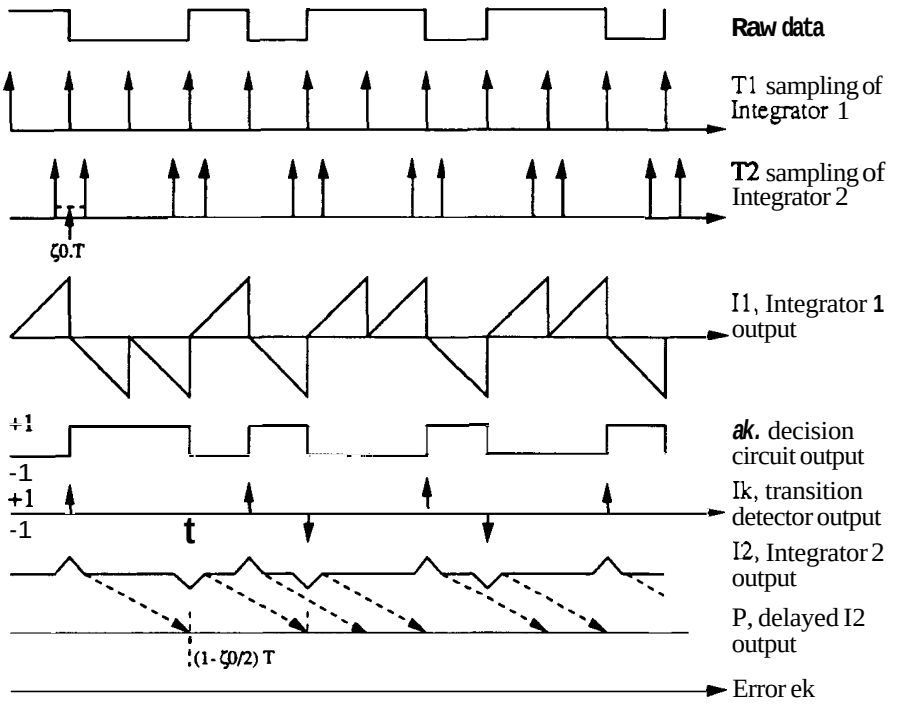

Fig. 8: DTTL synchronizer waveforms under perfect synchronization

4. Simulation of bit synchronizers for the DPSK scheme:

An exhaustive computer simulation of the all-digital synchronizers developed above (figs. 6 and 7) was carried out in order to understand and evaluate their performance. The parameters obtained from the simulation program are: (i) degradation of BER performance of a DPSK demodulator when sampled by the synchronizer output and for different signal to noise ratios (SNRs), (ii) jitter produced and its PDF at various SNRs and (iii) acquisition time of the receiver bit clock, at various SNRs. The details of the modular program used are given in [8].

The following conditions were used for the simulation:

Bit rate: 200 bits/sec.
Carrier frequency: 800 Hz., 2 level DPSK modulated with differential phase shifts of 0 and π radians for data 0 and 1, respectively.
Clock used for sampling the polarity signal: 128 X 200 Hz (25, 600 Hz).
Filter for the DPSK receiver: Bandwidth: 200 Hz centred around 800 Hz (ideal band-pass assumed). realized as a 128 tap transversal filter.

Noise source: Gaussian distribution, filtered with the above ideal band pass filter.
Number of bits used for simulation at each SNR: 10, 000

Effect of synchronizerson the BER performance of a DPSK demodulator is shown in fig. 9. The data for the curves in fig. 9 were obtained by running the simulation for SNRs from -4 dB to 8 dB with 2 dB steps and counting the number of bit errors which occured during the run. It can be seen from fig. 9 that the degradation of the demodulator performance due to the simplified MAP as well as to the DTTL synchronizeris negligible. Moreover, simulation with the ideal MAP scheme showed that the BER performance degradation due to the simplified schemes is only about 0.1 to 0.2 dB when compared with the ideal MAP scheme.

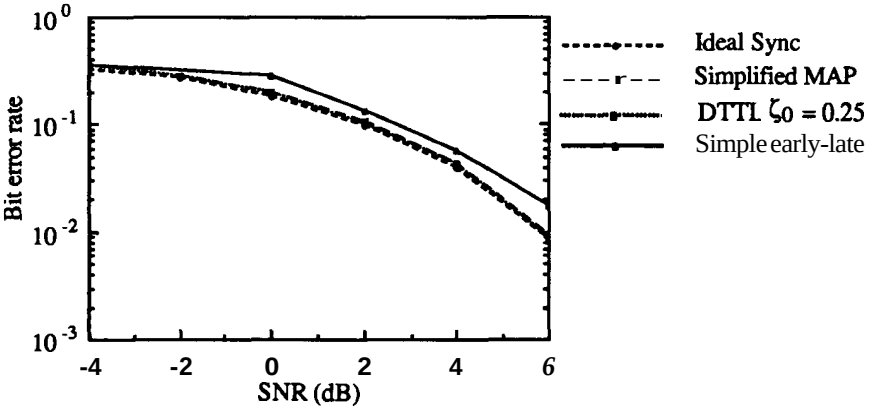

Fig. 9: BER of IAD DPSK demodulator with different synchronizers (simulation results)

The jitter performance (at SNR = 4 dB) of the synchronizers is shown in fig. 10. This was obtained by running the simulation program for SNRs from -4 dB to 12 dB in steps of 4 dB. In every run the jitter at each bit clock edge was noted after an initial synchronization period of 50 bits. After the run, the jitters noted in 10, 000 clock edges were statistically analyzed to obtain data for fig. 10. It is to be noted in fig. 10 that the simplified MAP and DTTL schemes have much shorter tails in their jitter distribution functions than the simple early-late scheme. This indicates that their higher order moments are lower than those of the simple early-late scheme. Moreover, these schemes have a mean jitter close to zero. Hence, the degradation of BER performance due to these schemes are less than that due to the simple early-late scheme.

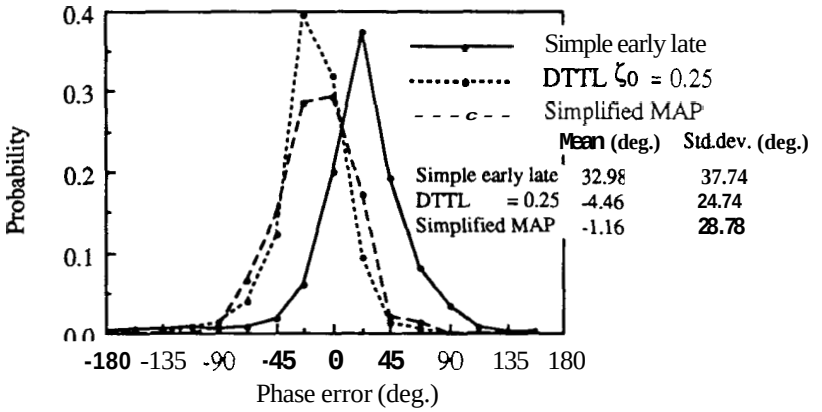

Fig. 1 0 Jitter distribution of different synchronizers (Simulated at SNR = 4 dB)

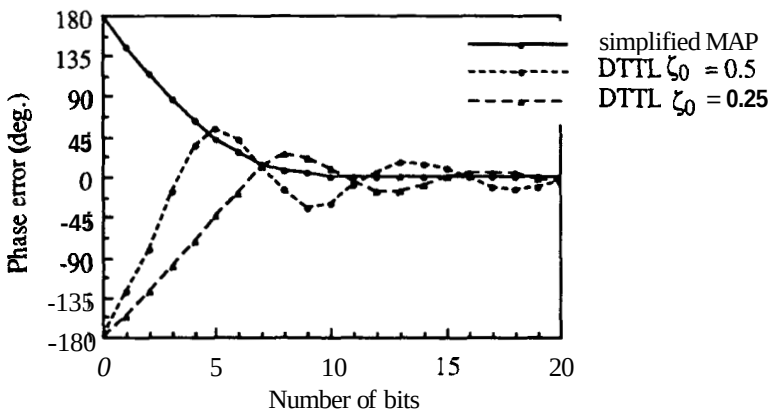

Fig. 11: Sync. acquisition of synchronizers (simulation results)

The time taken for achieving synchronization is shown in fig. 11. Data for this figure was obtained by running the simulation program with different initial phases and noting the phase error at the end of each data transition. When the phase error was lower than 5 deg. and was stable for at least 10 more bit transitions, synchronization was assumed to have been achieved. The simulation was carried out for SNRs from 0 dB to 16 dB in steps of 4 dB. Results are given for $SNR = 16$ dB in Fig. 11. While the simplified MAP synchronizer has the best acquisition time and a smooth sync. acquisition, the DTTL has a decaying oscillatory tendency during sync. acquisition. The nature of this oscillation is a function of the parameter ζ_0.

However, the acquisition time is nearly the same for different ζ_0 s. ζ_0 = 0.1 to 0.3 may be useful in the practical designs.

5. Hardware realization of MAP and DTTL synchronizers:

Simplified MAP and DTTL synchronizers with the following specifications were built with circuits based on ICs and a microprocessor:

Bit rate: 300 bits per second (BPS)
Carrier frequency : 300, 600, 1200, 1800, 2400 Hz, switch selectable
Receive signal: -45 to -6 dBm across 600 ohms
Transmit and Receive filters: 3 dB bandwidth of 300 Hz, centred around the carrier, pass band ripple less than 0.5 dB. Carrier rejection at +/- 450 Hz around the carrier, greater than 35 dB. Filters are realized as 32 bit transversal filters. followed by an active low pass filter to cut off harmonics of the sampling frequency used in the transversal filter.

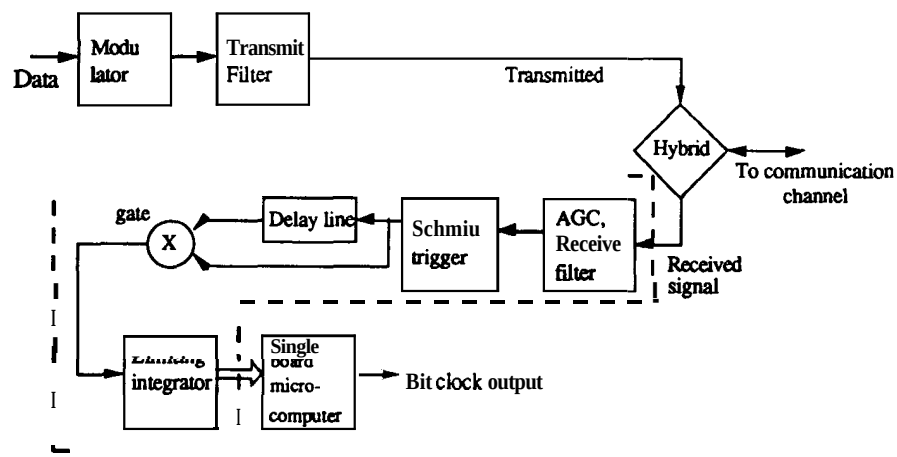

Fig. 1 2 Block schematic of the DPSK demodulator and synchronizer

The DPSK transmitter and filter with adjustable gain are built with digital ICs like flip-flops, shift registers, gates as well as with OPAMPs. The received signal is passed through a receive filter, automatic gain controlled amplifier (AGC) and a Schmitt trigger to obtain the polarity of the received signal. This polarity signal is then delayed by T, the bit time, using a shift register. The delayed output is combined with the undelayed polarity signal in an EXOR gate. The output of the EXOR gate is passed through a continuous integrator to obtain the raw data

output [9]. The receiver bit clock is generated by a microprocessor controlled timer. Every positive transition of the timer output interrupts the processor. The interrupt routine of the microprocessor then reads the limiting integrator value and determines the correction to be applied to the timer, based on the MAP or DTTL algorithms. The microprocessor card used for the synchronizer is a 8085 based single board-microcomputer.

The demodulator with the synchronizer is then tested for the BER, jitter and acquisition performances. The BER performance is tested using the HP 1645S data error analyzer of M/S Hewlett Packard. This instrument generates pseudo-random data sequences of different lengths for testing the data communication system, performs a bit-by-bit comparison between the data generated and the data fed back to the instrument through the data communication system to compute the BER and it also measures the percentage jitter in the receiver bit clock.

Fig. 13 gives the results of BER tests on the demodulator with different synchronizers. The test was conducted for SNRs from 0 to 16 dB in 2 dB steps up to 8 dB, and in 4 dB steps from there onwards. The noise generator used was based on the random noise produced by a Zener diode. This was filtered by an eighth order BPF to limit the noise bandwidth to +/- 150 Hz, centred around the carrier.

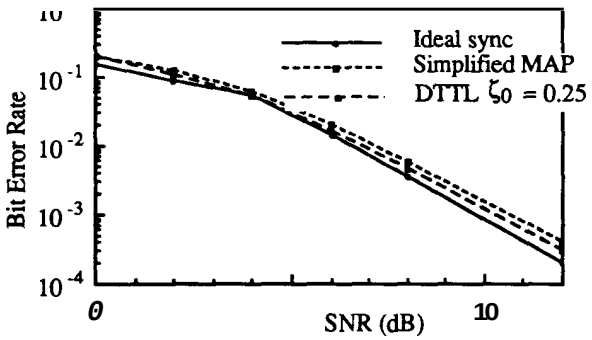

Fig. 13: BER vs SNR of DPSK demodulator with synchronizers (Hardware)

During the BER test, the percentage jitter was also measured by triggering the data error analyzer with the bit clock produced by the synchronizer. Results of this are shown in Fig. 14.

Acquisition time measurement were carried out here with noise removed. For measuring the acquisition time, the initial phase of the bit clock is set to any desired value and the program for synchronization is started. The phase error is given to one channel and the bit clock to another channel of a storage oscilloscope. Number of bit periods required for synchronization

to be achieved is then noted. It was found that the acquisition time as well as the phase error variation during synchronization agreed closely with the simulation results.

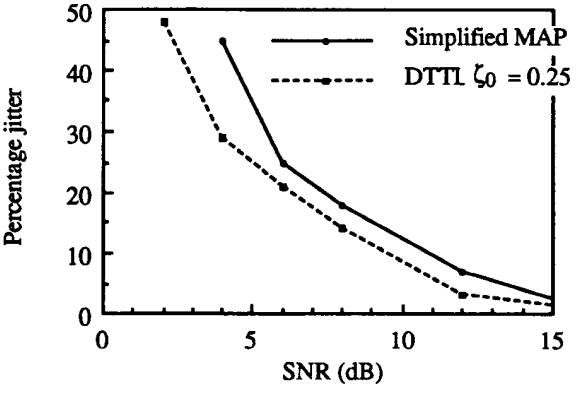

Fig. 14 : Percentage jitter vs SNR of synchronizers (Hardware test results)

6. Conclusions:

Analysis, computer simulation and hardware of simplified MAP and DTTL synchronizers for the 2 level DPSK scheme are presented in this paper, leading to the following results:

a) The optimal synchronizers can be transformed, with some modifications, into simpler schemes. The BER degradation introduced by these simplified schemes is nearly the same as that of the optimal synchronizer.

b) The simplified synchronizers perform substantially better than "ad-hoc" synchronizers, such as early-late synchronizers, without requiring excessive additional circuitry. One may note here that the simplified MAP scheme requires less hardware than the DTTL scheme.

c) These simpler schemes are realizable by digital ICs and a microprocessor. Therefore. it is possible to design a single chip IC consisting of a DPSK modulator, a demodulator and a synchronizer with the help of standard modules available from VLSI design libraries.

7. Appendix: Replacement of base-band generators by the polarity coincidence DPSK demodulator in the MAP synchronizer.

Proof that polarity coincidence DPSK demodulator can replace the base-band generators in the open loop MAP synchronizer is given below. The proof for the closed loop synchronizer proceeds along similar lines and is not given.

Consider the integral $\int_{(k-1)T+\varepsilon}^{kT+\varepsilon} v(t).h(t-(k-1)T-\varepsilon).\,dt$ in ***(5)***. Substituting the expression for v(t) in this expression and considering the noiseless case, we get:

$$\int_{(k-1)T+\varepsilon}^{kT+\varepsilon} v(t).h(t-(k-1)T-\varepsilon).\,dt) = \int_{(k-1)T+\varepsilon}^{kT+\varepsilon} a(k).\,h(t-(k-1).T-\varepsilon).\,h(t-(k-1)T-\varepsilon).\,dt$$

$$= a(k)\,.\,W_k, \text{ where } W_k = \int_{(k-1)T+\varepsilon}^{kT+\varepsilon} h(t-(k-1).T-\varepsilon).h(t-(k-1)T-\varepsilon).\,dt$$

Hence ***(5)*** can be rewritten as: $\lambda\,(v(t), \varepsilon) = \sum_{k=0}^{N} \ln \cosh\,(\frac{1}{\sigma_z^2} a(k)\,.\,W_k)$ but as $a(k) = \pm 1$ and Cosh is an even function of its argument, we get:

$$\lambda\,(v(t), \varepsilon) = \sum_{k=0}^{N} \ln \cosh\,(\frac{1}{\sigma_z^2} W_k) \qquad \text{(A1)}$$

Consider now the polarity coincidence **DPSK** demodulator output, shown in fig. 6. The output of this circuit is integral of the product of v(t) and its delayed version. Hence, its output is given by the integral $\int_{t}^{t+N.T} v(t)\,.v(t-T)\,dt$. Consider this integral during the k th instant in the noiseless case. It is given by:

$$I_{dpsk} = \int_{(k-1).T+\varepsilon}^{kT+\varepsilon} a(k).\,h(t-(k-1).T-\varepsilon).a(k-1).\,h(t-(k-2)T-\varepsilon)\,dt$$

$$= a(k).\,a(k-1) \int_{(k-1).T+\varepsilon}^{kT+\varepsilon} h(t-(k-1).T-\varepsilon).\,h(t-(k-2)T-\varepsilon)\,dt = a(k).\,a(k-1)\,W_k$$ because, as noted earlier h is a function independent of k. Consider the following function B(v(t), ε):

$$B(\,v(t), \varepsilon) = \sum_{k=0}^{N} \ln \cosh\,(\frac{1}{\sigma_z^2}\, I_{dpsk}) = \sum_{k=0}^{N} \ln \cosh\,(\frac{1}{\sigma_z^2}\,.\,a(k).\,a(k-1).\,W_k)$$

$$= \sum_{k=0}^{N} \ln \text{ Cosh } \left(\frac{1}{\sigma_z^2} \cdot W_k\right), \text{ as Cosh is an even function of its argument.}$$

This expression is the same as (A1). Hence, the base-band waveform generators required in the MAP synchronizer may be replaced by a polarity coincidence demodulator.

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