# Reduction of Tab-to-Chassis Capacitance of a Power MOSFET and Conducted Emission through Proper Mounting Arrangement

P. Sidharthan
Microwave Tube Research & Development Centre
Bangalore-560013, INDIA
sidharthan@mtrdc.drdo.in

G. Narayanan
Dept. of Electrical Engineering
Indian Institute of Science
Bangalore-560012, INDIA
gnar@iisc.ernet.in

***Abstract*— Tab-to-chassis capacitance of a power MOSFET and associated conducted emission is a matter of growing concern for switched-mode power converters as one prefers higher switching frequency to shrink the size and tries to limit the common-mode noise as mandated by contemporary electromagnetic emission norms. This paper explores a few techniques of mounting a MOSFET to the chassis to reduce conducted common-mode emission through proper dielectric isolation and shielding mechanism without compromising the thermal management. The effects are studied using analytical approach as well as through experiments. It is found that the connection of the device lead to a copper shield sandwiched between two dielectric sheets reduces the common-mode current by as much as 20 dB.**

***Index Terms*— Common-mode interference, Electromagnetic interference, Electromagnetic compatibility, power MOSFET, switch mode power supply**

## I. Introduction

Power supply designers face the challenge of delivering more power at higher efficiency, occupying smaller volumes for smarter applications, complying with newer and tougher electromagnetic compatibility (EMC) and emission standards [1]-[7]. The switching transitions in sub-micro seconds duration are rich in harmonic content, which could potentially interfere with internal and external electronic equipments through conducted and radiated emissions [8]. Such interferences need to be handled through appropriate measures including device mounting, PCB layout design, power converter packaging and EMI filter design [1], [2], [4].

The parasitic coupling between the switching nodes in the circuit and the chassis is the major source of common-mode conducted emission. Since power switching MOSFET is a significant contributor to the conducted EMI, this paper addresses a few techniques of mounting a MOSFET to the chassis through proper dielectric isolation and shielding mechanism. Care has been taken to ensure that the aspect of thermal management is not compromised while optimizing the mounting mechanism and the choice of dielectric material. It would be interesting to see as to how appropriate methods of isolation and shielding influence the common-mode current.

The paper is organized in seven sections. Section II briefly reviews the emission standards [5], [6]. Different arrangements for mounting a power MOSFET in an SMPC are described in section III. The coupling capacitance between the power MOSFET and the chassis is studied analytically and experimentally in section IV, section V deals with theoretical calculations of thermal resistances pertaining to different mounting arrangements. The conducted emission is studied experimentally in section VI. Section VII is devoted to conclude the study.

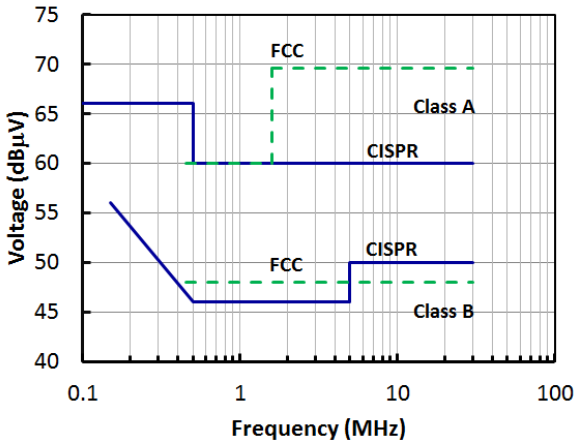


Fig.1 Comparison of conducted emission limits for FCC [5] and CISPR [6]

## II. Review of Conducted Emission Standards

The electromagnetic spectrum is shared by various agencies for intentional civil and military applications. In order to achieve uninterrupted functioning of co-located electronic and electrical instruments, certain regulations are laid down by various regulatory authorities[5]-[7]. The equipments are classified into class A and class B depending on their deployment [5], [6]. The conducted emission limit lines by FCC and CISPR agencies are given in Fig.1. In India, the radiated and conducted emission limits are defined by Bureau of Indian Standards (BIS) [7]. Quite often, CISPR and FCC standards are also followed in India with certain modifications. Most of the Military Standards related to EMI/EMC are tougher than that for commercial electronic equipments. Usually, the military equipments follow the EMI/EMC specifications laid down as per MIL-STD-461F, [9].

## III. Electrical considerations for mounting and choice of dielectrics

Considerable amount of parasitic capacitance exists between the tab of a power MOSFET and the heatsink, meant for power dissipation.With an intention to reduce switching loss, generally the designer drives the gate as fast as possible with the selected gate driver. The switching drain terminal (usually the tab of device) draws sharp transition currents through the parasitic capacitance from the chassis / heatsink constituting common-mode interference [10], [11].

The conventional method of mounting a power MOSFET available in a TO-220 packageis illustrated in Fig. 2(a). A thin dielectric sheet such as Sil-Pad® is used between the tab and heatsink [12]. Various methods of mounting the power MOSFETs in order to curtail the conducted emission within limits are studied here.

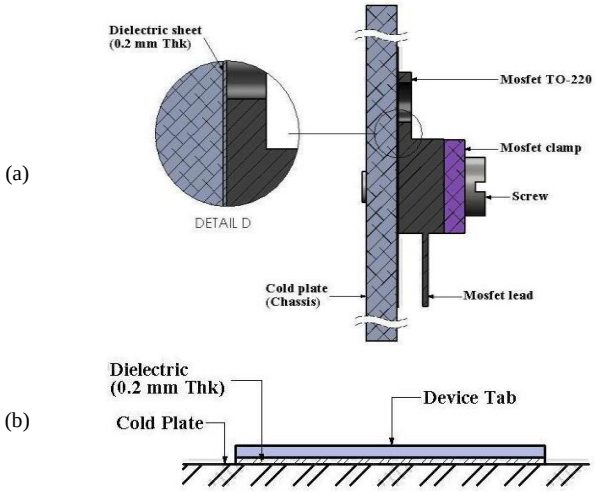


Fig. 2. Mounting arrangement-1 for the MOSFET (a) Cross sectional view and (b) Tab-to-chassis capacitance

Clearly the above arrangement in Fig. 2(a) results in a parasitic capacitance between the tab and the heatsink. In order to reduce this capacitance, the gap between the tab and the heatsink / chassis can be increased with a thermally conductive and electrically insulating material as shown in Fig. 3(a).

The mounting arrangement-2 (Fig. 3(a)) uses a wafer of aluminum nitride having a thermal conductivity of 175W/mK and dielectric breakdown strength of 20kV/mm. The thickness of wafer can be decided based on the thermal and electrical considerations. The thickness is chosen to be 2mm here. In addition to providing the electrical isolation, the aluminum nitride substrate helps appreciably in thermal management of the device (thermal conductivity ~ 10 times that of $Al_2O_3$).

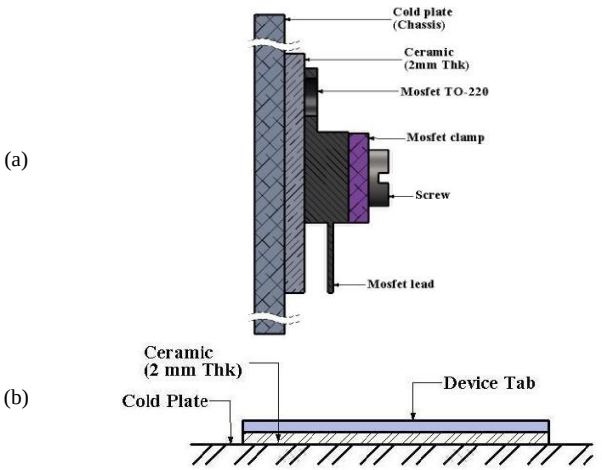


Fig. 3. Mounting arrangement-2 (a) Cross sectional view (b) Tab-chassis capacitance

The parasitic coupling can be reduced further by employing a copper foil as shown in Fig. 4(a). The shield prevents the switching tab from direct exposure to chassis, reducing the charging or discharging currents through the parasitic capacitance during switching transitions.

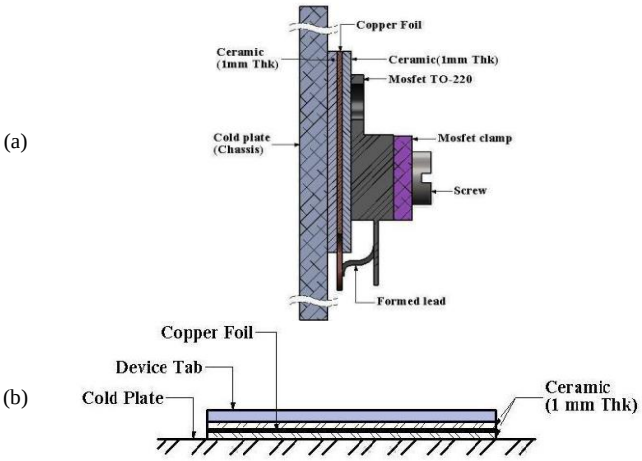


Fig.4. Mounting arrangement-3 (a) Cross sectional view (b) Tab-chassis capacitance

If the source lead of the MOSFET is connected to the negative DC rail (as in the present case, Fig. 5(a)), the source pin is directly soldered on to the copper shield as shown in Fig. 4(a) to reduce the parasitic inductance. If the drain of the MOSFET is connected to the positive DC rail, then the drain pin is soldered on to the copper shield.

The efficacy of the mounting arrangements-2 and 3 (Fig. 3 and Fig. 4) in reducing the parasitic capacitance between tab and chassis, compared to the conventional arrangement (Fig. 2), is studied theoretically and experimentally in the following section.

## IV. Study of Coupling Capacitance

The overlapping area between the device tab and the chassis in the various mounting arrangements along with the dielectric in between can be considered to constitute a parallel plate capacitance C, given by

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d} \quad (1)$$

where $\varepsilon_0$ is the permittivity of free space, $\varepsilon_r$is the relative permittivity of the dielectric material, A is the overlapping area (150mm$^2$) and d, the separation between the surfaces.The relative permittivities ( $\varepsilon_r$) of the dielectrics are indicated in Table.1. The theoretical values of the coupling capacitance of the three mounting arrangements are calculated using equation (1) for two types of dielectric materials namely aluminum nitride and Sil-Pad®. The parasitic capacitances for the different mounting arrangements are also measured using an LCR meter. Both the theoretical and measured values of the tab-chassis capacitance are tabulated in Table.1.

Table.1

| Mounting arrangement | Dielectric constant ($\varepsilon_r$) | Device Tab-Chassis Capacitance (pF) | |
|---|---|---|---|
| | | *Theory* | *Measurement* |
| Arrangement-1 with 0.2mm thick dielectric sheet (Sil-Pad®) | 5.5 | 36.5 | 36 |
| Arrangement-2 with 2mm thick ceramic (AlN) | 9 | 12 | 14 |
| Arrangement-3 with 1mm ceramic + copper foil + 1mm ceramic | 9 | 11 | 10 |

As seen from Table.1, appropriate selection of the dielectric and separation between the tab and chassis bring down the parasitic capacitance by a factor of three between arrangements-1 and 3.This should imply significant reduction in the common-mode current as will be ascertained in section VI.

## V. Calculation of Thermal Resistance

The conventional mounting discussed in arrangement-1 with Sil-Pad material SPK-10 yields a thermal resistance of the order of 2°C/W for TO-220 package. The mounting arrangement-2 with 2mm aluminum nitride introduces only 0.076°C/W owing to the high thermal conductivity. The mounting arrangement-3 discussed introduces two additional junctions in the path of heat flow from the device tab to the heat sink. These additional interfaces can be reasonably approximated by introducing an empirical reduction factor in effective area of cross section of the device tab involved in the heat transfer. In the present case, considering reduction factor of 0.8, we can calculate the effective thermal resistance of the mounting arrangement-3 as 0.095°C/W. The copper foil of 0.2mm thickness introduces negligible thermal resistance of 0.0033°C/W in the path of heat transfer. The calculation presented shows that the mounting arrangement-3 does not compromise on heat conduction from the device tab to the heatsink.

## VI. Experimental Study of Common-Mode Conducted Emission

This section describes the experimental set-up (Fig.5) and the procedure for measuring the common-mode current and its spectra, pertaining to mounting arrangements 1 and 3.

### *A. Experimental set-up*

A photograph of the experimental set-up is shown in Fig. 6. A 270V DC isolated sourceis used to feed a load resistance of 330Ω in series with a 600V, 20Apower MOSFET SPP20N60S5 [13], through a line impedance stabilization network (LISN). The MOSFET is driven by the lower MOSFET driver of IR2113 [14] through a 33Ω gate resistor ($R_2$). The gate drive circuit is powered by an isolated 15V power supply following star grounding near the source terminal of the MOSFET as shown in the schematic (Fig.5). This connection helps to segregate the various current paths and minimizes interferences from modifying the common-mode current being measured. The gate drive signal is issued from a function generatorwith a switching frequency of 100kHz and a duty cycle of 0.1.

The MOSFET and load are placed as close as possible to one another. Further a parallel combination of low ESR capacitors – low-ESR electrolytic capacitor (C1) and a polypropylene capacitor (C2) is placed in close proximity to the MOSFET and load. These decoupling capacitors serve to reduce the effect of the inductance of the lead wires, which are twisted ones, from the LISN.

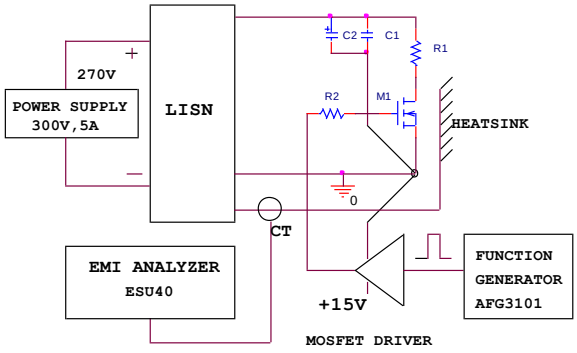


Fig.5.The schematic of experimental set up

The heatsink is connected to the LISN through a high bandwidth current transformer for measuring the common-mode current. The output from the current transformer is fed to an oscilloscope for current measurement.

Since the power dissipated in the load resistor is significant, a separate heatsink is used for cooling the same. The resistor's heatsink is isolated from the MOSFET heatsink with Teflon pillarsof length 10mm. This eliminates possible common-mode current injection from the load resistor to the MOSFET heatsink.

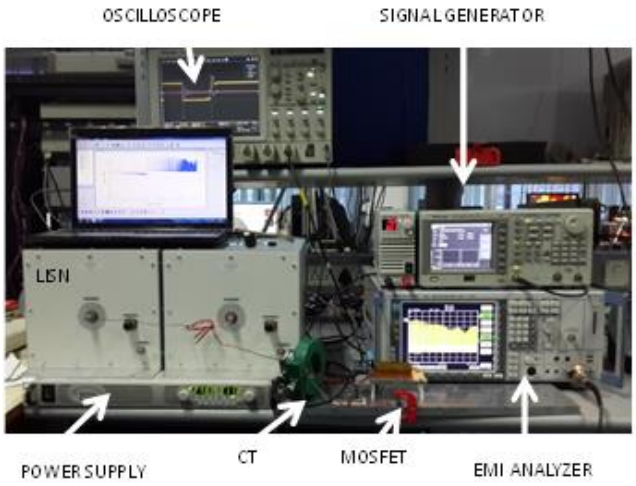


Fig.6. Photograph of the experimental set-up

*B. Measured Common-mode current*

As seen from Fig. 7(a) and Fig. 7(b), the device tab draws considerable current through the chassis during the transitions. The oscilloscope screen shot in Fig. 7(a) shows a peak common-mode current of amplitude close to 220mA with the conventional mounting arrangement-1. This current is reduced to a much lower value of 20 mA with mounting arrangement-3 as shown by Fig. 7(b).

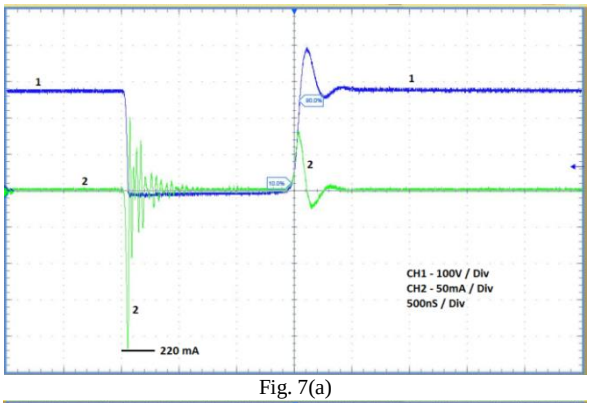


Fig. 7(a)

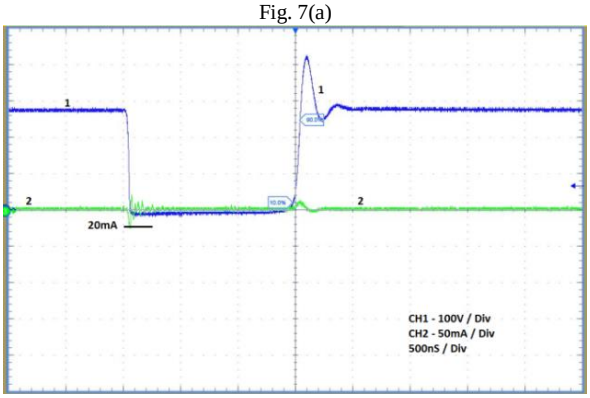


Fig. 7(b).

Drain voltage transition and common-mode current for MOSFET

Fig. 7(a) Mounting arrangement-1, $R_2$ =33Ω

Fig. 7(b) Mounting arrangement-3, $R_2$ =33Ω

Fig. 8(a) and Fig. 8(b) show a similar reduction in the common mode current with the mounting arrangement-3 for a different gate resistance of 10Ω. Once again, the peak common-mode current is found to reduce significantly from 285mA to 40mA. Thus the arrangement-3 is effective in reducing the common-mode current over a range of gate drive resistor values.

In all the oscillograms presented, channel-1 is set to 100 V/division for device voltage measurement; channel-2 is set to 50 mA/division for measuring common-mode current; the horizontal scale is 500ns / division.

*C. Measured Common-mode current spectra*

An EMI analyzer (ESU40 with EMC32 software) is used to examine the harmonic spectra of the measured common-mode currents. A high bandwidth current transformer is used as shown in Fig. 5 with a 20dB attenuator to protect the front end of the analyzer. It may therefore be noted that the spectra presented are not absolute - the discussion is only about the relative reduction among the different arrangements of mounting of power MOSFET.

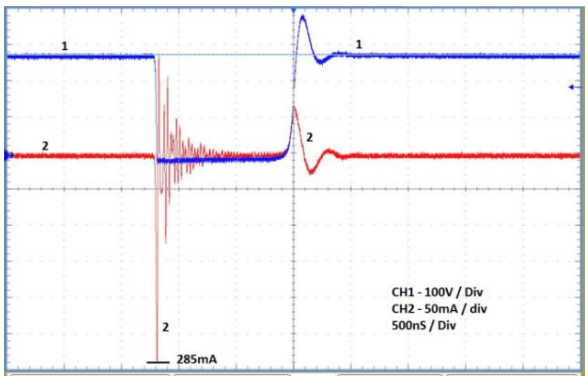


Fig. 8(a).

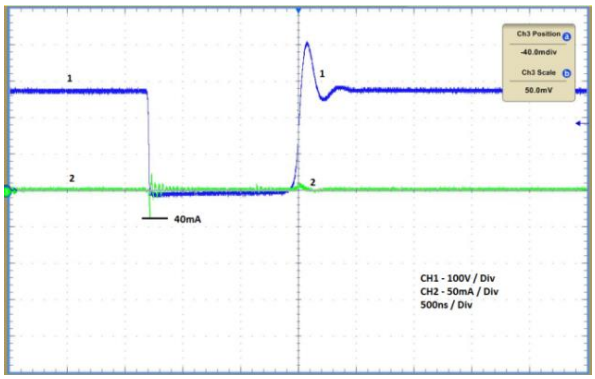


Fig. 8(b).

Drain voltage transition and common-mode current for MOSFET

Fig. 8(a).Mounting arrangement-1, $R_2$ =10Ω

Fig. 8(b).Mounting arrangement-3, $R_2$ =10Ω

The measured spectra corresponding to the common-mode currents in Fig. 7(a) and Fig. 7(b) are presented in Fig. 9(a) and Fig. 9(b), respectively. Similarly, the spectra corresponding to Fig. 8(a) and Fig. 8(b) are shown in Fig. 10(a) and Fig. 10(b) respectively. Compared to the conventional arrangement-1, a significant improvement in the harmonic spectrum can be seen with the mounting

arrangement-3 on account of the shielding provided by the copper foil in addition to the reduced parasitic capacitance between the device tab and heat sink.

For a gate resistance of 33 ohms, the amplitude in the common mode-current spectra can be seen to reduce from 45 dBμV to 25 dBμV in the low frequency range and from 40 dBμV to 23 dBμV in the high frequency range as shown by Fig.9. Similar observations can also be made regarding the spectra with 10-ohm gate resistance as shown by Fig.10.

It can be observed from Fig. 9(a) and Fig. 10(a) that faster turn on with reduced gate resistance pushes up the emission levels at the higher end of the spectrum. This has the potential to increase the radiated emission, apart from contributing to the conducted emission. The mounting arrangement-3 reduces the common-mode current harmonics and makes the conducted emission less sensitive to the gate resistance as evident from Fig. 9(b) and Fig. 10(b).

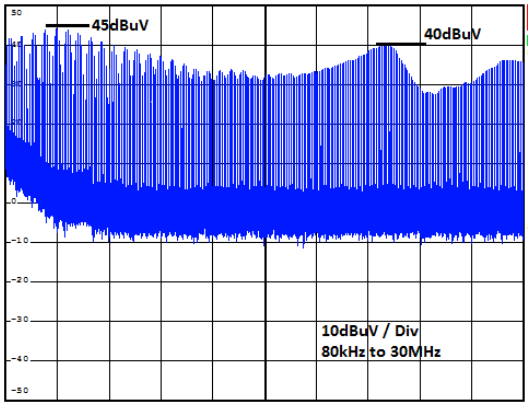


Fig. 9(a).

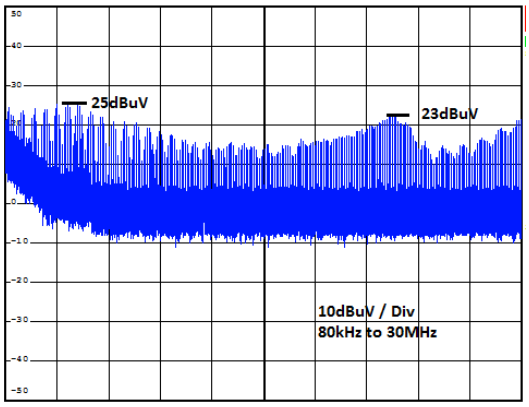


Fig. 9(b).
Common-mode current spectrum
Fig.9(a) Mounting arrangement-1, $R_2 = 33\Omega$
Fig.9(b) Mounting arrangement-3, $R_2 = 33\Omega$

## VII. Conclusion

The impact of MOSFET mounting on the parasitic capacitance between the device tab and chassis / heatsink is studied for a single MOSFET driving a resistive load. A comparative study was performed for three different types of mounting arrangements. It is verified that by suitable mounting, shielding and appropriate selection of the isolating dielectric, the common-mode conducted emission could be brought down by as much as 20 dB. The common-mode current waveforms and their harmonic spectra corroborate the theoretical expectations on reduction of the common-mode current by appropriate mounting arrangements. It is also shown that the mounting arrangement can be made without compromising the efficacy of heat transfer from the device tab to the heatsink.

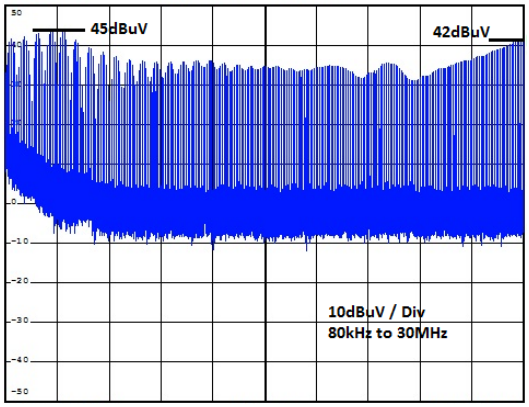


Fig. 10(a).

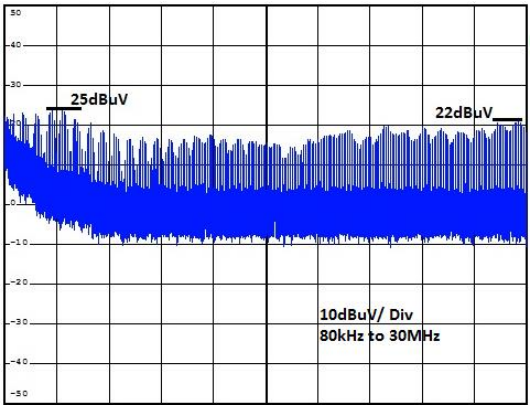


Fig. 10(b).
Common-mode current spectrum
Fig.10(a) Mounting arrangement-1, $R_2 = 10\Omega$
Fig.10(b) Mounting arrangement-3, $R_2 = 10\Omega$

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