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Performance tunability of field-effect transistors using $MoS_{2(1-x)}Se_{2x}$ alloys

Sooraj Sanjay[1,4], Kolla Lakshmi Ganapathi[2,4], Eswaraiah Varrla[3] and Navakanta Bhat[1,*]

[1] Centre for Nano Science and Engineering, Indian Institute of Science, Bengaluru - 560012, India
[2] Department of Physics, 2D Materials Research and Innovation-group, Quantum Centers in Diamond and Emergent Materials (QuCenDiEM)-group, Indian Institute of Technology Madras, Chennai - 600036, India
[3] Laboratory of Nanosheets and Nanocomposites, Department of Physics and Nanotechnology, SRM Institute of Science and Technology, Kattankulathur, Chengalpattu, Tamil Nadu - 603202, India

E-mail: navakant@iisc.ac.in

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Abstract

Ultra-thin channel materials with excellent tunability of their electronic properties are necessary for the scaling of electronic devices. Two-dimensional materials such as transition metal dichalcogenides (TMDs) are ideal candidates for this due to their layered nature and great electrostatic control. Ternary alloys of these TMDs show composition-dependent electronic structure, promising excellent tunability of their properties. Here, we systematically compare molybdenum sulphoselenide ($MoS_{2(1-x)}Se_{2x}$) alloys, MoS_1Se_1 and $MoS_{0.4}Se_{1.6}$. We observe variations in strain and carrier concentration with their composition. Using them, we demonstrate n-channel field-effect transistors (FETs) with SiO_2 and high-k HfO_2 as gate dielectrics, and show tunability in threshold voltage, subthreshold slope (SS), drain current, and mobility. MoS_1Se_1 shows better promise for low-power FETs with a minimum SS of 70 mV dec^{-1}, whereas $MoS_{0.4}Se_{1.6}$, with its higher mobility, is suitable for faster operations. Using HfO_2 as gate dielectric, there is an order of magnitude reduction in interface traps and 2× improvement in mobility and drain current, compared to SiO_2. In contrast to MoS_2, the FETs on HfO_2 also display enhancement-mode operation, making them better suited for CMOS applications.

Keywords: 2D alloys, FETs, tunability, HfO_2, interfaces, $MoS_{2(1-x)}Se_{2x}$

(Some figures may appear in colour only in the online journal)

1. Introduction

Two-dimensional layered materials attract great interest in next-generation electron devices due to their excellent electrostatics and atomically thin nature [1]. They are well suited for extremely scaled devices, which are vital for Moore's law scaling [2]. Of the large variety of these materials, transition metal dichalcogenides (TMDs) possess a non-zero bandgap, making them attractive candidates for field-effect transistors (FETs). Different members of the TMD family show a wide variety in properties like bandgap and electronic structure, which also varies with the number of layers [3]. For example, Molybdenum disulfide [4–6] (MoS_2) shows bandgap of 1.23 eV (indirect) in bulk form which increases to 1.89 eV (direct) in monolayer; molybdenum diselenide [4, 7] ($MoSe_2$) has bandgap from 1.09 eV in bulk to 1.5 eV in monolayer. Ternary alloys of these materials can offer additional knobs to tune their characteristics.

Various theoretical and experimental studies were conducted on the properties of ternary alloys of 2-D TMDs such as $MoS_{2(1-x)}Se_{2x}$ and $Mo_{1-x}W_xS_2$ [8–18]. Much like the III–V materials, these studies have shown that alloying in TMDs can systematically vary their characteristic properties. Variations in electronic structure and bandgaps have been observed with the incorporation of Se in MoS_2 or W in MoS_2 [9, 15, 18, 19]. The option to tune these characteristics could prove beneficial for device applications such as diodes [20],

[4] These authors contributed equally to this work.
[*] Author to whom any correspondence should be addressed.

photodetectors [21], and transistors. Early studies on TMD alloys have explored their synthesis and material characteristics. Various methods ranging from chemical vapor transport [12], chemical vapor deposition [15, 18], physical vapor deposition [13] to partial substitution via facile alloying [16] were used for their synthesis, and their material characteristics were extensively studied using spectroscopy. Much of the previous studies on their applications were focused on their catalytic activity and optical properties [12, 14, 17]. Despite the popularity of MoS_2 for FETs, detailed research of FETs of its alloys is limited. Although there are a few studies of FETs on other 2-D alloy systems such as $W_{1-x}Re_xS_2$ [22], $MoSe_{2x}Te_{2(1-x)}$ [23], $WS_{2x}Se_{2(1-x)}$ [24], etc, they are still limited to using SiO_2 as dielectric and do not explore the integration of high-k gate dielectrics for improved performance. In the case of MoS_2, alloying with another chalcogen, such as selenium, provides another knob to control its transistor characteristics. Besides, their integration with high-k dielectrics is also necessary to enable Moore's scaling for these devices.

In this work, we explore the characteristics of transistors using the alloys of MoS_2 and $MoSe_2$, of form $MoS_{2(1-x)}Se_{2x}$. Two different stoichiometries were chosen for this—the selenium-rich $MoS_{0.4}Se_{1.6}$ ($x = 0.8$), and MoS_1Se_1 ($x = 0.5$) with equal S:Se ratio. A brief material study into the nature of strain in these and their carrier concentrations is provided. To compare and contrast their utility as transistors, we fabricate FETs using SiO_2 as the dielectric. We also demonstrate the use of high-k dielectrics (hafnium oxide) to improve their performance even further. A detailed comparison of performance metrics and interface quality with these two dielectrics is also conducted. Our studies reveal tunability in parameters such as carrier concentrations and threshold voltage, along with variations in mobility, drain currents, and contact resistance with alloying. Among the composition studied in this work, MoS_1Se_1 shows better promise in lower power, while $MoS_{0.4}Se_{1.6}$ is more suited towards higher speed switching operations. The comparison of these results with that of MoS_2 provides key areas for future improvements.

2. Experiment methods

Micrometer-sized ternary alloys of bulk 2H-phase crystals of $MoS_{2(1-x)}Se_{2x}$ were used in our experiments, as reported elsewhere [12]. The material characterizations were conducted on bulk crystals or exfoliated flakes before the fabrication of any devices. The Raman and photoluminescence (PL) spectroscopy were conducted on few-layer flakes (5–7 nm or 8–10 layers) exfoliated on an oxide substrate (300 nm SiO_2) with a Horiba LabRAM HR spectrometer and an excitation wavelength of 532 nm. The system was calibrated using the silicon peak at 520 cm^{-1}. The laser power was set to less than 1 mW to prevent damage to the flakes. The x-ray photoelectron spectroscopy (XPS) was conducted on bulk crystals using an Axis Ultra DLD spectrometer from Kratos Analytical with a monochromatic Al Kα source. The obtained XPS spectra were calibrated using the adventitious carbon peak (C 1s) at 284.6 eV.

The schematic of the global back-gated FET used in this study is shown in figure 1(a). Thermally grown SiO_2 of 300 nm thickness on p++ silicon was used as the substrate for the initial devices. For subsequent higher performance devices, 30 nm of evaporated HfO_2 [25, 26] on silicon was used as the substrate. These HfO_2 thin films are completely amorphous and do not show any ferroelectric polarization effects, as reported by Bhattacharjee *et al* [27]. Flakes were mechanically exfoliated onto the substrate. Flakes of thickness 5–7 nm were identified by visual inspection and confirmed using atomic force microscopy (AFM—tapping mode, Bruker—Dimension Icon) as shown in figure 1(a). After each process, the samples were cleaned using standard acetone and isopropyl alcohol. Source/Drain contacts were patterned using two-step electron beam lithography (Raith Eline/Pioneer), and nickel metal was deposited by electron-beam evaporation followed by lift-off. Back-gated FETs of channel length (L_G) of 1 μm (devices on SiO_2) and 500 nm (devices on HfO_2) were fabricated.

These FETs were electrically characterized using Keysight B1500 semiconductor device analyzer at ambient conditions with a delay time of 1 ms between each voltage step. The saturation drain currents (I_{DSat}) were normalized for easy comparison between devices with SiO_2 and HfO_2 as gate dielectrics. To account for the different oxide thicknesses, the I_{DSat} was extracted at a common gate field of ~0.67 MV cm^{-1}, which corresponds to 20 V and 2 V gate overdrives for FETs with SiO_2 and HfO_2 dielectrics, respectively. To account for the different channel lengths, the I_{DSat} for devices with HfO_2 ($L_G = 500$ nm) as dielectric were also divided by a factor of 2 for easy comparison with the FETs using SiO_2 ($L_G = 1$ μm).

3. Results and discussion

Raman spectroscopy shows two vibrational modes, the in-plane E^1_{2g} and the out-of-plane A_{1g} modes, similar to pure MoS_2 and $MoSe_2$ (see figure 1(b)) [13]. MoS_1Se_1 shows MoS_2-like modes at 400.9 cm^{-1} and 370.8 cm^{-1} (A_{1g}, E^1_{2g}), whereas these peaks are suppressed in the selenium-rich $MoS_{0.4}Se_{1.6}$. Vibrational modes similar to $MoSe_2$ are observed around 266 cm^{-1} and 222 cm^{-1}, with additional minor/split peaks in the vicinity. Similar Raman spectra were reported for $MoS_{2(1-x)}Se_{2x}$ flakes elsewhere as well [12]. The relative shifts in peak position provide information about strain in the lattice. Substitution of selenium with smaller sulfur atoms in $MoSe_2$ lattice can cause tensile strain, whereas substituting sulfur with larger selenium in MoS_2 can result in compressive strain. Compared to the unstressed lattice, the Raman spectra can shift to a lower wavenumber for tensile stress and towards a higher wavenumber for compressive stress [28]. Both the MoS_2 and $MoSe_2$-like modes of these alloys are at a much lower frequency compared to either pure MoS_2 (A_{1g} 408 cm^{-1}, E^1_{2g} 383 cm^{-1}) [6, 29, 30], or pure $MoSe_2$ (A_{1g} 242 cm^{-1}, E^1_{2g} 286 cm^{-1}) [6], indicating the

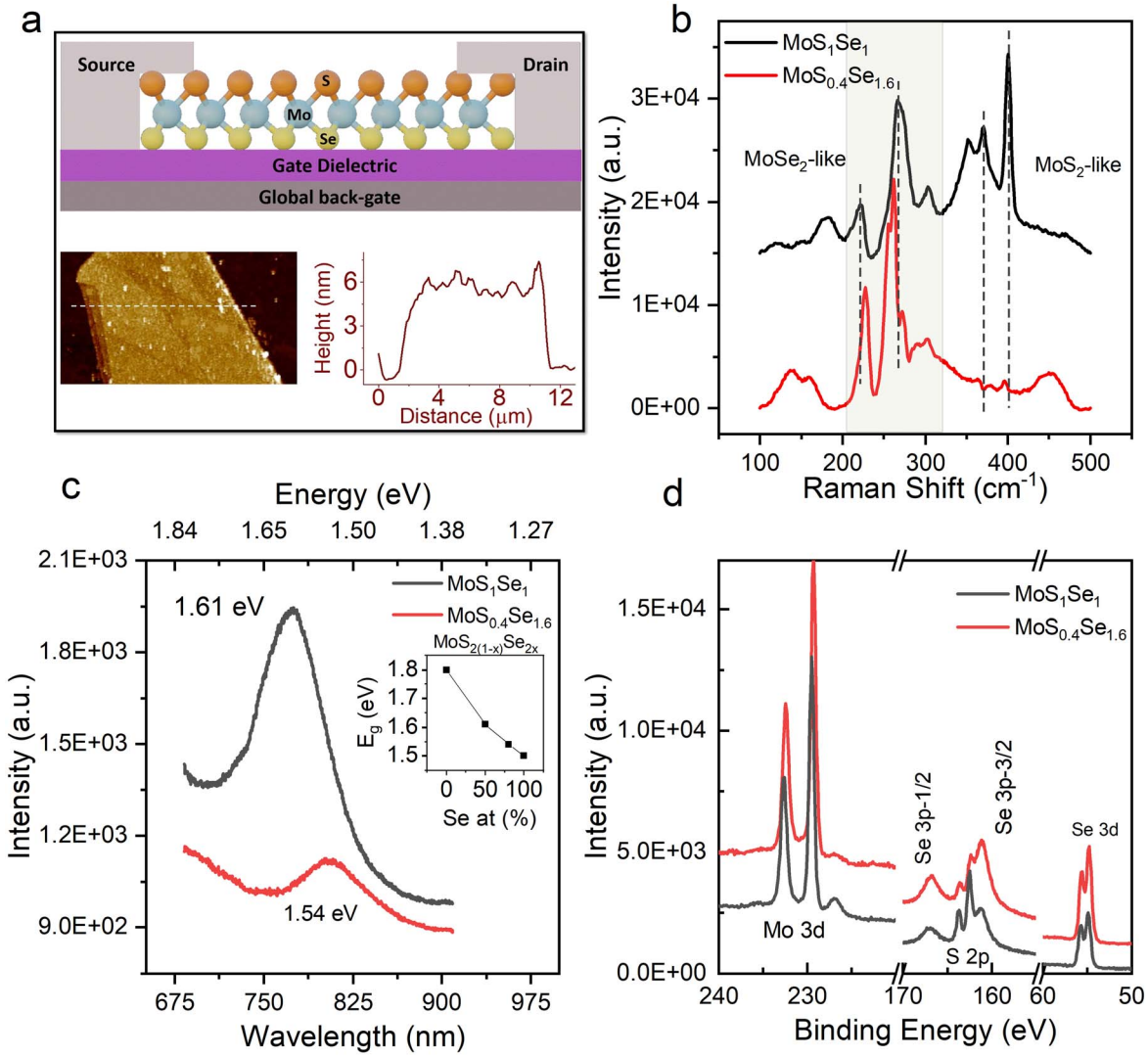

Figure 1. (a) Schematic of the back-gated FET used in this study, (below) AFM image of $MoS_{2(1-x)}Se_{2x}$ flakes, (b) Raman Spectra, (c) PL spectra, inset: optical bandgap v/s atomic concentration, (d) high resolution XPS spectra of MoS_1Se_1 and $MoS_{0.4}Se_{1.6}$.

lattice is under tensile stress compared to them. The shift to lower frequency is often attributed to the interaction between S and Se atoms [17]. However, the split in the MoS_2-like E^1_{2g} mode for MoS_1Se_1 also points towards high strain [30]. MoS_1Se_1 has an equal ratio of sulfur and selenium and is likely to be under the highest strain among other compositions. The strain can also cause defects that increase their catalytic activity, as reported in previous studies [14]. The broader Raman peaks for MoS_1Se_1 are indicative of its high defect density. As the stoichiometry is further changed, the properties of the corresponding alloys can shift closer to either of the pure material. Here, the in-plane $MoSe_2$ like E^1_{2g} mode of $MoS_{0.4}Se_{1.6}$ is blue-shifted from MoS_1Se_1, making it closer to pure $MoSe_2$ structure. However, the corresponding A_{1g} peak splits into multiple peaks, suggesting changes in crystal symmetry as it approaches $MoSe_2$.

The tunable bandgap of $MoS_{2(1-x)}Se_{2x}$ alloys has been reported earlier [13, 15, 31]. Photo-luminescence spectroscopy (see figure 1(c)) was conducted to study the variation in their optical bandgap. MoS_1Se_1 shows a peak at a wavelength of 771.5 nm, whereas the peak is at 803.4 nm for $MoS_{0.4}Se_{1.6}$, indicating an optical bandgap of 1.61 eV and 1.54 eV, respectively. The variation of optical bandgap with the atomic concentration is shown in figure 1 (c, inset), along with the bandgaps of few-layer MoS_2 and $MoSe_2$ for [7]. The bandgap decreases linearly with increasing selenium ratio. At few-layer thickness, the bandgaps are much higher than the bulk values for $MoSe_2$ or MoS_2 (1.1 and 1.2 eV). This behavior was reported in $MoSe_2$, where the bandgap of few-layer flakes was nearly degenerate with their monolayer bandgap [7]. Further study may be required to understand the evolution of bandgap, and its nature, with the number of layers for alloy materials.

We investigated the chemical states of constituent elements using high-resolution XPS conducted on bulk crystals of the alloys, shown in figure 1(d). The Mo $3d_{\frac{5}{2}}$ peak at ~229 eV represents +4 oxidation state of Mo in 2H phase [32]. On MoS_1Se_1, the Mo $3d_{\frac{5}{2}}$ peak is at 229.5 eV and $3d_{\frac{3}{2}}$ is at 232.6 eV. Presence of sulfur is characterized by S $2p_{\frac{3}{2}}$ and $2p_{\frac{1}{2}}$ peaks at 162.5 eV and 163.7 eV, respectively. Selenium

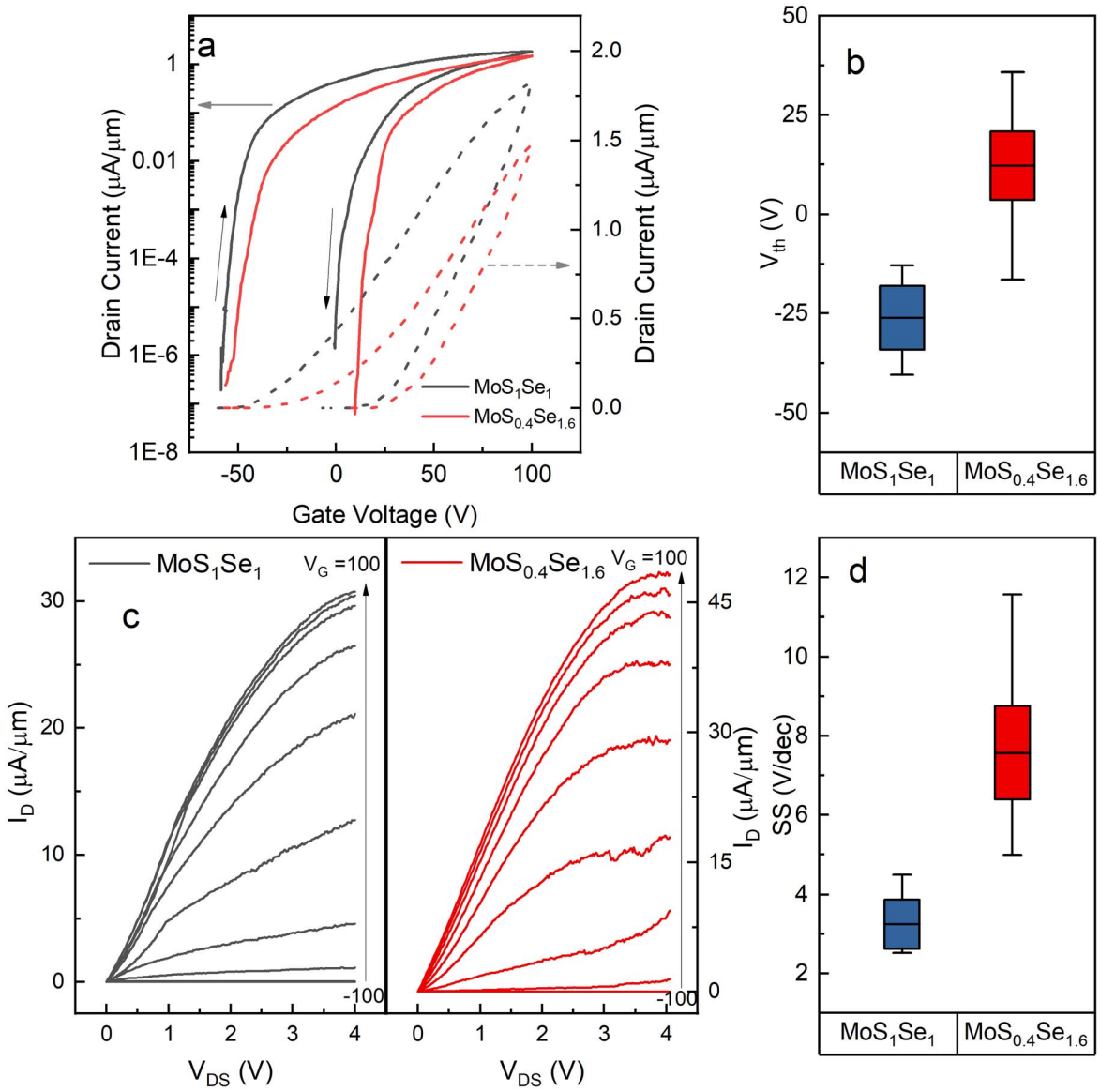

Figure 2. Characteristics of FETs ($L_G = 1$ μm) of MoS_1Se_1 and $MoS_{0.4}Se_{1.6}$ using SiO_2 as dielectric, (a) transfer characteristics at $V_{DS} =$ 100 mV, (b) threshold voltage, (c) output Characteristics, (d) subthreshold slope.

has prominent $3d_{\frac{5}{2}}$ and $3d_{\frac{3}{2}}$ peaks at 54.9 eV and 55.7 eV, respectively, and also shows 3p peaks at 161.2 eV ($3p_{\frac{3}{2}}$) and 167.3 eV ($3p_{\frac{1}{2}}$) which overlaps with 2p peaks of sulfur. The higher ratio of selenium in $MoS_{0.4}Se_{1.6}$ is marked by the higher intensity of its peaks corresponding to Se 3p and 3d orbitals. Further, the spectra are shifted by ∼0.1–0.2 eV to lower binding energy for $MoS_{0.4}Se_{1.6}$, indicating a corresponding shift in Fermi levels towards the valence band [17, 33]. This helps to change the doping concentration with the composition of the alloys and could prove significant for electron devices using these materials.

To study the electrical characteristics of the alloys, we fabricated global back-gated FETs as shown in figure 1(a). First, we fabricated back-gated FETs using 300 nm SiO_2 as the gate dielectric. These devices were used to compare and contrast the electrical characteristics of $MoS_{2(1-x)}Se_{2x}$. Figures 2(a) and (c) shows the transfer characteristics and output characteristics of these FETs. They offer a high ON–OFF ratio $>10^6$ and proper saturation in output characteristics. Although both compositions show clear n-type characteristics and n-channel operation, the threshold voltage (V_{th}) for $MoS_{0.4}Se_{1.6}$ is shifted to much higher gate voltages (figure 2(b)), indicating lower doping concentration. The change in doping is also supported by the Fermi-level shift observed from XPS measurements (shown in figure 1(d)). We estimate the approximate doping concentration from the change in V_{th} and the Fermi level. The threshold voltage for an accumulation type FET is given as [34]:

$$V_{th} = V_{FB} - \frac{Q_{Dep}}{C_{ox}}, \tag{1}$$

where V_{FB} is the flat-band voltage, Q_{Dep} is the depletion charge, and C_{ox} is the gate capacitance. Considering fully

Table 1. Estimated material and interface parameters.

		On SiO_2			On HfO_2		
			Fast interface traps	Slow interface traps		D_{it}	N_{it}
Material	Doping N_D (cm^{-3})	Hysteresis V_H (V)	D_{it} (cm^{-2} eV^{-1})	N_{it} (cm^{-2})	V_H (V)	(cm^{-2} eV^{-1})	(cm^{-2})
MoS_1Se_1	1.2×10^{18}	50.78	3.8×10^{12}	3.6×10^{12}	0.158	5.8×10^{11}	3.5×10^{11}
$MoS_{0.4}Se_{1.6}$	2.3×10^{17}	25.96	9.0×10^{12}	1.9×10^{12}	0.062	1.5×10^{12}	1.4×10^{11}

depleted channel (thickness, $t_{ch} = 5$ nm) while turned off and assuming the V_{th} shift is entirely due to doping, the difference in doping concentrations ($\Delta N_D \sim 10^{18}$ cm^{-3}) is calculated using the equation [34]:

$$\Delta N_D = -\frac{C_{ox}\Delta V_{th}}{qt_{ch}}. \quad (2)$$

Also, considering a Fermi level shift of 0.1 eV (from the XPS) and using the standard Boltzmann carrier density equations, the doping concentrations can be extracted, as shown in table 1.

The subthreshold slope (SS) and hysteresis (V_H) supply information about the interface between the semiconducting channel and the dielectric. The clockwise nature of the hysteresis confirms the dominance of interface traps in the transfer characteristics. $MoS_{0.4}Se_{1.6}$ has significantly worse SS despite having lower carrier density (figure 2(d)). The presence of fast interface traps (D_{it}) degrades the SS. They are short-lived interface traps with lifetimes much lower than the measurement duration. We estimate their density, D_{it}, by the equation:

$$SS = \ln(10)\frac{kT}{q}\left(1 + \frac{C_{dep} + C_{it}}{C_{ox}}\right), \quad (3)$$

where the depletion capacitance (C_{Dep}) is neglected, and $C_{it} = qD_{it}$ is the capacitance due to the interface traps. On the other hand, longer-lived slow interface traps produce hysteresis in the transfer characteristics of the FET. In addition to interface traps, other defects near the interface can also create slow traps and cause hysteresis. Together, we estimate these as the slow interface trap density (N_{it}) using the following relation.

$$V_H = q\frac{N_{it}}{C_{ox}}. \quad (4)$$

The hysteresis values, along with estimated N_{it} (slow) and D_{it} (fast), are summarized in table 1. $MoS_{0.4}Se_{1.6}$ shows twice the D_{it} compared to MoS_1Se_1, whereas N_{it} follows the opposite trend. Studies on hysteresis in MoS_2 FETs have pointed towards multiple factors—extrinsic factors like adsorbed moisture and oxygen [35–38], the presence of intrinsic defects [39], and oxide traps [40–42]. The oxide trap (also called border traps) [43] levels in SiO_2 are long-lived, also contributing to hysteresis [44]. Analysis based on Raman spectroscopy and earlier reports has shown higher strain and more defects in MoS_1Se_1 [14]. These defects can act as intrinsic traps or as sites for gaseous adsorbents, causing larger hysteresis than in $MoS_{0.4}Se_{1.6}$. Despite the greater hysteresis, MoS_1Se_1 shows much better SS, suggesting that most of its traps are of a larger lifetime. The reduction in fast-traps maybe because this is a 2D–3D interface; some of these intrinsic defects may help passivate the dangling bonds at the 3D dielectric. A detailed study is required to understand both the origin and the exact lifetimes of the traps/defects involved in these interfaces. The better SS in MoS_1Se_1 makes it a better candidate for low power switching devices with proper hysteresis control.

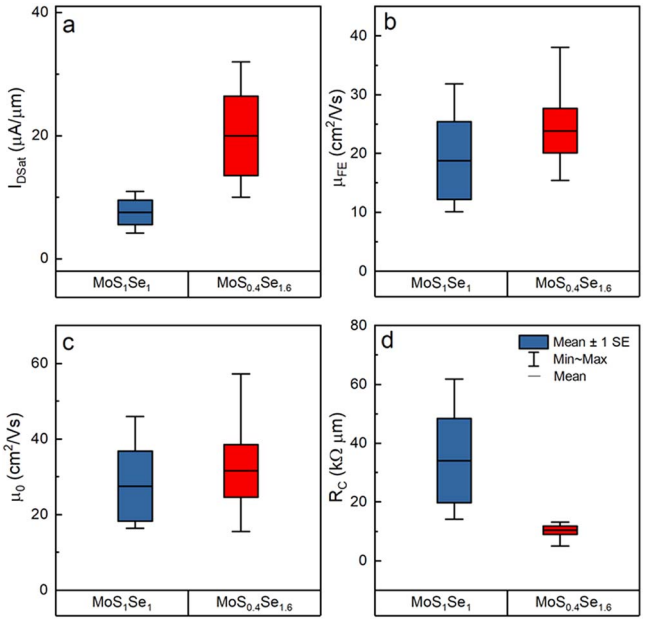

Figure 3. Comparison of electrical characteristics of FETs (L_G = 1 μm) of $MoS_{2(1-x)}Se_{2x}$ on SiO_2 dielectric, (a) saturation current at $V_{ov} = 20$ V, (b) field-effect mobility, (c) intrinsic mobility (excluding effect of R_C), (d) contact resistance (R_C).

To evaluate the FET performance, we extract various metrics such as saturation drain current (I_{DSat}) and field-effect mobility (μ_{FE}). The field-effect mobility often deviates from the actual or intrinsic mobility of the channel due to the effect of resistance at the source and drain contacts. Hence, we use the *y*-function [45, 46] method to extract the intrinsic mobility (μ_0) and the contact resistance (R_C), which are shown in figure 3. $MoS_{0.4}Se_{1.6}$ shows higher drain currents, field-effect mobility, and lower contact resistance. The poorer I_{DSat} and μ_{FE} are partially due to significantly higher R_C of MoS_1Se_1. However, the higher intrinsic mobility of $MoS_{0.4}Se_{1.6}$ also highlights its superior channel properties.

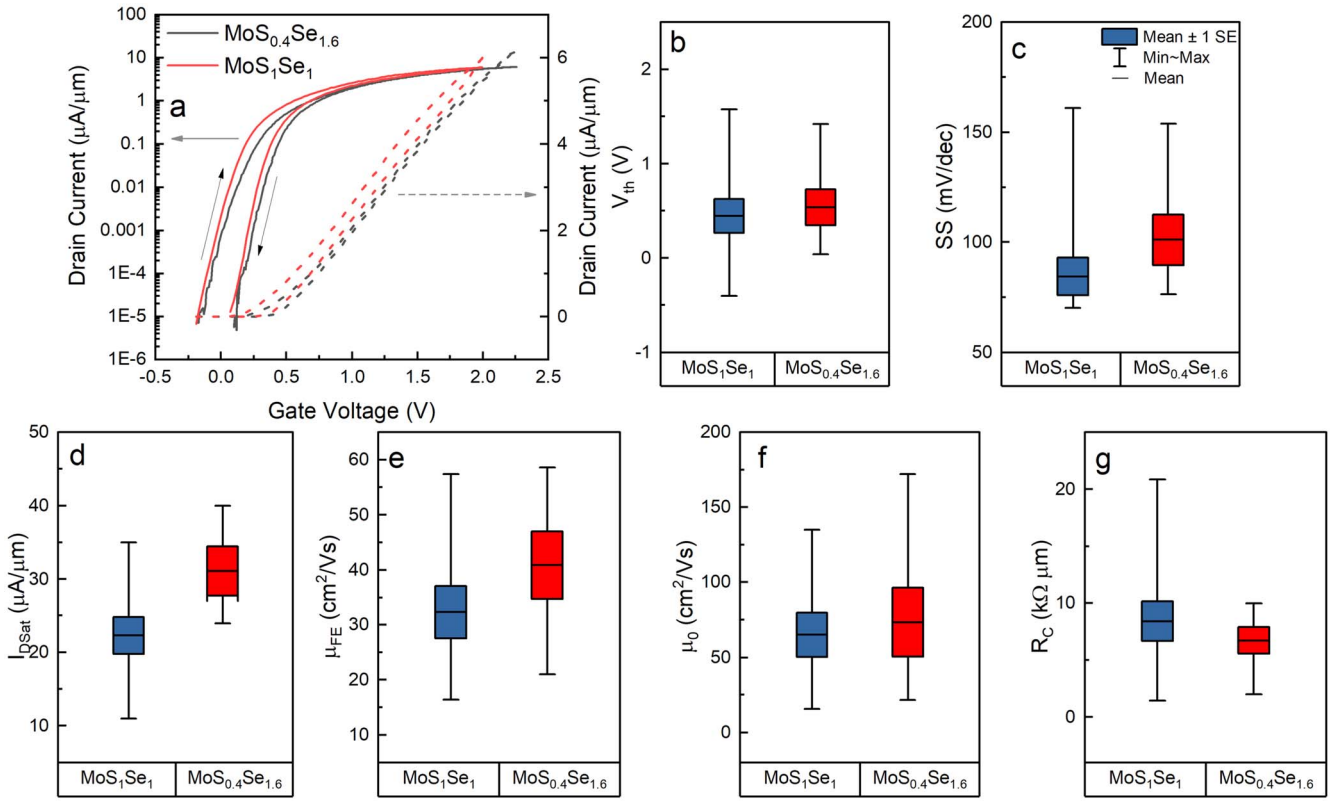

Figure 4. Characteristics of FETs (L_G = 500 nm) of $MoS_{2(1-x)}Se_{2x}$ on HfO_2 dielectric, (a) transfer characteristics at V_{DS} = 100 mV, (b) threshold voltage, (c) subthreshold slope, (d) saturation drain current at V_{ov} = 2 V (scaled down by 2 to normalize the channel length), (e) field-effect mobility, (f) intrinsic mobility (excluding the effect of R_C), (g) contact resistance (R_C).

High-*k* dielectric materials improve the gate coupling and increase the mobility as it screens the charged impurities near the channel [47–49]. We fabricate FETs with hafnium oxide (HfO_2) as the dielectric to reduce the hysteresis and improve device performance. We use a thin HfO_2 of 30 nm thickness which shows good contrast for the flakes [47], and further reduce the channel length to 500 nm to highlight its benefit in device scaling. The enhanced gate coupling of thin HfO_2 ensures that there are negligible short-channel effects at these dimensions. This also ensures that standard MOSFET equations can be used to analyze the characteristics in all the FETs in this study. Figure 4(a) shows the transfer characteristics of the new devices. The devices show enhancement-mode behavior, i.e. positive threshold voltages (figure 4(b)). The clockwise nature of the hysteresis confirms the dominance of interface traps and the absence of any ferroelectric polarization in the HfO_2 dielectric [50]. Also, there is a significant reduction in hysteresis from ∼25 to 50 V to a few hundred millivolts (see table 1). Although this is partially due to the higher oxide capacitance, our calculations show ∼1 order of magnitude reduction in the density of slow interface traps, N_{it}. The SS (figure 4(c)) show remarkable improvements, with the best value of 70.2 mV dec^{-1} on MoS_1Se_1 FET. Calculations suggest ∼1 order of magnitude reduction in the D_{it} (table 1) with HfO_2 dielectric compared to SiO_2. The trends in these characteristics between MoS_1Se_1 and $MoS_{0.4}Se_{1.6}$ remain similar as on SiO_2–MoS_1Se_1 shows lower (fast) D_{it} but higher (slow) N_{it}. Crucial performance metrics were extracted, as mentioned previously, and are shown in figures 4(d)–(g). The saturation current, field mobility, and intrinsic mobility are 2× higher than those using SiO_2 as dielectric and offer low contact resistance of ∼5–10 kΩ μm. Between MoS_1Se_1 and $MoS_{0.4}Se_{1.6}$, the trends in these metrics remain similar to FETs on SiO_2.

To offer a fair comparison with the longer channel length of the FETs with SiO_2 as dielectric, the saturation current in figure 4(d) is scaled down by 2 from the measured values ($I_{DS} \propto 1/L$). The secondary effects of channel length on mobility and other parameters are negligible as long as the device still operates in the long channel regime, which is still valid at 500 nm channel length [51]. The improvements in these parameters, despite being normalized for channel length, is because of the enhanced mobility due to columbic screening from a high-*k* dielectric.

The reduction in both slow and fast interface traps points towards a much better interface of the 2D material with HfO_2 than SiO_2. There are multiple reasons for the reduction in the trap densities. The border traps in the oxides are charged at high gate electric fields [43, 52]. The electric field in FETs with HfO_2 is lower than SiO_2 due to the lower gate voltages required, resulting from its high dielectric constant (higher C_{ox}). Thus the density of border traps (counted among N_{it}) will be lower with HfO_2 than with SiO_2 [53]. Also, *ab initio* studies have shown that impurities and adsorbents, such as hydrogen (H), on SiO_2 can introduce defect states within the bandgap of MoS_2–SiO_2 interfaces [54]. On the contrary, the

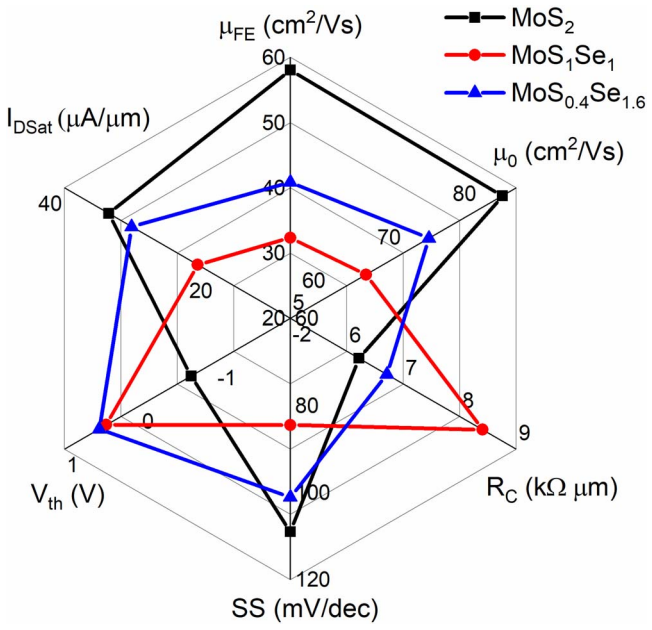

Figure 5. Spider plot comparing performance metrics of FETs on HfO_2.

MoS_2–HfO_2 interface is more stable and does not show prominent gap states [55]. Also, thermodynamically stable defects such as oxygen vacancies and H impurities cause more n-type doping in HfO_2–MoS_2 systems [56]. Assuming similar interfaces for alloys of MoS_2 (i.e. $MoS_{2(1-x)}Se_{2x}$), using HfO_2 as gate dielectric will lower the distribution of gap states for the alloy FETs and reduce the D_{it}. Further improvement in interface trap densities may be possible by integrating 2-D dielectrics such as hexagonal boron nitride (h-BN) [57]. For best performance, this may require a stack of h-BN and a high-k dielectric due to the low dielectric constant of h-BN.

The improved interface of HfO_2-MoS_1Se_1 with a lower density of interface traps helps in reaching a very low SS of 70.2 mV dec^{-1}. Although this value is still higher than the ideal Boltzmann limit of 60 mV dec^{-1}, the gap can be closed by utilizing specific device architectures. A simple upgrade to a double-gated architecture, commonly used to improve the gate control, can boost this SS to near ideal values [58]. Sub-thermionic switching can be achieved using specialized configurations such as Negative Capacitance FETs [59], Tunnel FETs [60], or Gate Tunable Thermionic-Tunnel FETs, [27, 61] etc. The flexibility offered by alloying could further improve the steep SS shown in such devices.

The performance characteristics of FETs (HfO_2 dielectric) are summarized in a spider plot (figure 5) along with a comparison against MoS_2 FETs from our previous studies [62]. Although MoS_2 FETs show higher mobility and saturation current, $MoS_{0.4}Se_{1.6}$ shows comparable values while showing positive V_{th} (enhancement mode) and a lower SS. Thus, they show promise in faster switching applications with comparable performance to MoS_2. MoS_1Se_1 has slight degradation in mobility and drain currents, but its much lower SS makes it suitable for lower power operations. Enhancement-mode or normally-off FETs are essential for CMOS logic circuits. The need for extra device engineering for this is eliminated in these alloys. Although there is a gap in performance with pure MoS_2, it could be mitigated by reducing the contact resistance, using methods such as work-function engineering with different contact metals, surface engineering processes such as sulfur treatment [62, 63], or by doping [64]. Further studies on different alloy compositions may reveal greater tunability in performance metrics and find the sweet spot offering the best of both worlds, i.e. higher drain currents together with lower SS.

Finally, in table 2, we provide a comparison of the electrical characteristics from our study, with other reports on FETs using 2D alloys in literature. To ensure a fair comparison, we limit this to 2D alloys only and avoid their corresponding pure materials. Although all of these studies show tunability in parameters such as mobility, many of them suffer from severe degradation upon alloying, reducing their utility for FETs. The differences in their synthesis methods could also contribute to these variabilities. Most of these reports use only a thick SiO_2 as the gate dielectric, limiting their performance, whereas the integration of HfO_2 in our study shows dramatic performance improvements and allows enhancement mode operation. Further, the $MoS_{2(1-x)}Se_{2x}$ alloys used in our study offer decent mobility and drain currents at all compositions and retains a high On–Off ratio, providing great flexibility for any applications without any significant penalty.

4. Conclusions

A detailed investigation into the performance tunability of FET with 2D alloys of $MoS_{2(1-x)}Se_{2x}$ material has been carried out in this study. These materials are integrated with two different gate dielectrics—SiO_2 and HfO_2, to demonstrate further performance improvements with a high-k dielectric. Raman spectroscopy reveals the presence of tensile strain in both the alloys, higher in MoS_1Se_1. XPS has shown variation in carrier densities which allows tuning the FET threshold voltages with the stoichiometry of the alloys. Hysteresis is larger in FETs with MoS_1Se_1 than $MoS_{0.4}Se_{1.6}$ due to the strain-induced defects. Nevertheless, the former shows a steeper SS. On both the dielectrics, $MoS_{0.4}Se_{1.6}$ delivers higher mobility and drain currents than MoS_1Se_1, whereas the latter is better suited for low power operations due to its steeper subthreshold region. Both the hysteresis and the SS are improved using high-k HfO_2, which provides an order of magnitude reduction in interface trap densities at the dielectric-semiconductor interface. Also, there is a 2× improvement in mobility and drain currents with HfO_2. Unlike the typical behavior in MoS_2, the positive threshold voltages (with HfO_2 dielectric) of the alloy FETs help to realize normally-off (enhancement-mode) FETs necessary for CMOS operation. This study demonstrates that alloying of 2D materials is a powerful technique to tune the transistor performance for CMOS applications. The superior electrical characteristics of FETs and the investigation into the use of

Table 2. Comparison with other reported 2D alloy FETs.

Material	Gate dielectric	Transport type	On–Off Ratio	I_{DSat} (μA μm^{-1})	Mobility (cm^2 V^{-1} s^{-1})	V_{th} (V)	References
$MoS_{2(1-x)}Se_{2x}$	SiO_2 (300 nm)	n	10^7	7.5–20	19–24	−26 to 12.24	This work
$MoS_{2(1-x)}Se_{2x}$	HfO_2 (30 nm)	n	10^7	61–75	32.3–40.8	0.62 to 0.82	This work
$SnSe_{2(1-x)}S_{2x}$	SiO_2 (300 nm)	n	1.4–4000	0.2–20	71.3–2.3	—	[10]
$MoS_{2(1-x)}Se_{2x}$	SiO_2 (270 nm)	n	10^5	0.4–3	0.1–0.4	−22 to −27	[13]
$WS_{2x}Se_{2(1-x)}$	SiO_2 (300 nm)	p to n	10^6	—	0.4–0.03 (n), 0.48–0.09 (p)	−50 to 50	[24]
$MoSe_{2x}Te_{2(1-x)}$	SiO_2 (300 nm)	ambipolar	10^7	8	2.82	—	[23]
$W_{1-x}Re_xS_2$	SiO_2 (300 nm)	n	—	0.2	0.4	—	[22]
$WS_{2x}Se_{2(1-x)}$	SiO_2 (300 nm)	p to n	10^5–10^8	10	5.3–68 (p), 0.9–11.8 (n)	—	[65]
$Mo_{1-x}W_xSe_2$	SiO_2 (300 nm)	n	$>10^5$	1	0.003–0.2	—	[66]

high-*k* dielectrics differentiate this study from other reported literature.

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Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

ORCID iDs

Sooraj Sanjay https://orcid.org/0000-0003-4252-4817
Kolla Lakshmi Ganapathi https://orcid.org/0000-0002-8693-5733
Eswaraiah Varrla https://orcid.org/0000-0003-0246-0695
Navakanta Bhat https://orcid.org/0000-0003-4364-1767

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