ANALYSIS OF A CLASS OF PWM SINEWAVE INVERTERS WITH BIGH FREQUENCY LINK

S.R. Narayana Prakash
B .R. Iyengar

Department of Electrical Engineering
Indian Institute of Science
Bangalore 560 012, INDIA

P.V. Ananda Mohan

Digital Group, Transmission R&D
Indian Telephone Industries Ltd.
Bangalore 560 016, INDIA

ABSTRACT

In this paper the salient features of four different topologies of low frequency sinewave inverter with high frequency link and PWM control is presented. The inverters employ ferrite cored transformers, inductors, resonant filters tuned to switching frequency ($\geqslant$20 kHz) and power MOSFETs resulting in compact design. Equivalent circuit approach is used for analyzing all the four topologies and computer simulation. The method of synthesizing the sinusoidal PWM waveform, as well as estimation of total harmonic distortion and response of the low pass filters using discrete time domain analysis are presented along with relevant graph:; and waveforms.

INTRODUCTION

The significant developments in the application of digital computers particularly the personal computer;, has enhanced the demand for reliable uninterruptible power supply systems in which the inverters form an important part apart from the batteries and chargers. In many applicatio:s, features such as high pcwer to weight r.tio, low total harmonic content, fast response, high efficiency & reliabilitv, lower cost and negligible audible noise ope ainn are desired. These features have been realized in the P.W.M. and resonant type of inverters with high frequency link [:-12].

In Topology I [5] of Fig. 1, commutation tor unfolding of. the alternate half cycles of the low frequency output voltage is accomplished with a pair of switches on the sscondary side of the high frequency ferrite cored transformer TF1. While the PWM control is quite simple, the commut.tion of these switches, with isolated gate drive was quite involved. This problem has been overcome in the sinewave inverter. Topology II [6] shown in rig. 2 wherein the process of high frequency rectification and commutat on at low frequency is integrated intc a single stage with a pair of MOSFETs operating as s/nchronous rectifiers. The fast recovery diodes on the transformer secondary (Pig. 2) connected in series with the MOSFETs prevent the Source to Drain body diodes from conducting during the off time of the respective MOSFETs. In topologies I and II the duration of energy trans er from the DC power source at the input to the load is restricted to only 50% of the switching period, with a maximum duty ratio of 0.5. The inverter capacity can be urther enhanced by incorporating the push-pull configuration fopology III and IV [7] as shown in Figs. 3 and 4 respectively. The ener jy transfer can now b. extended upto 90% of the switching period while each of the switches on the primary side of TF1 conduct for only 45% of the total period. If the switching frequency is maintained at 50 kHz, the frequency of the ripple current through the inductor L_1 in topologies III arid IV will be 100 kHz which corresponds to twice the frequency of ripple current in topologies I and II resulting in considerable reduction of the filter component size and ratings. The improvement in the utilization factor of transformer TF1 and the reduction of the filter ratings is thus achieved in Topologres III end IV. The salient features of the four inverter topol>gies are briefly presented.

PRINCIPLE OF OPERATION

Topology I: The schematic of the single phase PWM sinewave inverter is shown in Fig. 1. The input filter is provided to reduce the ripple current from the DC voltag. source. The output of this filter is switched by Q1, driven by sinusoidally modulated PWM pulses P1 at a high frequency F_c, to achieve reduction in the size of the transformers, inductors and filter components. The PWM drive pulses for Q1 are obtained from the pulse width modulator control circuit which will be described later.

During the 'ON' time of Q1, energy is transferred from the input DC voltage source to the load as well as to inductor L1 via TF1 and diodes D2 or D4 depending upon the conduction of the commutating switches Q2 and Q3. The energy stored in L1 is freewheeled through the load via D3 & Q2 or D5 & Q3 during the 'OFF' time of Q1. The flux level in TF1 is forced to zero during the off time of Q1 by the flux reset winding NP2 aid D1. The inductor L1, in addition to storing the energy, forms a low pass filter in combination with the capacitor C1. To filter out the higher order harmonics, the cut off frequency of this LC filter is fixed at about one decade less than the switching frequency F_c. The amplitude of oscillation corresponding to $1/2\pi\sqrt{L1C1}$ is controlled by the damping resisto: R1, in series with C1.

The harmonic voltage at frequency F_c is attenuated further by the parallel resonant filter L2C2 anti the series resonant filter L3C3 each of them tuned to frequency F_c so that the the resulting output voltage across the load will approximate the reference modul ting signal with very low harmonic content. The full wave rectified voltage waveform with low harmonic content so obtained is unfolded across the load to yet a sinusoidal output voltage by switching on Q2 and Q3 during alternate half rycles of the reference modulating signal. The duration of conduction of Q2 and Q3 driven by

drive pulses P2 and P3 respectively is decided by the zero cross over points of the reference sinusoidal signal as shown in Fig. 1. In order to prevent the ferrite cored pulse transformer (not shown in figure), providing isolated gate drive to Q2 & Q3, from going into saturation due to extended 'ON' time, the effective gate source capacitance of the respective MOSFETs is refreshed periodically for the duration of conduction at the rate of 10 times F_c.

This inverter (Fig. 1) can be visualized as being equivalent to two identical transformer coupled buck type of DC-DC converters each of them feeding a resistive load during alternate half cycles of the reference modulating signal. It is known that in a transformer coupled buck type of DC-DC converter, the output voltage is propcrtional to the product of the input DC voltage, the transformer turns ratio and the duty cycle 'D' (defined as the ratio of the 'ON' time to the total switching period $1/F_c$). Since the transformer turns ratio is fixed, by changing 'D' the voltage transformation ratio can be varied. If the value of 'D' is varied continuously such that it is proportional to the instantaneous value of the reference modulating signal (viz. a full wave rectified 50 Hz sinewave) at the midpoint of each of the sampling periods corresponding to $1/F_c$, the average output voltage across the load for a given input DC vcltage will closely follow the reference modulating signal. The negative feedback used to obtain pulse width control ensures good output voltage regulation for input DC voltage as well as load variations.

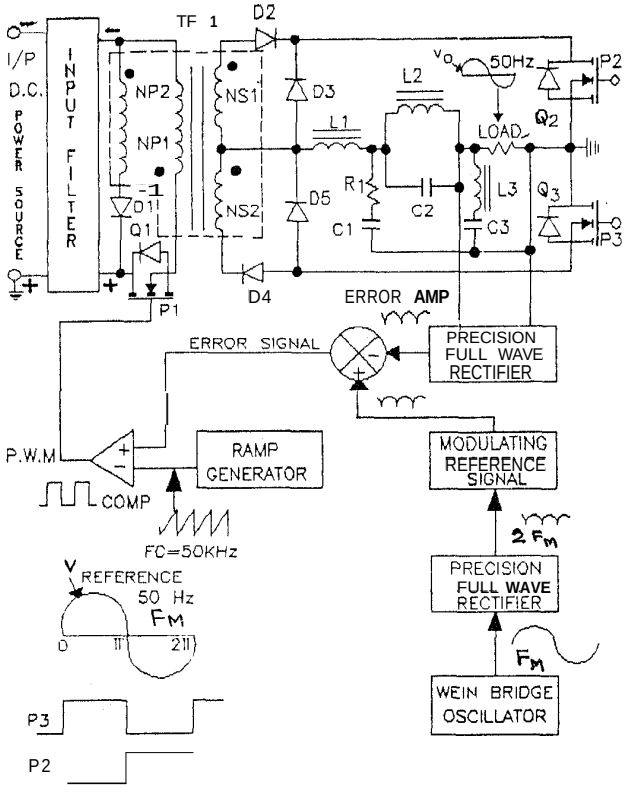


Figure 1: Inverter Topology I with Load Side Commutation

PWM Drive Pulse Generaticn

The sinusoidal voltage across the load is rectified by the precision full wave rectifier [4] and is compared with the modulating signal to obtain on error voltage proportional to the instantaneous difference of the two signals. This is compared with the carrier voltage ramp at frequency F to generate sinusoidal PWM signals.

The operating flux density of TF1 is a function of the input DC voltage and operating frequency F_c for a given transformer core geometry and the number of turns. This permits the fundamental frequency F_M of the sinusoidal output voltage of the inverter to be varied over wide range without varying its amplitude. In order to maintain good output voltage regulation within the specified limits, the value of L1 must be determined at the minimum input voltage and load. However, the physical size of L1 is decided by its peak current at full load so that it remains unsaturated.

It is possible to increase the duty ratio of Q1 beyond 0.5 by reducing the number of turns of the flux reset winding NP2 which results in lower RMS primary current and reduction in input capacitance for the same hold up time, increase of the voltage across the primary winding during the off time and hence higher voltage stress across Q1. For a given transistor breakdown voltage, the maximum permissible duty ratio is decided by the maximum input DC voltage. The transistor Q1 and fast recovery diodes are provided with suitable snubber circuits to reduce the power dissipation in the devices and the voltage spikes at the output.

Topology 11: In the topology shown in Fig. 2, the filtered input DC voltage is switched by Q1, driven by the sinusoidally modulated PWM pulses P1 at a frequency F_c. The method of generating sinusoidally modulated PWM pulses P1 and the process of filtering higher order harmonics of the output voltage are similar to Topology I. However, the scheme of high frequency rectification and commutation at modulating frequency is different from Topology I.

The modes of operation, during the positive and negative half cycles of the output voltage are identical wherein Q1, Q5, D5, Q4, D4 and Q1, D2, Q2, D3, Q3 operate during the respective half periods. The process of energy transfer from the DC source to the load and waveshaping is explained with respect to the positive half cycle which holds good for the negative half cycle as well. During the 'ON' time of Q1, the energy from the source is transferred to the load and a part of it is stored in L1 via TF1, Q5, D5 and filter L2C2 while Q4 is 'OFF'. The energy stored in L1 is freewheeled through the load via Q4, D4 and filter L2C2 when Q1 and Q5 are 'OFF'. The MOSFET pairs Q1 and Q5 function as synchronous rectifiers during the positive half cycle of the output voltage. The PWM drive pulse P5 to Q5 and the inverted PWM drive pulse P4 to 44 are given only during the positive half cycle as shown in Fig. 2. When the 'ON' time of Q1 and Q5 (at low duty ratio) is negligible, 44 has to conduct for nearly the entire switching

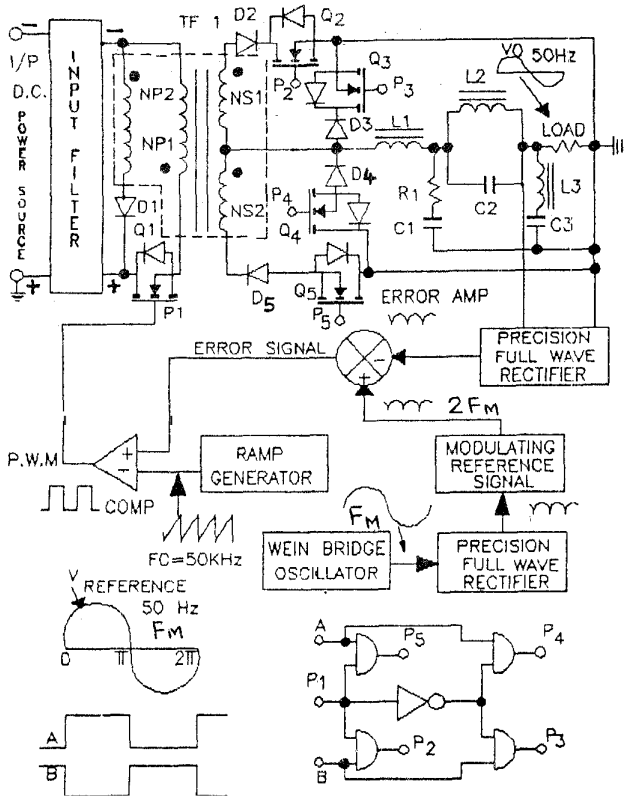


Figure 2: Inverter Topology II with Integrated Synchronous Rectification and Commutation

period $1/F_c$ and hence its effective gate scurce capacitance is refreshed petiodically via pulse transformer as explained earlier in Topology I, The flux level in TF1 is forced to zero during the 'OFF' time of Q1 by the flux reset winding NP2 and diode D1.

During the negative half cycle of the output voltage, devices D2, Q2, D3 and Q3 operate in place of Q5, D5, Q4 and D4, while Q1 continues to perform as explained earlier for positive half cycle. The MOSFETs Q1and Q2 act as synchronous rectifiers during the negative half cycle. The diodes D2-D5 prevent the Source-Drain body diodes of the MOSFETs from conducting during the off time of the respective MOSFETs Q2-Q5. The direction of flow of current through the load during each half cycle of the reference signal is made Opposite by operating the Q1, Q5, D5. Q4, D4 and Q1, Q2, D2, Q3, D3 group of switches alternately resulting in sinusoidal output voltage across the load. A finite idle period is provided by blanking drive pulses at the zero cross over points to ensure that the outgoing group of switches are completely off before the incoming group of switches are turned on.

Topology III: The schematic of the single phase PWM push-pull sinewave inverter of topology III is shown in Fig. 3. The filtered input DC voltage is switched by the MOSFETs Q1 and Q2, driven by the sinusoidally modulated pulses P1 and P2 respectively, at frequency F_c. The switching frequency is maintained at 50 kHz in order to reduce the size of the transformers, energy storage inductor and filter components. These sinusoidally modulated PWM drive pulses are obtained from the PWM control circuit as shown in Fig. 3 .

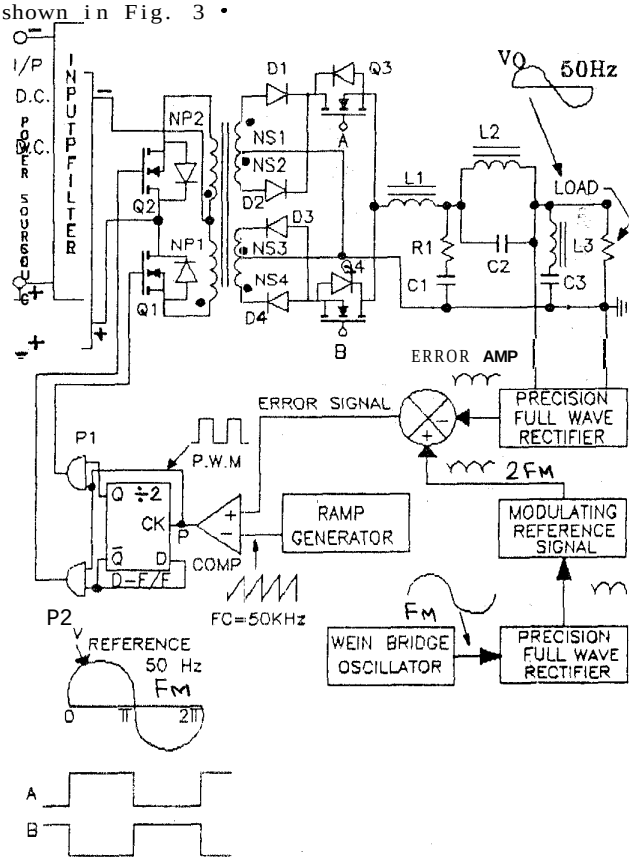


Figure 3: Inverter Topology III with Push-Pull Configuration and Load Side commutation

The modes of operation during the positive and negative half cycles of the output voltage are identical wherein Q1, Q2, D1, D2, Q3 operate during the positive half cycle and Q1, Q2, D3, D4, Q4 operate during the negative half cycle of the output voltage. The process of energy transfer and waveshaping is explained with respect to the positive half cycle which holds good for negative half cycle as well. During the positive half cycle, when Q1 is turned 'ON', energy from the source is transferred to the load and a part of it is stored in L1 via TF1, D1, Q3 and filter L2C2 while Q2 is 'OFF'. This energy in L1 is freewheeled through the load via D2, Q3 and L2C2 when both Q1 and Q2 are off and diode D1 is reverse biased. Similarly when Q2 is turned 'ON' energy is transferred from the source to the load via TF1, D2, Q3 and L2C2. The stored energy in L1 is freewheeled through the load via D1, Q3 and L2C2 when Q1 and Q2 both are 'OFF' and D2 is reverse biased.

During the negative half cycle of the output voltage, devices D3, D4 and Q4 operate in place of D1, D2 and Q3, while Q1 and Q2 continue to operate as during the positive half cycle. The duration of conduction of Q3 and Q4

are controlled by the gate pulses A and B respectively. Similar to Topology I and II, the effective gate-source capacitance of Q3 & Q4 (with transformer coupled gate drive and extended 'ON' time) is refreshed periodically. A finite idle period is provided to ensure that Q3 is completely 'OFF' before Q4 is turned 'ON' and vice-versa in order to prevent a short circuit across the secondary of the transformer.

Topology IV: The schematic of inverter topology IV is shown in Fig. 4. The process of energy transfer from the source to the load when either of Q1 or Q2 is 'ON', freewheeling of the energy stored in L1 through the load during the 'OFF' time of Q1 & Q2, waveshaping of the output voltage and closed loop control remain same as in topology III. The functions of diodes D1-D4 and commutating switches Q3 and Q4 (operating at the fundamental frequency) of topology III have been integrated into the synchronous rectifiers as explained in topology If. The MOSFET pairs Q1 & Q3 and Q2 & Q4 form synchronous rectifiers for operation during the positive half cycle while fast recovery diodes D1 and D2 prevent the drain-source body diodes of Q3 and Q4 from conducting during the off time of the respective MOSFETs. Similarly, the MOSFET pairs Q1 & Q5 and Q2 & Q6 form the other set of synchronous rectifiers during the negative half cycle. The fast recovery diodes D3 and D4 prevent the conduction of the drain-source body diodes of Q5 and Q6 from conducting during the 'OFF' time of the respective MOSFETs. The method of generation of the drive pulses to Q3,Q4,Q5 and Q6 is shown in Fig. 4.

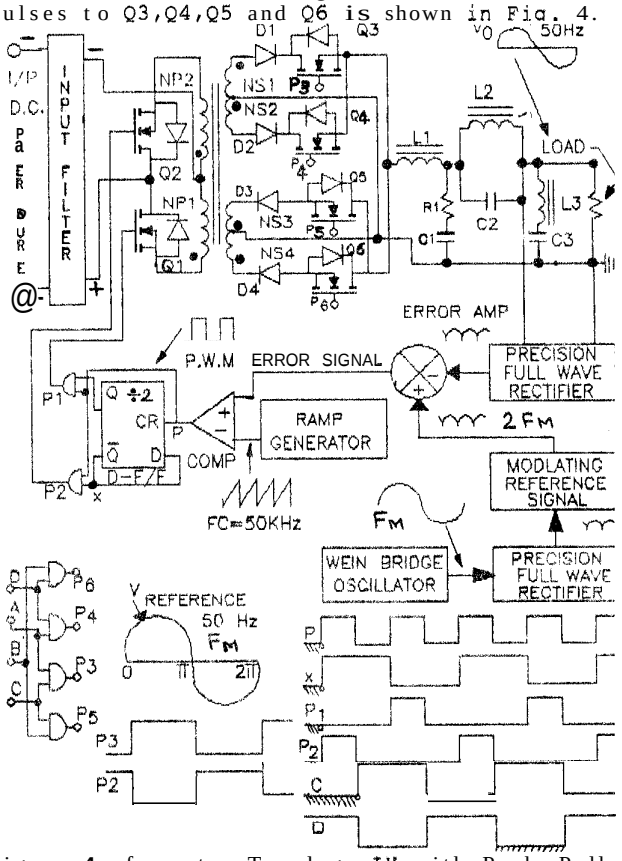


Figure 4: fnverter Topology IV with Push-Pull Configuration and Synchronous Rectifiers

ANALYSIS OF EQUIVALENT CIRCUIT

The input voltage is switched and transformed to the required voltage level E by transformer TF1 operating at switching frequency F_c (50 kHz) in all the four inverter topologies. The sinusoidally modulated PWM pulses are applied to the low pass filter on the secondary side of TF1 to obtain the required sinusoidal output voltage across the load by commutating the relevant group of switches in corresponding inverter topologies. The equivalent circuit shown in Fig. 5

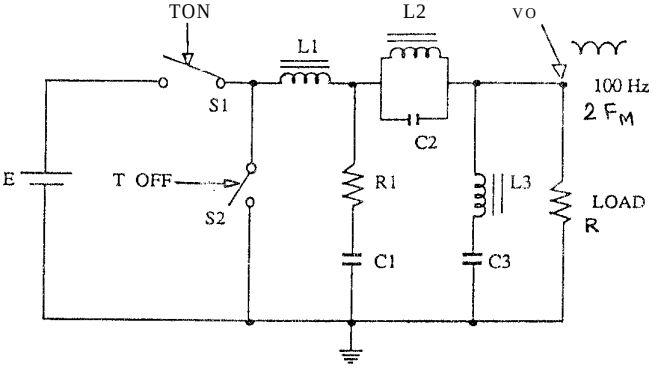


Figure 5: Equivalent Circuit Representation of all the Four Inverter Topologies

represents all the four inverter topologies except For the difference that the ripple current through the inductor L1 will be at the switching frequency F_c in Topologies I and II whereas it will be $2F_c$ in Topologies 111 and IV. It is aspumed that with the low pass filter comprised of L1, R1 and C1 having a cutoff frequency at about one decade less than the frequency of the ripple current through L1, the content of the higher order harmonics of the ripple current will be negligible, Further it has been shown in Fig. 7 that with sinusoidal modulation and high FC/FM ratios the total harmonic distortion without blanking pulses will be negligible. This implies that the current through the load resistor will essentially be a sinewave. Thus the equivalent circuit shown in Fig. 5 is further simplified to the one shown in Figure 6. This equivalent circuit is mathematically modelled as follows.

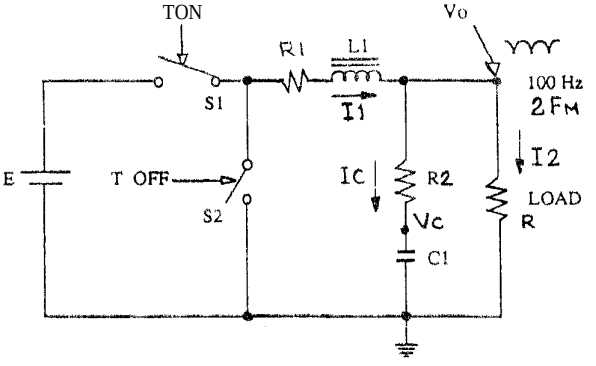


Figure 6: Simplified Equivalent Circuit

Assumptions:

1. The sampling frequency F_c is much higher than the modulating signal $2F_M$.
2. The current through the inductor L1 is continuous.
3. The voltage drop across the switches and their turn on, turn off time is negligible and hence assumed to be zero.
4. The input DC voltage source is ideal.

(a) Mode 1: For T_{ON} duration, S1 is closed, S2 is open and the applied voltage to the network is E.

(b) Mode 2: For T_{OFF} duration, S1 is open, S2 is closed and applied voltage to the network is zero.

Assuming the initial current through the inductor $I_1((n-1)T)$ and capacitor voltage $V_c((n-1)T)$ to be zero, the inductor current $I_1(nT)$, output voltage $V_o(nT)$, capacitor current $I_c(nT)$ and capacitor voltage $V_c(nT)$ can be calculated at any instant of time 'nT' by the following set of equations during both modes of operation.

$$I_1(nT) = \frac{E + I_1((n-1)T).L/T - V_c((n-1)T).R/(R+R2)}{R1 + (L/T) + (R.R2)/(R+R2)}$$

$$V_o(nT) = I_1(nT).(R.R2)/(R+R2) + V_c((n-1)T).R/R+R2$$

$$I_2(nT) = V_o(nT)/R$$

$$I_c(nT) = I_1(nT) - I_2(nT)$$

$$V_c(nT) = V_c((n-1)T) + I_c(nT).T/C$$

where $T \ll T_{ON}$ for mode 1 and

$T \ll T_{OFF}$ for mode 2.

$T_{ON} + T_{OFF} = 1/F_c$

The duration of conduction of switches S1 and S2 for T_{ON} and T_{OFF} periods respectively is calculated from the required duty ratio during each sampling period $1/F_c$ such that the averaged voltage for a given input DC voltage E is equal to the instantaneous value of the reference modulating signal at the mid point of the corresponding sampling period. This follows the assumption that the reference modulating signal is a staircase waveform with N number of unequal steps where N corresponds to FC/2Fm and the duration of each step is equal to 1/FC. Since the magnitude of each of these steps varies continuously proportional to the instantaneous value of the modulating signal. at the mid point of the corresponding sampling period, the duty ratio also changes sinusoidally for a given input voltage E. Thus the required sinusoidally modulated PWM pulses are synthesized over a period of the reference modulating signal corresponding to 1/2FM. The magnitude of the individual harmonics and the total harmonic distortion (% THD) is calculated by determining the Fourier coefficients for a given fundamental frequency FM and sampling frequency FC.

In order to ensure that the outgoing group of switches on the secondary side of TF1 in each of the inverter topologies are completely turned off before the incoming group of switches are turned on a? the zero cross over points of the sinusoidal output voltage, a certain number of pulses on either side of the zero cross over points needs to be provided to prevent any short circuit on the secondary side.. This leads to an increase in the total harmonic content in the sinusoidal output voltage. In the waveform synthesis and Fourier analysis as detailed earlier, these desired blanking pulses have been taken into account. The graph shown in Fig. 7 shows that for a given FC/FM ratio, the % THD varies with the increase in the number of blanking pulses per half cycle of the sinusoidal output voltage.

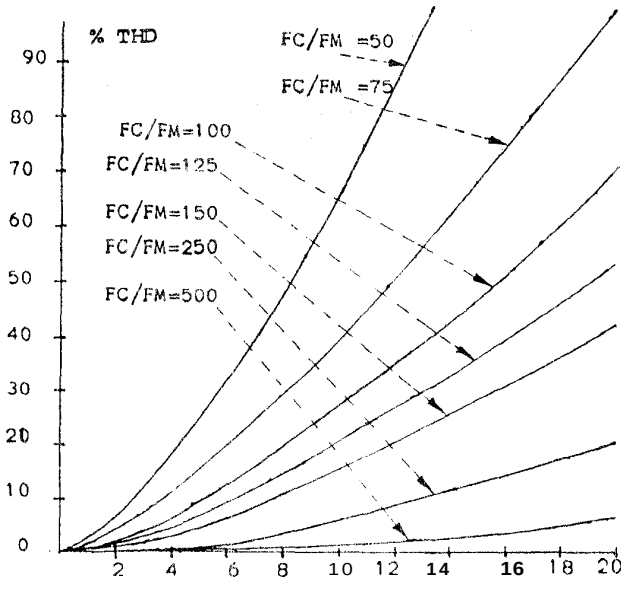


Fig. 7

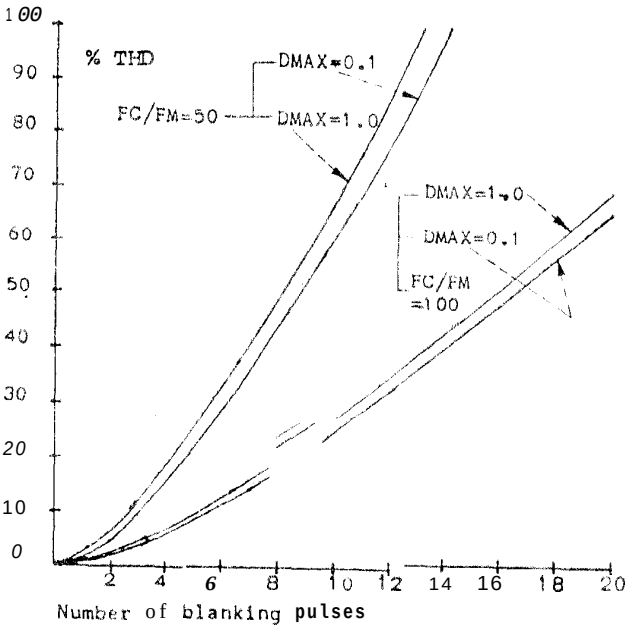
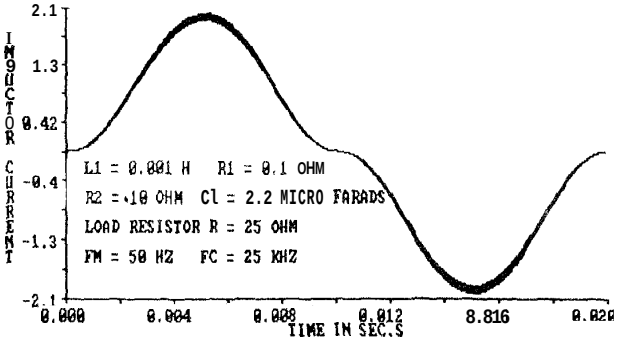
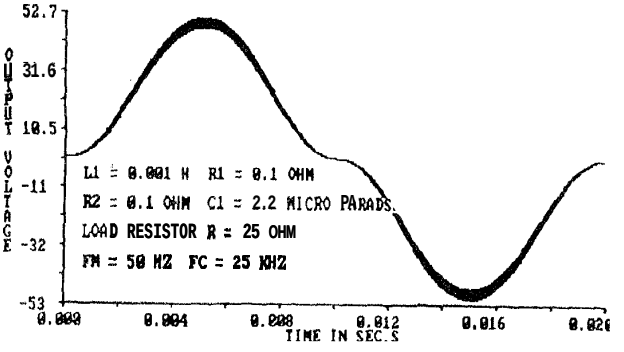
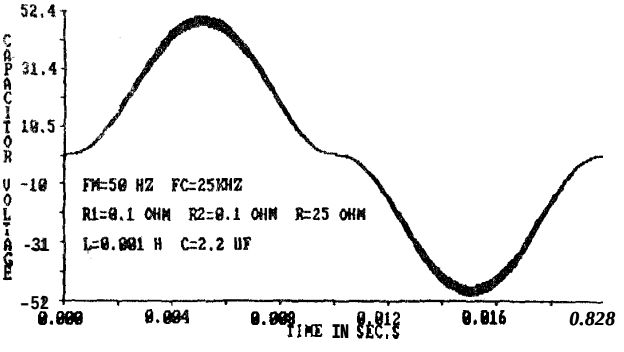


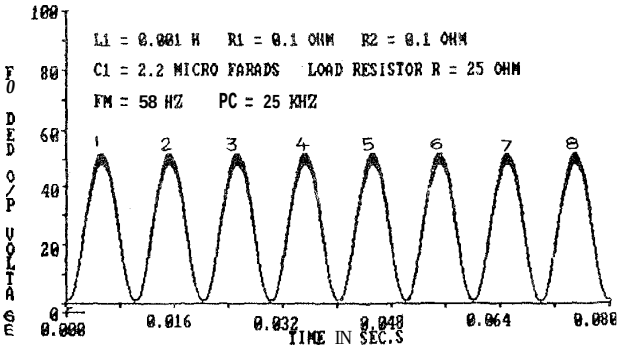
Fig. 8

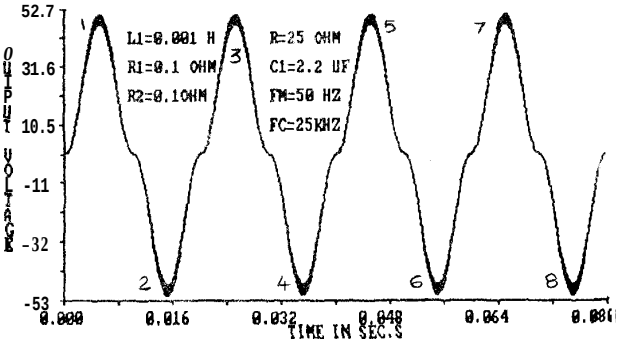
Also it may be noted that with the increasing FC/FM ratio, the % THD decreases for a given number of blanking pulses. In Fig. 8, the variation of % THD vs. number of blanking pulses is shown fcr maximum duty ratios of D_{MAX} = 0.1 & 1.0. The factor D_{MAX} indicates the maximum duty ratio for which the inverter is to be designed at minimum input voltage and maximum load. It is interesting to note that if the inverter is designed for a maximum duty ratio D_{MAX} anywhere between 0.1 and 1.0 there is not much variation in % THD for a given number of blanking pulses and F_C/FM ratio. The graphs shown in Figs. 7 and 8 can be used as design guidelines while selecting the sampling frequency FC, the required number of blanking pulses and the maximum duty ratio, for a given fundamental frequency FM.











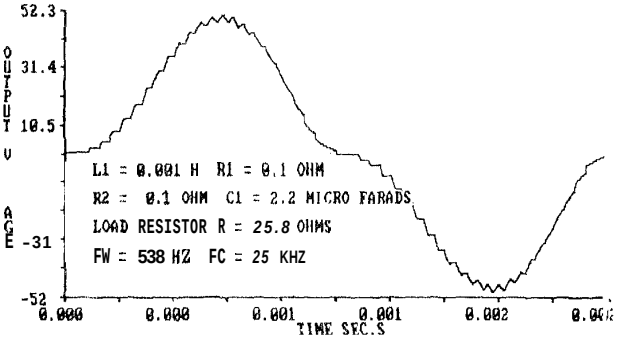


Figure 9: Voltage and Current Waveforms from Simulation

Fig. 9 shows some of the relevant waveforms obtained after PWM waveform synthesis. Fourier analysis and computation of the transient response to illustrate the accuracy of the model and the usefulness of the digital computer simulation *of* the inverter equivalent circuit. In Fig. 10, the output voltage waveform obtained from the prototype of the inverter Topology I is shown for comparison.

CONCLUSIONS

The principle of operation of four PWM inverter topologies **have** been described. An equivalent circuit which represents all the four topologies is derived and the method of **analysis** to determine the response in discrete

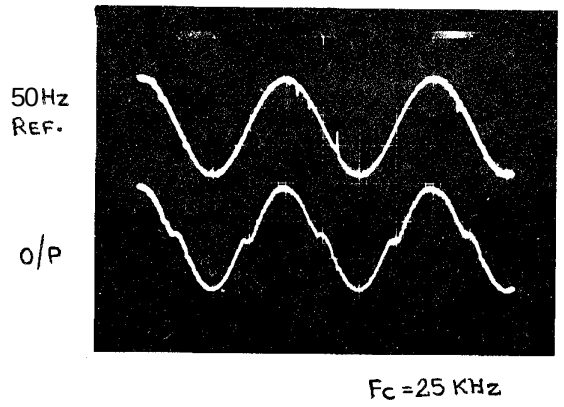


Figure 10: Output Voltage Waveform from Experimental Results

time domain is explained with reference to a simplified equivalent circuit. The procedure for synthesizing the sinusoidally modulated PWM pulse waveform and determining its % total harmonic content is explained in brief. The relevant waveforms generated with computer graphics from simulation illustrate the accuracy of the model of the inverter topologies. The graphs indicating the variation of the % total harmonic distortion with the number of blanking pulses and the sampling to fundamental frequency ratio FC/FM can be used as guidelines for designing PWM inverters with these four new inverter topologies.

REFERENCES

1. B.D. Bedford, R.G. Hoft, 'Principles of Inverter Circuits', John Wiley & Sons Inc., New York, 1964.

2. S.B. Dewan, A. Straughen, 'Power Semi Conductor Circuits', John Wiley & Sons, New York, 1975.

3. Duncan, A. Grant, John Gowar, 'Power MOSFETs - Theory and Application', John Wiley & Sons Inc., (Wiley-Interscience), New York, 1989.

4. Fredrick W. Hughes, 'Op-Amp Handbook', 2nd Edition, Prentice Hall, Englewood Cliffs, New Jersey, 1986.

5. S.R. Narayana Prakash, P.V. Ananda Mohan, B.S.R. Iyengar, 'Low frequency sinewave inverter using ferrites', Paper identification No. 313, Proc. of the 3rd European Conf. on Power Electronics and Applications, Aachen, West. Germany, Oct. 9-12, 1989.

6. S.R. Narayana Prakash, P.V. Ananda Mohan, B.S.R. Iyengar, 'A new sinewave inverter with high frequency link and synchronous rectification using power MOSFETs', IEEE Power Electronics Specialists Conf., San Antonio, Texas, U.S.A., June 11-14, 1990.

7. S.R. Narayana Pr-akash, P.V. Ananda Mohan, B.S.R. Iyengar, 'A novel high frequency PWM inverter generates sinusoidal output voltage at 50 Hz', Presented at the IEEE International Telecommunication Energy Conf., Orlando, Florida, U.S.A., Oct. 21-25, 1990.

8. R.D. Middlebrock, S'Cuk, 'Advances in switched mode power conversion', Vol. I, II and III, Tesla & Co., Pasadena, California.

9. R.L. Steigarwald, et al., 'Applications of power transistors to residential and intermediate rating photovoltaic array power conditioners', International Semiconductor Conf. Record IEEE/IAS, 1982, pp. 84-96.

10. Alan Cocouni, S'Cuk, R.D. Middlebrook, 'High frequency isolated 4 kW photovoltaic inverter for utility interface', Proc. of the 7th International PCI '83 Conf., Sept. 13-15, 1983.

11. A.K.S. Bhat and S.B. Dewan, 'Analysis and design of a high frequency link resonant converter using LCC type commutation', IEEE/PESC Record 1986, pp. 359-366.

12. A.K.S. Bhat and S.B. Dewan, 'Analysis and design of a high-frequency link DC to utility interface using square wave output resonant inverter', IEEE/PESC Record, 1986, pp. 333-342.