A NEW GATE DRIVE CIRCUIT FOR MOSFETS SWITCHING AT LOW FREQUENCY

S.R. Narayana Prakash
B.S.R. Iyengar

Department of Electrical Engg.
Indian Institute of Science
Bangalore 560 012, INDIA

P.V. Ananda Mohan

Digital Group, Transmission R&D
Indian Telephone Industries Ltd.
Bangalore 560 016, INDIA

ABSTRACT

A new gate drive circuit, with ferrite core transformer isolation, for power MOSFETs switching at low frequency in the micro Hertz range has been presented. The technique involves periodic refreshing of charge on the effective gate source capacitance of the MOSFET in order to ensure low ON-state resistance, $R_{DS}(ON)$, by maintaining its gate-source voltage above the threshold level. The simulation of the drive circuit using circuit analysis program PSPICE is described with results and relevant waveforms.

INTRODUCTION

The availability of reliable and efficient power semiconductor switching devices has contributed significantly to the development and application of power electronic systems in the fields of generation, transmission and distribution of electric power, telecommunication and variable speed drives. The direction, extent and pace of progress in the development and application of power electronics in these areas has been dependent largely on the improvements in the power handling capability as well as the control schemes of these switching devices. The selection of these devices, such as thyristors (SCRs) bipolar transistors (BJTs), MOSFETs and isolated gate bipolar transistors (IGBTs), is decided by the forward current, blocking voltage, turn-on & turn-off times and tho switching losses that the device is expected to handle in a given application. Thyristors are used for low frequency application due to its considerable turn-on, turn-off times and involved commutation process. For high frequency switching applications BJTs, MOSFETs and IGBTs are preferred on account of their excellent switching characteristics like negligible turn-on and turn-off times and easier control schemes. In general, most of these switching devices are provided with isolated drive using pulse transformers, for isolating the power and control circuits.

Therefore, when the switching frequency is extremely low and devices such as BJTs, MOSFETs and IGBTs are used as controlled switches with isolated drive, the size of the pulse transformer becomes enormously large for preventing core saturation. Further, the BJTs consume considerable drive power compared to MOSFETs under similar operating conditions. To alleviate these problems, a new ferrite cored transformer coupled gate drive circuit has been developed for power MOSFETs switching at low frequency incorporating features like negligible turn-on and turn-off times, low gate power requirement, and miniature ferrite cored pulse transformer. This new gate drive circuit finds applications in switch mode DC-DC converters and DC-AC inverters with high frequency link and PWM control [6-8] wherein some of the MOSFETs have to conduct with duty cycle extended beyond 50%.

PRINCIPLE OF OPERATION

The power MOSFETs are charge controlled devices [1-4] with a nearly pure capacitance as the input impedance between its gate and source. For a N-channel enhancement mode MOSPET to switch with low on-state resistance $R_{DS}(ON)$, its effective gate source capacitance $C_{GS}(eff)$ must be charged with a gate drive such that the voltage V_{GS} across it, is above the threshold level V_{TO} (typically 10 volts). In the absence of such a gate drive, the loss of charge on $C_{GS}(eff)$ due to leakage current leads to the voltage across it to fall exponentially

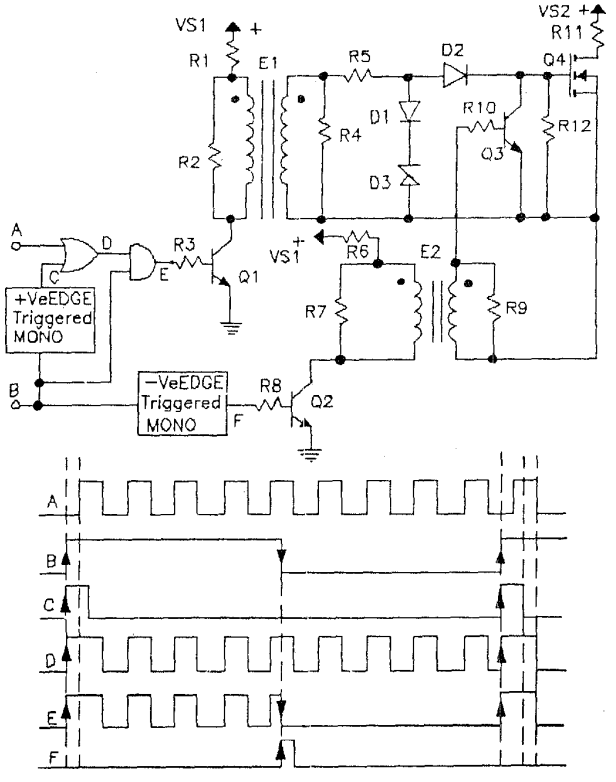

Figure 1: New Gate Drive Circuit for Enhancement Type N-Channel MOSFET with Extended Duty Cycle

below V_{TO} and consequent increase of the on-state resistance $R_{DS}(ON)$. Thus in order to maintain the RDS(ON) low, it is mandatory to refresh the charge on $C_{GS}(eff)$ at a rate greater than the rate at which the charge is lost due to the leakage current. When the MOSFET has to be maintained in the, ON-state with low $R_{DS}(ON)$ for long duration, it would be impossible to maintain the ferrite cored pulse transformer, to remain unsaturated with a constant drive pulse such that V_{GS} is above V_{TO} at any specified drain current, drain source voltage and operating temperature. To circumvent this problem, the charge on the effective gate source capacitance is refreshed at high frequency (above 20 kHz) such that the voltage across $C_{GS}(eff)$ is above the gate threshold voltage V_{TO} for the duration of conduction and the ferrite transformer remains unsaturated.

The concept of periodic refreshing of charge used in DRAMs to retain its memory [2-3], has teen extended in this paper for control. of POWER MOSFETs as an ideal controlled switch at low frequency. The proposed gate drive circuit schematic is shown in Figure 1. The POWER MOSFET Q4 is the switch to be operated at low frequency and the duration of conduction of which is decided by pulse B. The resistor R12 (which represents the resistance of the leakage path) and the effective gate source capacitance $C_{GS}(eff)$ determines the rate of loss of charge on $C_{GS}(eff)$. The charge on $C_{GS}(eff)$ is refreshed at a rate faster than the rate of discharge by pulse A via the transistor Q1, ferrite cored pulse tradsformer E1, R5 and blocking diode D2, such that V_{GS} is above V_{TO} for the duration of conduction. During the period of conduction of MOSFET Q4, Q3 is maintained in the OFF - state. The diode D1 and the zener diode D3 limit the voltage V_{GS} approximately to that of the zener diode voltage rating. The diode D2 prevents the gate-source capacitance from discharging through the transformer E1 in the absence of a charging pulse, while D1 prevents the zener diode D3 from conducting during the off time. For Q4 to turn-on when B goes high, the first rising edge of A must. be synchronised with the rising edge of B. In situations wherein this condition is not met by A, the output of the positive edge triggered monostable multivibrator i.e., pulse C, in combination with A provides the required pulse D which satisfies the above mentioned criterion. The width of pulse C preferably must not exceed 1/4th the period of pulse A and the transformer E1 must be designed to operate without saturation with extended pulse widths as shown by pulse D. In order to minimise the size of the ferrite cored pulse transformer E1, the frequency of A is fixed above 20 kHz. The duration of refreshing of charge on $C_{GS}(eff)$ via Q1 and E1 is controlled by B as shown by pulse E. The MOSFET Q4 is turned off by discharging $C_{GS}(eff)$. This is accomplished by switching on Q3 by the drive pulse F via pulse transformer E2 and Q2. The turn off pulse F is generated at the end of the duration of conduction by the negative edge triggered monostable multivibrator when B goes low.

The voltage source VS1 provides the required energy to charge and discharge the gate source capacitance. The voltage source

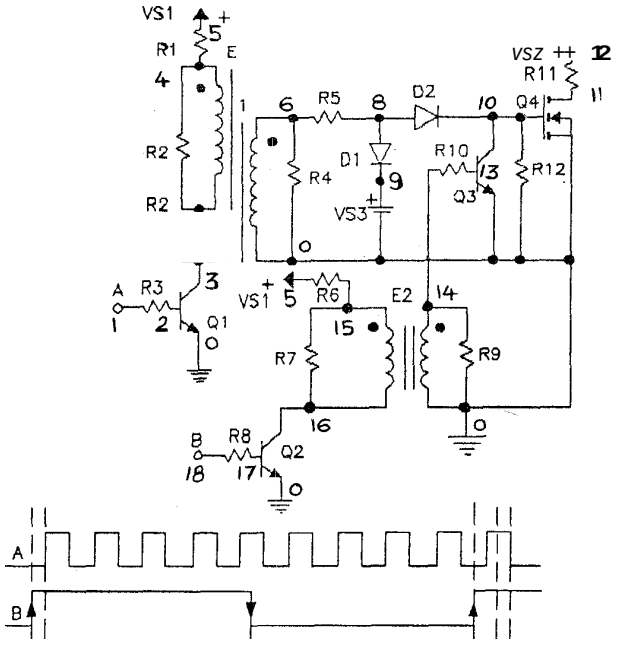

Figure 2: Equivalent Circuit of New Gate Drive for Simulation using PSPICE.

VS2 along with load resistor R11 determines the drain current. The prototype of the new gate drive circuit has been tested with BUZ 24 power MOSFET. It has been observed that a turn on time of 0.6 microsec. and a turn off time of 0.2 microsec can be achieved with negligible gate power consumption.

SIMULATION WITH PSPICE

The new gate drive circuit has been simulated using the circuit analysis program PSPICE on a personal computer. The equivalent circuit for simulation is shown in Figure 2. For the purpose of simplification, the various logic gates shown in Figure 1 have been eliminated. The gate source capacitance is charged by pulse A via Q1, E1, R5 and D2. The frequency of A is fixed at 25 kHz with 50% duty ratio. The transformer E1 is the voltage controlled voltage source with 6 and 0 as controlled nodes, 4 and 3 as controlling nodes and voltage transfer ratio being V_{43}/V_{60} = 1/1.2. The zener diode D3 is replaced by a constant DC voltage source VS3 of 15 volts. The leakage current is determined by resistor R12 at a given V_{GS}. The effective gate source capacitance C_{GSO} for Q4 is represented by a channel width of 2 microns and a gate source overlap capacitance of 750 micro Farads per meter of channel width [5]. The gate source threshold voltage, for Q4 to be in the ON-state, is set by VIO (typically 10.0 volts). The maximum forward current gain Beta is fixed at 100.0 for the BJTs. The pulse transformer E2 is represented by another voltage controlled voltage source with 14 and 0 as the controlled nodes, 15 and 16 as controlling nodes and voltage transfer ratio being $V_{15,16}/V_{14,0}$ = 1/1.2.

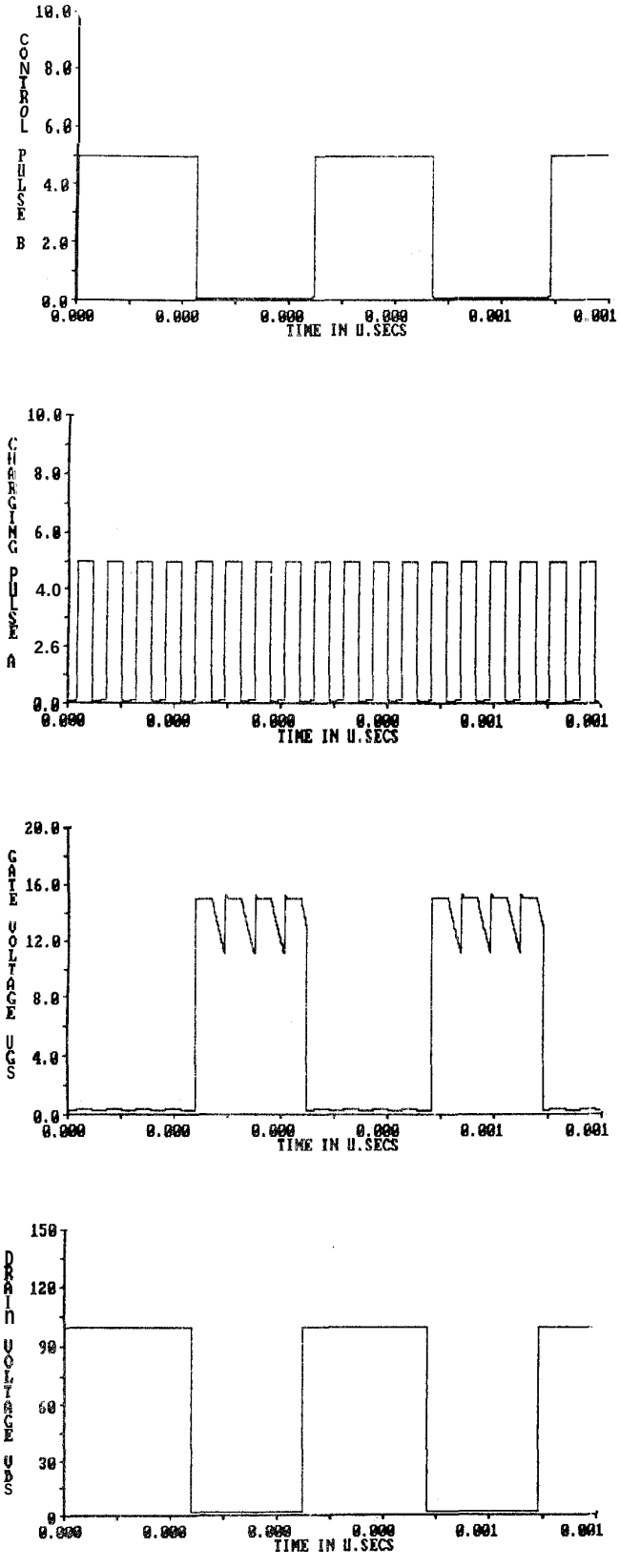

Figure 3: Waveforms from Simulation Results

The gate source capacitance is charged for the duration when B is low and Q3 is in the OFF-state. The charging and discharging of the CGS(eff) with respect to A and B can be seen in Figure 3. At the end of the charging period, when B goes high, Q3 is turned-ON via Q2 and E2 thereby reducing the voltage U_{GS} below the required threshold voltage V_{TO} and consequently turning off Q4. It car: be observed that even at the end of the discharging period, when B is low, the voltage at node 10 across the gate source capacitance is above the threshold level and therefore Q4 continues to be in the ON-state with low $R_{DS}(ON)$.

The detailed listing of the PSPICE program is given in the Appendix I which can be run on a personal computer,. The effect of variation of different parameters such as VTO, CGSO, leakage current path resistance R12 and zener clamping voltage represented by VS3, on the switching characteristics of the MOSFET can be studied using PSPICE program before implementing the circuit. The various waveforms of pulse A, B and voltages at node 10 and 11 are shown in Figure 3. The results obtained from simulation have been found to agree well. with the experimental results.

CONCLUSION

The power MOSFET in combination with this new gate drive circuit provides an ideal alternative to the! BJTs and SCRs as a controlled switch at: low switching Erequency and mode~rate power level. The problems associated with considerable drive power requirement of BJTs and/or involved commutation of SCRs have been alleviated with the technique presented in this paper for the control of power MOSFETs while retaining its excellent switching characteristics and negligible gate power requirements. The PSPICE program listing has been provided to study the salient features of this new gate drive circuit on a personal computer and relevant waveforms of simulation are also presented.

APPENDIX A

```
THIS PROGRAM ANALYSIS NEW GATE DRIVE CIRCUIT FOR POWER MOSFETS

VS1 5 0 DC 15
VS2 12 0 DC 100
VS3 9 0 DC 15
R1 5 4 1K
R2 4 3 8.2K
R3 1 2 10K
R4 6 0 8.2K
R5 6 8 10
R6 5 15 1K
R7 15 16 8.2K
R8 18 17 10K
R9 14 0 8.2K
R10 14 13 1K
R11 12 11 1K
R12 10 0 39K
D1 8 9 DSWIT
D2 8 10 DSWIT
 .MODEL DSWIT D(RS=0.1)
*-----------------------------------------------
*VINA IS THE CHARGING, PULSE A AT NODE 1
*VINB IS THE CONTROL PULSE B AT NODE 18
```

```
*VINX M N PULSE ( INITIAL VALUE,FINAL VALUE,
*                DELAY TIME, RISE TIME,FALL
*                TIME,PULSE WIDTH,PERIOD )
*-----------------------------------------------
VINA 1 0 PULSE(0.0 5.0 10.0US 0.0US 0.0US
+ 20.0US 40.0US)
VINB 18 0 PULSE(0.0 5.0 0.0MS 0.0US 0.0US
+ 160.0US 320.0US)
Q1 3 2 0 BJT
Q2 16 17 0 BJT
Q3 10 13 0 BJT
 .MODEL BJT NPN BF=100.0
E1 6 0 4 3 1.2
E2 14 0 15 16 1.2
MOS 11 10 0 0 NTYPE
 .MODEL NTYPE NMOS VTO=8.0 KP=5.0 LAMBDA=.02
+ RS=.05 W=2U CGSO=750.0UF
 .OP
 .OPTIONS NODE
 .OPTIONS NOMOD NOPAGE
 .OPTIONS RELTOL=1M ABSTOL=1U VNTOL=1U
 .OPTIONS ITL2=20
 .OPTIONS ITL5=0 CHGTOL=1U
 .OPTIONS LIMPTS=50000
 .TRAN 1.0US 720.0US
 .PRINT TRAN V(1) V(18)
 .PLOT TRAN V(1) V(18)
 .END
```

REFERENCES

1. Duncan, A. Grant, John Gowar, 'Power MOSFETs - Theory and Applications', John Wiley & Sons, Inc., (A Wiley Interscience), New York, 1989.

2. Betty Prince, Gunnar Due - Gundersen, 'Semiconductor memories', John Wiley & Sons, Inc., (A Wiley Interscience), New York, 1983.

3. Walter, A. Tricbel, Alfrea E. Chu, 'Handbook of Semiconductor and Bubble Memories', Prentice-Hall Inc., New Jersey, 1982.

4. Roland Sitting, P. Roggmiller, 'Semi-conductor Drives for Power Conditioning', Plenum Press, New York, 1982.

5. H. Nienhans, J. Bowers, 'A high power MOSFET computer model', IEEE Power Electronics Specialists Conf. Record 1980, pp. 97-103.

6. S.R. Narayana Prakash, P.V. Ananda Mohan, B.S.R. Iyengar, 'Low frequency sinewave inverter using ferrites', Paper identification No. 313, Proc. of the 3rd European Conf. on Power Electronics and Applications, Aachen, West Germany, Oct. 9-12, 1989.

7. S.R. Narayana Prakash, P.V. Ananda Mohan, B.S.R. Iyengar, 'A new sinewave inverter with high frequency link and synchronous rectification using power MOSFETs', IEEE Power Electronics Specialists Conf., San Antonio, Texas, U.S.A., June 11-14, 1990.

8. S.R. Narayana Prakash, P.V. Ananda Mohan, B.S.R. Iyengar, 'A novel high frequency PWM inverter generates sinusoidal output voltage at 50 Hz', Presented at the IEEE International Telecommunication Energy Conf., Orlando, Florida, U.S.A., Oct. 21-2[illegible] 1990.