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LETTER

Common mode disturbance tolerant broadband differential SPDT switch for Ka-band radar

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Abstract The proposed broadband fully differential single-pole double-throw (SPDT) switch for Ka-band radar with high 1-dB power compression point (P_{-1dB}) and isolation is demonstrated using 0.13 μm SiGe BiCMOS technology. In contrast to traditional circuit, SPDT switch utilizes fully differential topology with virtual grounding, so it also offers cancellation to common mode disturbance. As a result, this SPDT switch will help in improving radar range due to its high P_{-1dB}, high range-resolution and accuracy due to its broad-bandwidth. Further, this paper also introduces the use of asymmetrical tapered inductor in SPDT switch to improve layout area of SPDT switch with normal spiral inductor. Measurement results of fabricated differential SPDT switch with conventional layout has demonstrated a minimum insertion loss of 2.9 dB and an isolation of −39 dB in 25 GHz to 40 GHz frequency-band, and input P_{-1dB} of 12.6 dBm at 34 GHz with 0.47 mm^2 area. EM simulation results of compact differential SPDT switch with symmetrically tapered inductor in layout has demonstrated minimum insertion loss of 1.8 dB and isolation of -39 dB in same frequency-band, input P_{-1dB} of 14.1 dBm at 34 GHz with 0.11 mm^2 area.
Keywords: BiCMOS, CMOS, differential SPDT, FMICW, radar
Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

The technology advancement in the field of CMOS and BiCMOS based processes has lead to realization of integrated system with analog, RF and digital functionalities on a single-chip using system-on-chip (SoC) approach [1]. This approach is widely used in communication system, particularly for realization of frequency modulated interrupted continuous wave (FMICW) short range radar [2], and telecommunication industry, in realization of transmit/receive (T/R) module [3, 4, 5, 6] for mm-wave phased array based 5G communication system.

The SPDT switch is one of the main RF circuit blocks in FMICW and T/R modules. These applications are based on half-duplex communication and require a switch to reconfigure system in transmit or receive mode as per the predetermined programming. Since in most of the applications, SPDT switch is positioned just after the antenna or LNA/PA, it is necessary that it should introduce minimum insertion-loss, provide good isolation between transmit and receive ports, and have high power handling capability [7, 8]. Apart from these system-level specifications, at circuit design-level it should provide proper ground, capability to reject common mode disturbance and possess identical layout for transmit and receive configuration. In RF circuits, bias voltage and ground play an important role in deciding noise figure (especially in the case of LNA [9]), power output (especially in the case of PA [10]), gain/insertion-loss and P_{-1dB} of other circuit blocks in general. If common mode disturbance exists, it will disturb the common mode biasing voltage of MOS transistor and grounding in the circuit, hence power output, P_{-1dB} and gain/insertion loss characteristics of current and subsequent circuit block will be disturbed.

Traditionally, these RF SPDT switches are being realized using III-V semiconductor technologies [11, 12, 13, 14], since they offer high isolation and high P_{-1dB}, and introduce low insertion loss. But fabrication of multi-functional chips (MFCs) or core-chips using these processes is expensive and poses challenges in integration. To minimize the chip area, a shunt nMOS SPDT switch is adopted in [3], however, it has poor power handling capability. In silicon circuits, to overcome the disadvantage of low-power handling capability, saturated or reverse saturated HBTs [15, 16, 17] are used for designing millimetre wave SPDT switches and $\lambda/4$ transmission line. But, realization of accurate $\lambda/4$ transmission line is challenging, occupying more area at Ka-band, and these SPDT switches [15, 16, 18, 19] have poor isolation due to single-ended architecture an hence susceptible to common mode disturbances. Also, these switches need perfect or near to perfect ground for better decoupling. In [20], switchable balun and stacked nMOS transistors [21] are used for improving the area and P_{-1dB} of the SPDT switch. But these circuits [20, 21] suffer from poor common mode rejection due to single ended architecture, poor-isolation, higher insertion-loss and require additional bias voltage for source and drain biasing. In [22], transformer type differential inductor is used for differential SPDT switch design. However, due to the use of transformer type inductor, coupling is limited and hence has poor isolation, limited 3 GHz bandwidth and high insertion loss at Ku-band. In [23], high substrate resistance is used to improve the insertion-loss and power handling performance over a limited bandwidth of 5 GHz, i.e., for 35 GHz to 40 GHz operating frequency. However, in later part of this paper, authors have pointed out that, due to series switch architecture, insertion-loss and isolation performance of this SPDT switch are dependent on input-power, hence suitable for only transmitter path. Isolation of this switch is minimum 25 dB for input power of 16 dBm.

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In this paper, we have proposed an analysis of SPDT switch design consideration for short range radar, and proposed a fully differential Ka-band shunt nNMOS SPDT switch with virtual grounding using 0.13 μm BiCMOS technology. The SPDT switch topology is introduced for cancellation of common-mode disturbance and improving power handling capability. Virtual grounding concept is used throughout SPDT switch for providing immunity to poor grounding. To miniaturize the size of the differential SPDT switch in the first design (called 'design 1'), we have introduced the use of asymmetrically tapered inductor in the second design of SPDT switch (called 'design 2'). In comparison to conventional circuit architecture, this proposed SPDT switch circuit architecture (design 2) has compact layout and common mode disturbance tolerance capability. Both the designs have demonstrated broadband performance of 15 GHz with high power handling capability (P_{-1dB} > 14.1 dBm at 34 GHz for SPDT switch design 2) as well as good isolation (max. 39 dB), simultaneously at Ka-band.

2. SPDT switch design considerations

A block diagram of RF front-end for T/R module and short-range FMICW radar is shown in Fig. 1, presenting the critical positioning of SPDT switch.

For a short range Radar system with transmitted power of (P_t) ~ 10 dBm, the impact of critical SPDT switch specifications on overall system performance are: Insertion loss ∝ noise figure (NF), P_{-1dB} ∝ linear output power, switching speed ∝ minimum detectable range (R_{min}), and isolation ∝ coupling of transmitted signal in the receiver path and bandwidth.

In the case of RF frontend for T/R module, as shown in Fig. 1 (a), SPDT switch is positioned prior to power amplifier in transmission-path and hence power levels are relatively lower than FMICW radar (Fig. 1 (b)), where SPDT switch is positioned after power amplifier. From radar range equation [24], maximum range (R_{max}) for a radar operating at frequency (f) with minimum received power (P_{rmin}), transmitted power (P_t), transmitted antenna gain (G_t), received antenna gain (G_r), speed of signal (c = 3×10^8 m/sec) and radar cross-section (σ) is given by:

$$R_{max} \simeq \left[\frac{P_t G_t G_r c^2 \sigma}{4\pi^3 f^2 P_{rmin}}\right]^{1/4} \quad (1)$$

For FMICW type system, R_{min}, range resolution (ΔR) and range accuracy (σ_R) are given by [24]:

$$R_{min} = \frac{c\tau_{total}}{2} \quad \tau_{total} = \tau_{ON} + \tau_{SW} \quad (2)$$

$$\Delta R = \frac{c}{2B_{RF}} \quad \sigma_R = \frac{c}{3.6B_{RF}\sqrt{2SNR}} \quad (3)$$

where, τ_{total} is total transmitter ON time, τ_{ON} is the time for which Radar is transmitting, τ_{SW} is switching time of SPDT switch, B_{RF} is RF bandwidth and SNR is received signal-to-noise ratio. In such a system, as per equation (3), for higher range resolution and accuracy, it is preferred to choose higher frequency of operation to take advantage of available higher bandwidth. However, as per equation (1), as frequency increases, maximum range decreases due to increase in path-loss and insertion-loss at higher frequencies. So, to achieve same range at frequency ($f_2 > f_1$), we need to transmit higher power by $20\log(f_2/f_1)$. Hence, we need SPDT switch of higher P_{-1dB}. It is also important to note that designing a CMOS/BiCMOS SPDT switch with low insertion-loss and higher P_{-1dB} is increasingly difficult at high frequencies, more so, especially at mm-wave frequencies due to dominating EM effects and parasitics. So, considering a trade-off between insertion-loss, isolation, P_{-1dB}, technology limitation, and range requirement of the SPDT switch, we have selected Ka-band as frequency of operation, and 15 GHz as RF bandwidth for high range resolution and accuracy.

3. SPDT switch circuit design

Fig. 2 (a) and (b) present single-ended matching and switching networks and corresponding fully differential circuits realized by virtual grounding of the common node. Fig. 3 (a) shows the circuit diagram of the proposed resultant fully differential SPDT switch. This circuit is based on fully differential architecture for high common-mode rejection. We have designed the matching network using $\lambda/4$ impedance transformer, realized with the combination of series inductor, shunt capacitor and transistor's parasitic capacitance. As per equation (1), for a Ka-band FMICW Radar, output P_{-1dB} ≃ 10 dBm is sufficient for the ground target at ≃ 100 m distance with appropriate G_t, G_r and σ values. We have used nMOS shunt switches to meet the requirement of minimum

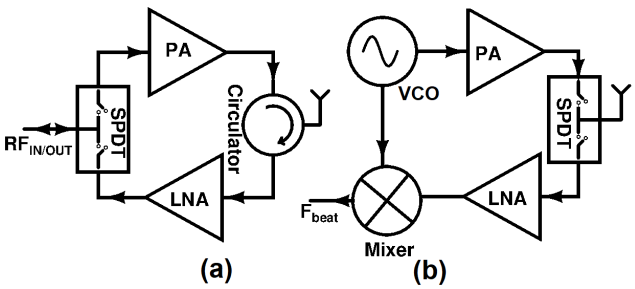

Fig. 1 Block diagram of RF front end for (a) T/R module and (b) FMICW radar

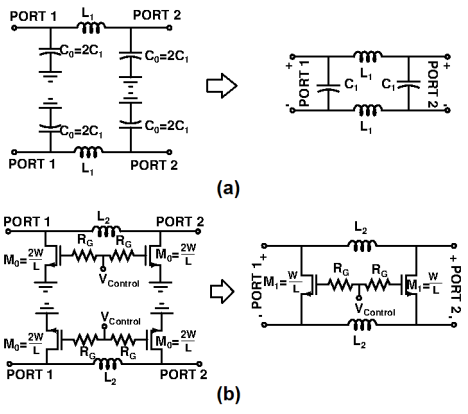

Fig. 2 Circuit diagrams of the (a) single ended grounded and corresponding ungrounded differential matching network, and (b) single ended grounded and corresponding ungrounded differential switching network

insertion loss (< 4 dB), output $P_{-1dB} \simeq 10$ dBm, isolation > 30dB, and $tau_{total} \simeq 5.3$ nsec across 25 GHz to 40 GHz frequency band. Differential signalling is used throughout the SPDT switch circuit to provide immunity to poor physical ground supplied externally. Further, a high resistance ($R_G = 20\ K\Omega$) is added in series with gate to avoid coupling of signal with control signal, and minimize the variation in transistor parasitics. And, a high resistance ($R_S = 20\ K\Omega$) is also added in series with substrate to avoid coupling of signal with substrate [25, 26]. This CMOS switch supports maximum gate/control voltage of 1.5 V and has typical threshold voltage of 0.37 V. Use of higher R_G has improved the switch linearity, but it leads to increase in switching time of nMOS switch, due to corresponding increase in RC time constant of R_G and MOS gate capacitance ($\simeq$ 95 fF). However, for this application switching time requirement is less than or equal to 1 ns, and is met with $R_G = 20\ K\Omega$.

3.1 Differential signalling

At high frequencies, RF signals are guarded with ground to minimize the interference/coupling among the different RF signals within a chip, since ground provides the low impedance path to RF signal. But at high frequencies, due to the effects of dominating electromagnetic (EM) and distributed parasitics, providing a perfect ground is almost impossible, hence this leads to degradation in circuit performance. In practice, in an integrated T/R module or FMICW radar, multiple ground pads are kept within a chip to provide better ground, but this leads to increase in number of pins, package size and complexity. In this present work, fully differential topology is realized by means of coupling of single ended network and un-grounding the common net as shown in Fig. 2 (a,b).

Single ended Π-matching or shunt switching network is susceptible to ground disturbance or poor grounding, hence is very likely to have poor common mode rejection. Theoretically, fully differential passive network with no grounded nets will have infinite common mode rejection. Practically, we get some degradation in common mode rejection due to distributed and parasitics effects at high frequencies [27, 28].

3.2 SPDT switch operating principle

The diffenital shunt SPDT switch has been designed using a combination of differenital $\lambda/4$ line, formed by differential L_1-C_1-$L_1 - C_1$ Π-network and differential shunt switch, formed by differential MOS-inductor Π-network (M_1-L_2-M_1-L_2). In this configuration, when switch is ON, differenital $\lambda/4$ transformer transforms high impedance of the ON-state to low impedance at the common node and vice-versa.

3.3 SPDT switch layout

The layout design plays a critical role in determining the performance of circuit at mm-wave frequencies as distributed circuit effects become more prominent. Hence, it is essential that parasitics and non-idealities of circuit layout are to be estimated accurately, and included at the design stage. To minimize the degradation in quality factor, and to model all the parasitics effects, we have used ADS simulator for EM simulations. To minimize the losses we have used thick top metals, with minimum resistivity for all the routing and synthesizing the inductors. To minimize the losses further, metal width for routing have been maintained constant and bends have been minimized.

3.3.1 SPDT switch design 1

In this SPDT switch, considering layout fitness and better utilization of area, L_1 and L_2 have been synthesized as square inductors. Same layouts of the L_1 and L_2 have been used for doing identical layout design of both the branches in SPDT switch. Integrated layout has been designed by taking positioning of pads, isolation and integration with LNA and PA into account.

3.3.2 Differential SPDT switch design 2

To overcome the increase in layout area of SPDT switch design 1 (due to increase in number of inductors), we have proposed the use of integrated layout for L_1 and L_2 as shown in Fig. 3 (a) and by tapping the inductor asymmetrically. In this design, we have chosen a hexagonal inductor, since for a required inductance value it offers better quality factor compared to a square inductor, and with very less impact on area (< 10%), as shown in Fig. 3 (b, c).

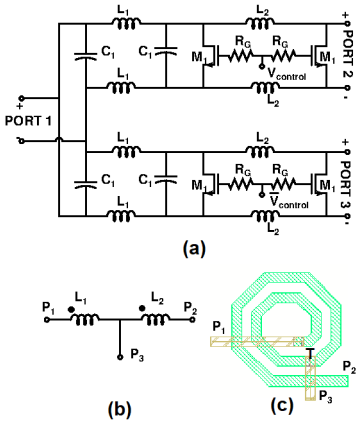

Fig. 3 Circuit diagrams of (a) the proposed SPDT switch, (b) the T-section of SPDT switch design with L_1 and L_2 inductors, and (c) integrated layout of T-section using asymmetrically tapered inductor

Due to layout of two separate inductors as a single spiral inductor, the values of L_1 and L_2 inductors will get changed to $L_1^{'}$ and $L_2^{'}$, respectively, and are given by [29]:

$$L_1^{'} = L_1 + M_{21} \qquad L_2^{'} = L_2 + M_{21} \qquad M_{21} = k_{21}\sqrt{L_1^{'}L_2^{'}} \tag{4}$$

In the above equations, M_{21} is mutual inductance and k_{21} is coupling coefficient between $L_1^{'}$ and $L_2^{'}$. This change in inductance values of L_1 and L_2 inductors can be countered by resizing the respective layouts followed by EM simulation. We have also minimized the coupling between inductors L_1 and L_2 by choosing suitable length of TP_3 layout, thereby introducing a positive inductance at common node T [29]. Same layout has been used for all the T-sections of SPDT switch, and a symmetrical layout has been carried out for better matching. This SPDT switch design 2 has all the advantages of differential architecture and with a chip area similar to single-ended design.

Table I Performance summary and comparison

Ref.	[4]	[8]	[30]	[31] Rx/Tx	This work Design 1	This work Design 2
Technology (nm)	BiCMOS 130	GaAs 150	CMOS 65	CMOS 65	BiCMOS 130	BiCMOS 130
Frequency (GHz)	30-45	22-26	25-39.5	25-30	**25-40**	**25-40**
Insertion loss (dB)	2.7-3.7	2.5	0.89-1.5	0.74-1.16/ 0.96-1.1	2.9-4.2	**1.8-3.1**
Isolation (dB)	33-51	44	11-18.2	16-29/ 27-28	**31-39.2**	**33-39**
P_{-1dB} (dBm)	8 @ 35 GHz	36 @ 24.5 GHz	12.55 @ 28 GHz	5.2/31.8 @ 28 GHz	**12.6** @ 34 GHz	**14.1** @ 34 GHz
S_{11}/S_{22} (dB)	< -13	$< -7/< -9$	< -20	$< -15.9/< -14.2$	< -11	< -10.5
Area (mm^2)	0.029	3.1	0.009	0.043	0.47	0.11

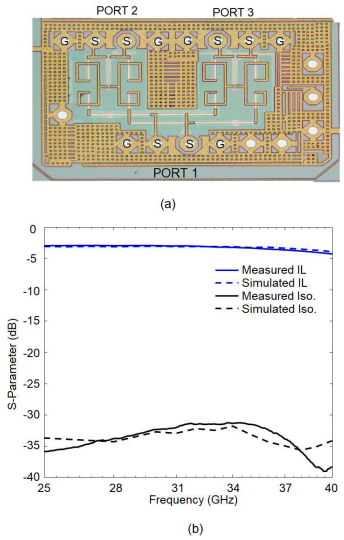

Fig. 4 (a) Die photo of fabricated differential SPDT switch design 1 with area of 0.48 mm × 0.98 mm without pads and (b) measured and simulated, insertion loss and isolation plots of the fabricated *SPDT switch design 1* die.

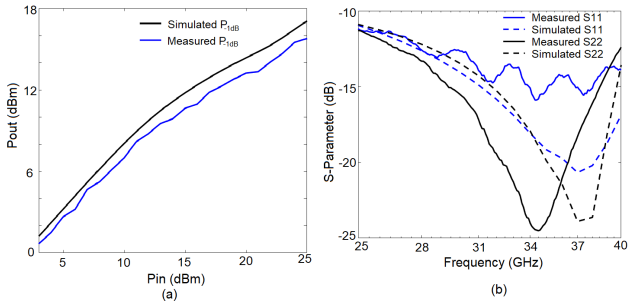

Fig. 5 Measured and simulated (a) P_{-1dB} and (b) input and output matching S-parameter plots of the fabricated *SPDT design 1* die by using gate control voltage = 0 V

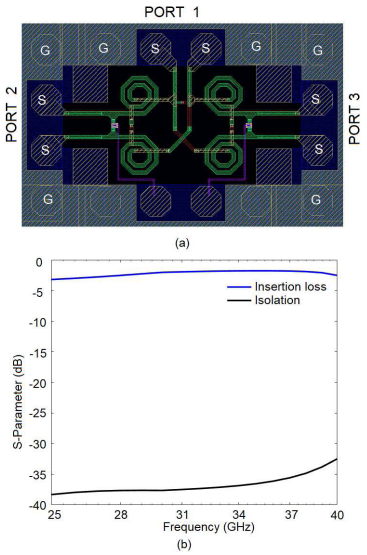

Fig. 6 (a) Layout photo of differential *SPDT switch design 2* with area of 0.38 mm x 0.31 mm without pads and (b) 3D EM simulation plots of insertion loss and isolation for the compact *SPDT switch design 2*

4. Simulation and measurement results

Design and layout of differential SPDT switches 1 and 2 have been done using 0.13 μm BiCMOS technology. In this paper, we present EM simulation and measurement of differential SPDT switch 1, and EM simulation of differential SPDT switch 2. EM simulations of the circuit layout were carried out using ADS 3D simulator and wafer measurements were carried out using Agilent PNA-X and 100 Ω differential ground-signal-signal-ground (GSSG) probes. The measurement and simulation results are carried using port 1 as input port and port 2 or port 3 as output port.

Fabricated SPDT switch 1 occupies a chip area of 0.98 mm x 0.48 mm, i.e., 0.47 mm^2 without pads, as shown in Fig. 4 (a). Fig. 4 (b) shows the measured and simulated insertion loss and isolation plots with matching trends. The measured insertion loss of this design varies between 2.9 dB and 4.2 dB, and isolation varies between −31.2 dB and −39 dB across the frequency band of operation, i.e., 25 GHz to 40 GHz, and demonstrated a measured input P_{-1dB} of this design as 12.6 dBm at 34 GHz (Fig. 5 (a)). Fig. 5 (b) shows the measured and simulated input (S_{11}) and output (S_{22}) return loss values of SPDT switch design 1, both showing similar trends. The measured values of S_{11} and S_{22} are lower than −11 dB, and switching speed is in between 260 ps and 300 ps across the frequency band of operation. The variation in the values of simulated and measured S_{11}, S_{22}, insertion loss and P_{-1dB} is due to the dominant EM effects, variation in device parameters post-fabrication and use of limited layout EM meshing during 3-D EM simulation.

The layout chip area of the compact differential SPDT switch 2 with tapered inductor is 0.38 mm × 0.31 mm, i.e., 0.11 mm^2 without pads, as shown in Fig. 6 (a). 3D EM simulation of the compact differential SPDT switch design 2

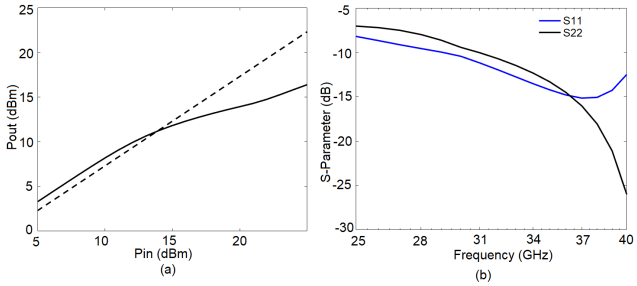

Fig. 7 3D EM simulation plots of (a) P_{-1dB} and (b) input and output matching S-parameters for the compact *SPDT switch design 2 by using gate control voltage = 0 V*

was carried out by following the simulation settings similar to SPDT switch design 1. This design has demonstrated insertion loss between 1.8 dB and 3.1 dB, and isolation between −33 dB and −39 dB in the frequency band of operation, i.e., 25 GHz to 40 GHz, and has demonstrated a P_{-1dB} of 14.1 dBm at 34 GHz, as shown in Fig. 6 (b) and Fig. 7 (a), respectively. This design has also demonstrated S_{11} and S_{22} values lower than −10.5 dB, as shown in Fig. 7 (b), and switching speed is in between 250 ps and 300 ps, across the frequency band of operation. In this design, S_{11} as well as S_{22} values for OFF/ON state of switching network, i.e., shunt MOS - series L - shunt MOS is (8.1+j0.066) Ω/(99.4-j0.58) Ω and (120.74+j18.6) Ω for $\lambda/4$ differential Π LC matching network at 35 GHz, by taking characteristic differential impedance Z_0 of 100 Ω. At the integrated level, OFF-state SPST path offers high impedance from 216-268 Ω at the common node across the frequency band of operation and hence achieves high isolation from −33 dB to −39 dB.

As per our literature survey, compared to the proposed SPDT switch architecture, all the available SPDT switch architectures with operating frequency above 25 GHz are single-ended, and hence are susceptible to common mode disturbance. Apart from immunity to common mode disturbance, as a result of its differential architecture, this work of SPDT switch designs 1 and 2 offers better isolation [30, 31], higher P_{-1dB} [4, 30, 31] and 15 GHz bandwidth of operation, i.e., high range resolution and accuracy with similar insertion loss (Table I).

5. Conclusion

In this paper, we presented the impact analysis of SPDT switch design considerations for the performance of FMICW or T/R module radar. To provide immunity to the common-mode disturbances, we proposed a new differential SPDT switch design 1 with virtual grounding. Further the area of SPDT switch design 1 was reduced by use of asymmetrically tapered inductor in layout of SPDT switch design 2. The measured results of fabricated SPDT switch design 1 has demonstrated an insertion loss of 2.9-4.2 dB, isolation of 31-39.2 dB, switching speed is between 260 ps and 300 ps in the operating frequency of 30-45 GHz and input P_{-1dB} of 12.6 dBm at 34 GHz, with an area of 0.47 mm^2. A 3D EM simulation of compact differential SPDT switch design 2 has demonstrated an insertion loss of 1.8-3.1 dB, isolation of 33-39 dB in the operating frequency of 30-45 GHz, switching speed in between 250 ps and 300 ps and input P_{-1dB} of 14.1 dBm at 34 GHz, with an area of 0.11 mm^2. In comparison to other available SPDT switches, due to its differential architecture, these SPDT switch designs 1 and 2 have demonstrated high P_{-1dB} (>12.6 dBm) along with good isolation (>31 dB) with a wide frequency band (15 GHz) of operation, i.e., all three performance parameters are superior at the same time with reasonably low value of insertion loss and area.

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