SLOT-SWITCHED SELF-ROUTING IN A NON-CROSSBAR OPTICAL SWITCHING ARCHITECTURE

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Abstract

A novel duration switching method for self-routing in multi-stage non-crossbar optical switching architectures using a two-Wavelength header scheme is proposed. Closed form expressions are derived for the worst-case signal-to-crosstalk ratio and the insertion loss and the maximum size of the architecture is estimated from these.

1 Introduction

With the increasing use of the optical fiber as a primary transmission medium, there is a strong motivation to achieve the switching of photonic data streams in the optical domain to avoid the electronic-photonic-electronic conversion overheads. Further, the demand for system bandwidth encourages the choice of photonic switching architectures (PSAs) since the bit rates are high enough to place severe demands on the electronic subsystems.

Self-routing of photonic data streams obviates the necessity for high-speed electronics. It has been achieved, partially, by replacing the electronic functions in a conventional self-routing electronic switch with their functional photonic equivalents, as suggested by Haque [1] or optically self-routed bit-switching [2]. We suggest a novel method by which the data and the destination tag – the header – are sent simultaneously over one fiber.

2 The data format

We propose the following data format as shown in Fig.1. In a m-stage architecture, m sub-headers ($S_i, i = 0, \ldots, m$) would be required for each data slot — one for earh of the m stages the signal path encounters. Moreover, each S_i, $i = 0, \ldots, m$, consists of an unique code which may be chosen such that the inter-code interference is minimized [3]. The S_i are put on a carrier wavelength of λ_1 while the data is put on the wavelength λ_2. The separation of the data and the header is achieved through dichroic filters before the first stage. Since the optical switches are usually wavelength-dependent] this is essential. This ensures that:

1. only the data enters the switching fabric while the header information is routed through to the arbitration and decision logic overlaying each stage

2. header and data are sent simultaneously

The data is delayed by sending it through a passive optical fiber delay line [4] so that the sub-header S_i arrives τ seconds before the data slot arrives at the input of the switch in stage 1 where τ is the processing time required for the sub-header recognition and the Arbitration Control Unit (ACU). The ACU logic could be an incoherent power summation substituting for the correlation function. Though generalization to any interconnection network is possible, we adopt the planar network as suggested by Taylor [5] (Fig.2) with the optical switching function realised by any 2 x 2 photonic switch—for instance, the electro-optic directional coupler.

Assuming that the stages are numbered as $0, \ldots, (m-1)$ the data slot must pass through $(k-1)$ delays of d *seconds* each between the stages in 1 and k — artificial delays must be introduced between stages, therefore] that do not have a switch between them to guarantee correct timing. However, by staggering the relative timing of the data slot relative to the header, it would be possible to avoid the delay elements at the cost of a reduced data rate.

While the above scheme ensures that a data slot of duration d will be correctly switched, it does not take care of output contention (either switch or output contention). In the case when two inputs require a common output, or two signals try to force a single switch into two contradicting states, we suggest the following policies:

1. ***Arrival*** *time fixed priority* : Data slots are switched on a first-come-first-served basis. Header priority is fixed by the arrival time of the S_0 and annulled by the arrival of the S_{m-1} (which signifies that the data is already past the stage 0)

2. *Input fixed priority* : Each input has a particular predetermined priority *viz.* input **j** has a higher priority than input *i* if **j** > i. The header request of a data slot arriving on an input with a higher priority is given precedence over the header request of one arriving on an input of a lower priority – this could be advantageous when override signals are to be sent.

3. *Self-fixed priority :* Each header, in this scheme, carries its own priority code. The arbitration logic would then allow the header with the higher priority to achieve the connection while delaying the lower priority code.

When a contention is detected, the input which is blocked is prevented from sending its signal by diverting the signal through the switch into a re-circulant delay line (RDL) so that it is presented at the same input after a fixed-delay interval equal to one frame. The length of the RDL is determined by the nature and rate of the data traffic.

From the worst-case signal path length, the expression may easily be derived to be,

$$SXR[dB] = 10\log\left[\frac{(1-10^{0.1x})^N}{1-(1-10^{0.1x})^N}\right]$$

On the worst case signal path, the insertion loss is given by

$$Insertion\ loss = (2N+3)f_c + N(P+X) + D + 3$$

where N is the number of inputs, f_c is the fiber-fiber coupling loss, P is the propagation loss through one switch, X is the leakage loss per switch and D is the transmission loss per dichroic element.

While typical values of the above parameters (Fig.3) would allow a 64 x 64 switch to be built, we estimate that the size of such a switch would be restricted by the SXR ratio to about 50 x 50 (Fig.4). The pulse width duration is extremely critical to the entire scheme. Also the pulses in the data may have different polarizations which could cause non-uniform modulation of the data pulses. To avoid this, data could be generated from a source with a single polarisation or a polarization- independent switch could be used.

References

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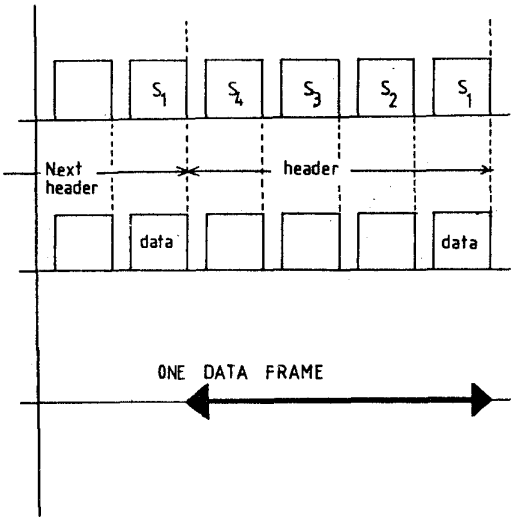

Fig.1 **Data slot format : Two-header scheme**

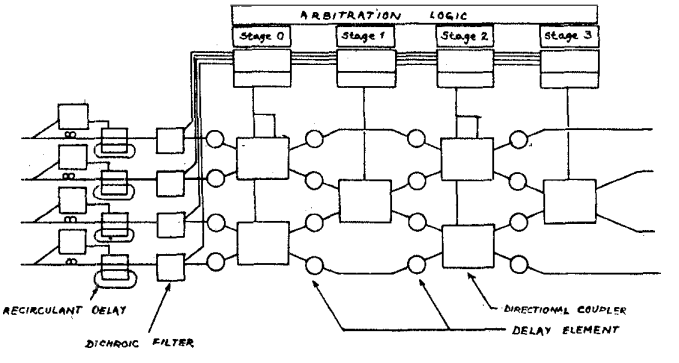

Fig.2 Schematic for slot switched self routing in a multistage non-crossbar architecture

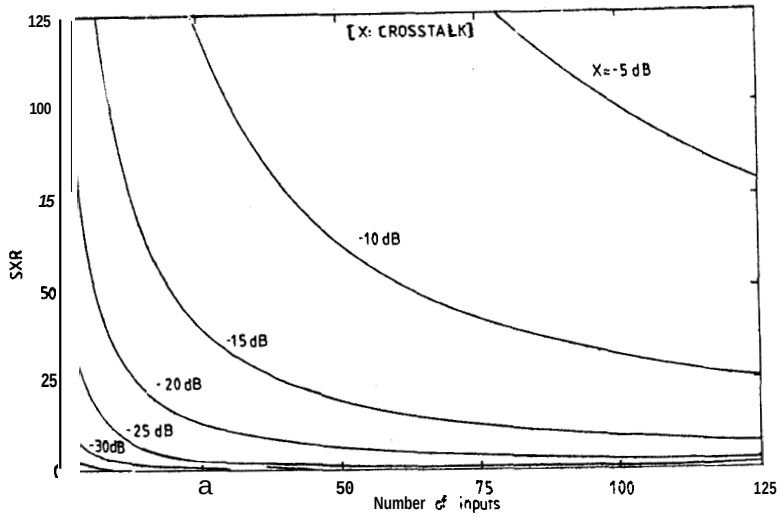

Fig.3 SXR *vs* **Number of inputs for the two-header scheme**

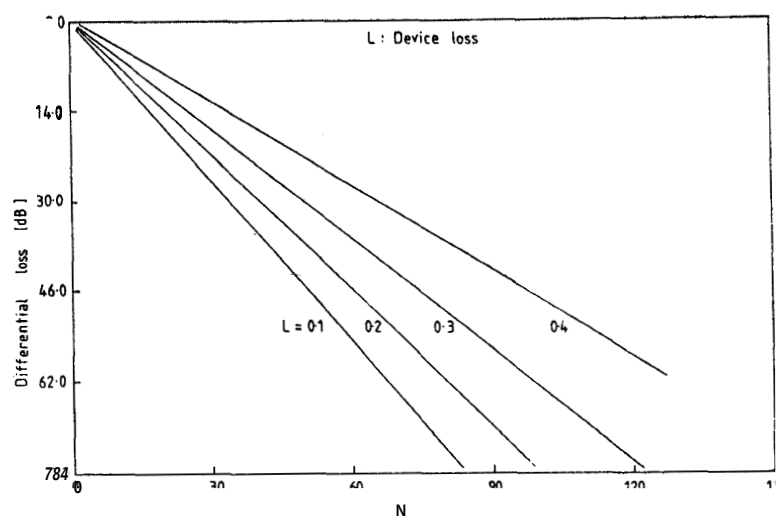

Fig.4 Differential insertion loss *vs* Number of switches in the two-header scheme