**Supplementary information**

**Molecular Switching Operation in Gate Constricted 2D-Heterostructure**

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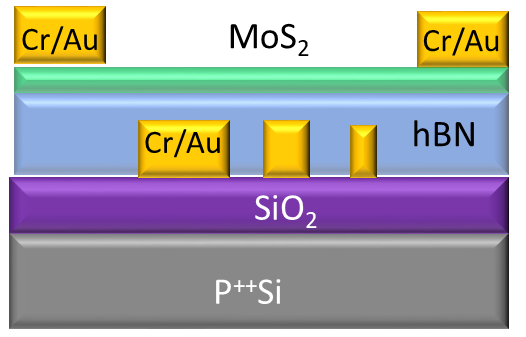
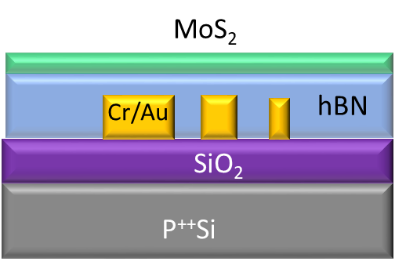
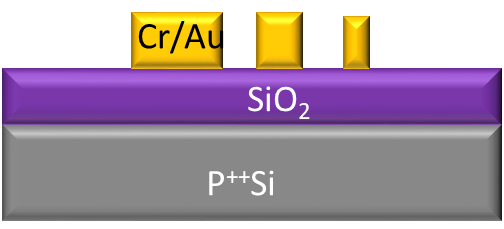
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**Ⅰ. Heterostructure Fabrication Process**

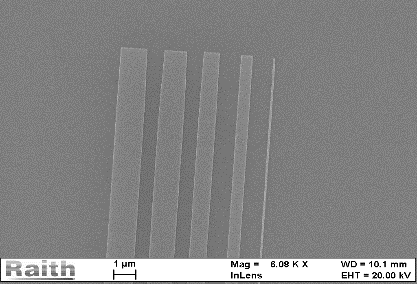
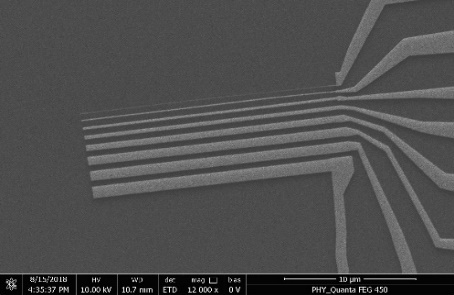
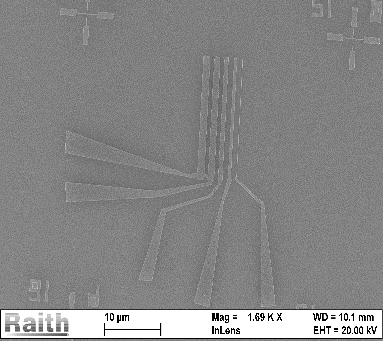
**Figure S1.** (a) SEM image of local gates after deposition of metals (b) Optical image and schematic of the device after transferring of h-BN and MoS2 flake on the patterned electrode. (c) Schematic and optical image of the device after contact electrode fabrication.



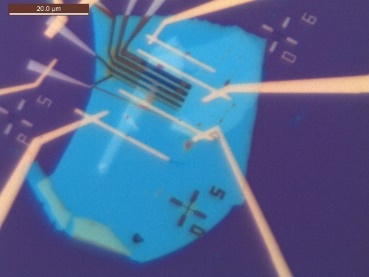
(b)



(a)



(c)



20 µ

The MoS2 and h-BN bulk crystals were bought from Manchester nanomaterials. The gates and electrodes of our devices are fabricated prior to the exfoliation h-BN flakes. The detailed fabrication process is described below and illustrated in Figure S1.

1. **Fabrication of local gate electrodes (Figure S1(a))**

High-resolution parallel metal lines are used as the local bottom gate to control the carrier flow dynamics in the channel to measure the switching effect with molecular interaction. To achieve feature sizes near 50 nm, a more precise version of the above-discussed steps is used. Instead of bilayer PMMA resist coating, only 495 K PMMA is spin-coated on the wafer leads towards the small feature size. The developing parameters of the exposed resist must be optimized accurately to get successful developing or metallization. An overdeveloped resist can increase the feature size significantly and can potentially merge with the adjacent line. Whereas an underdeveloped resist can lead to breaks or discontinuity in the metal line. To achieve correct parameters of developing, a dose test is done using a matrix of the feature (consisting of several parallel lines) with a dose vector of 50 μC/cm2 along both the row, 'Cold development' technique is used to achieve better contrast and to have more control over the developing time, that is to develop the resist in much lower solvent temperature than the ambient, is performed. The kinetic energy of the solvent molecules at a lower temperature is not sufficient to remove fragments of the exposed long-chain polymer. Still, it can remove the very short chain fragments. For the dose test, both the developing solution and IPA stopper solution are kept at −20ºC for 10 minutes prior to developing. The wafers kept for 35 sec in MIBK:IPA solution and IPA stopper solution. After developing in cold solutions, 20 nm gold metallization is done to check for the optimum e-beam dose for that feature using scanning electron micrograph (SEM) imaging. The process details are mentioned stepwise below.

1. Dice Si++/SiO2 wafer into appropriately sized pieces, followed by spin-coating and baking a bilayer PMMA-based resist:
2. 495A5, spun at 3000 rpm for 40 seconds, baked at 180C for 2 minutes
3. 950A5, spun at 3000 rpm for 40 seconds, baked at 180C for 3 minutes
4. Electron beam lithography in Raith e-line system (acceleration voltage 30 kV) to define gate electrodes with widths ranging from 50nm to 1000nm.
5. Develop resist in a DI water:IPA (1:3 by weight) mixture.
6. Deposit Cr(5nm)/Au(20nm) in a e-beam evaporator.
7. Liftoff process in acetone, followed by sonication in Remover PG, and final rinse in acetone and IPA.
8. Annealing at 100C for 1+ hours in N2 environment.

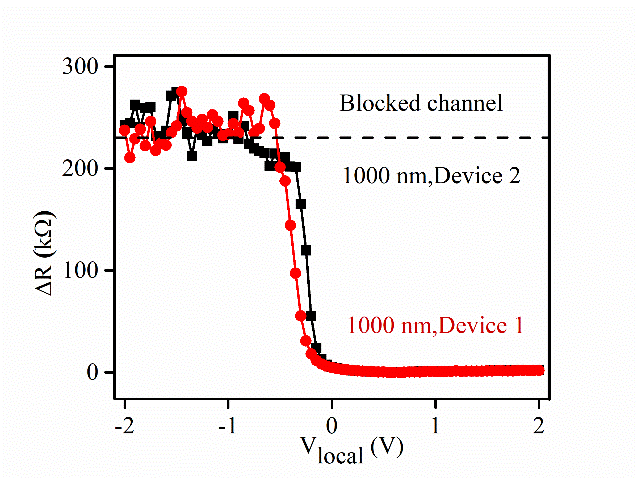
**2. Transfer of bottom h-BN and MoS2 heterostructure stack (Figure S1(b))**

1. Exfoliate h-BN onto cleaned Si/SiO2 wafer.
2. Pick up and transfer the flake onto the gates via standard dry transfer techniques using a PDMS (Gel pack 4) stamp.
3. MoS2 flakes are exfoliated and identified in a PDMS stamp in an optical microscope with 100X objective.
4. The flake was carefully transferred on top of h-BN flake ensuring that the flake is well inside the bottom local gate electrodes.

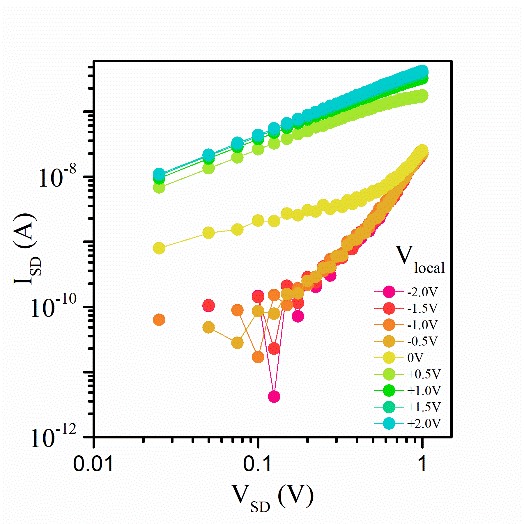
**3. Fabrication of contact electrodes (Fig. S1(c))**

1. Spin and bake of a PMMA-based bilayer resist recipe.
2. 2nd layer electron beam lithography to define contacts.
3. Develop resist in a DI water:IPA (1:3 by weight) mixture.
4. Deposition of Cr (10 nm)/Au (70nm) in a e-beam evaporator.
5. Liftoff with successive baths of acetone and IPA.
6. Annealing at 100C for 1+ hours in N2 environment.
7. Mount chip into chip carrier and wire bond

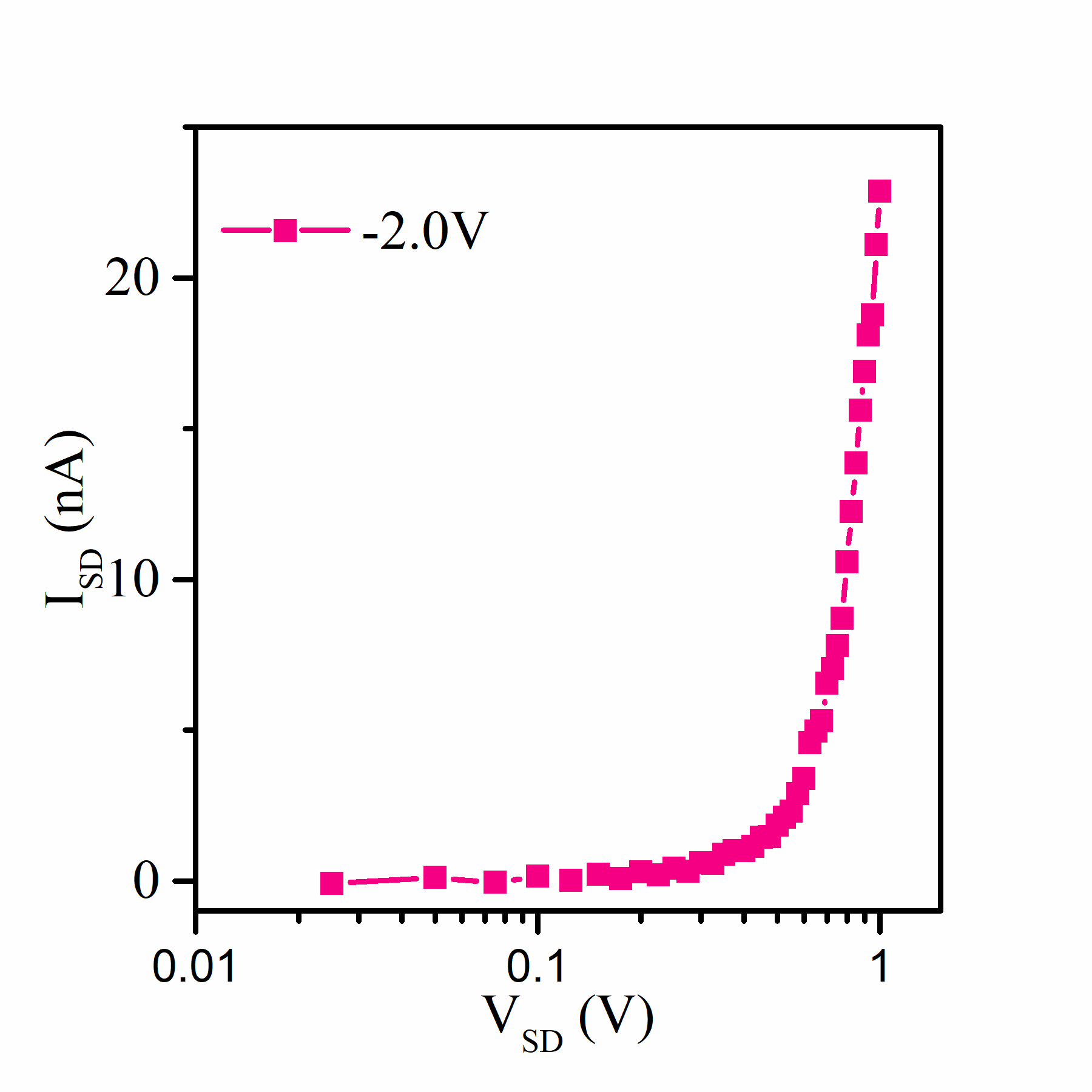
**Π. Charge Transferred based Switching (CTS) Characteristic of the Device**



(a)



(b)

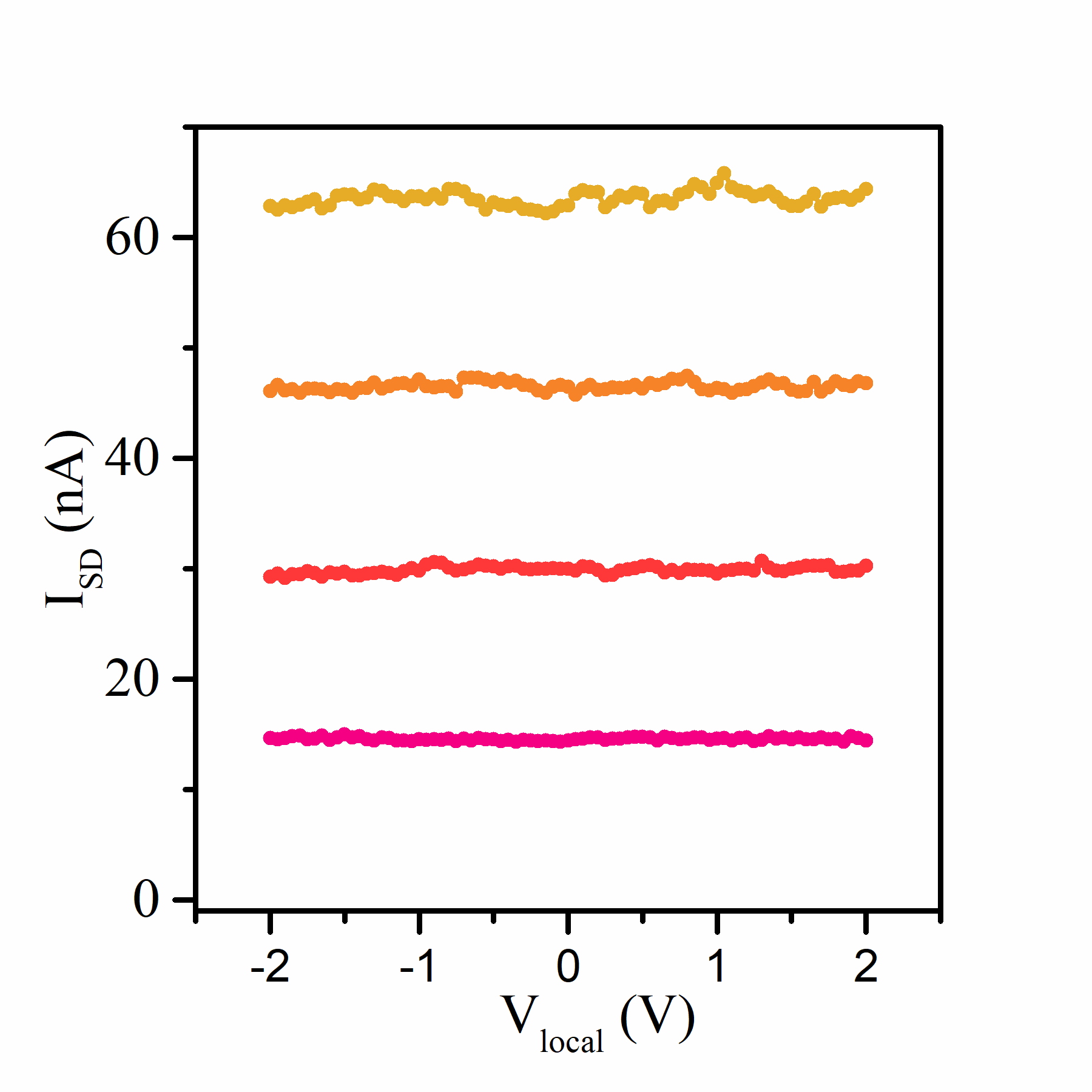


(c)

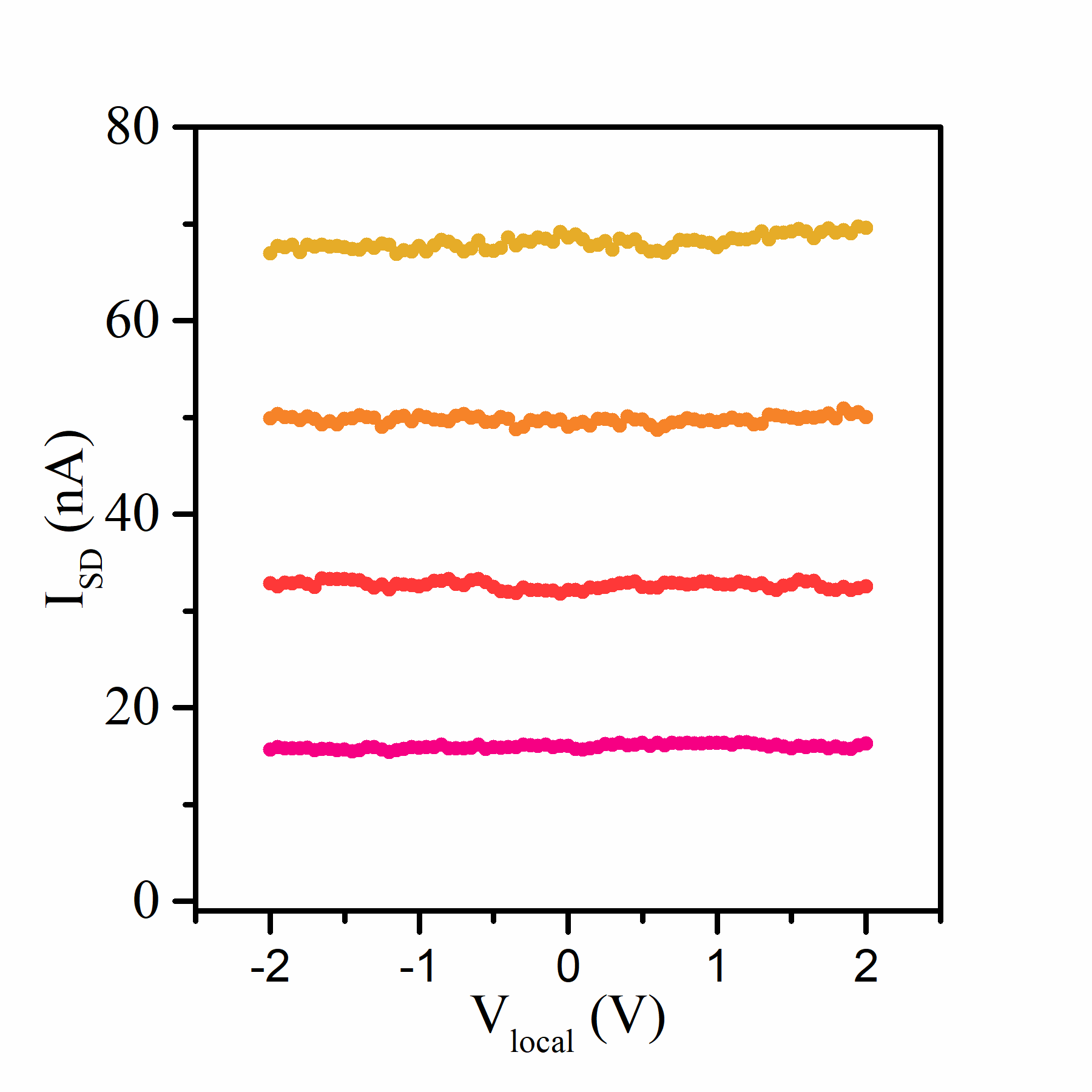
**Figure S2.** (a) Switching behavior of the device for 1000 nm local gate width with different device (D2). (b) ISD-VSD plot with different local gate voltages in logarithmic scale for D2. (c) Exponential increment of current with VSD for -2V Vlocal a typical signature of tunneling presented in D2.

Figure S2(a) shows a change in resistance with local gates which shows a clear transition from OFF state to ON state by controlling the transfer of charges from source to drain for device 1 (D1) and device 2 (D2). Each device shows quite similar kind of trend which is well reproduceable for each device. On the other hand, the charge transfer-based switching (CTS) is well modulated by the local gate voltages (Vlocal). At positive Vlocal the ISD becomes linear with VSD clearly indicating the barrier free nature of the channel which is shown in Figure S2(b). To evaluate the phenomena more, we have plotted the ISD with VSD at -2V Vlocal which is showing an exponential relation due to tunneling of the carriers. In contrast to that for +2V Vlocal there is linear change in ISD shows the direct movement of the carrier in the channel without any barrier. The exponential change of drain current with VSD is shown in Figure S2(c) for D2 which further confirms the presence of barrier for -2V Vlocal in case of D2. Also, we have evaluated the molecular switching phenomena for D2 which has shown a consistent result with the earlier one.

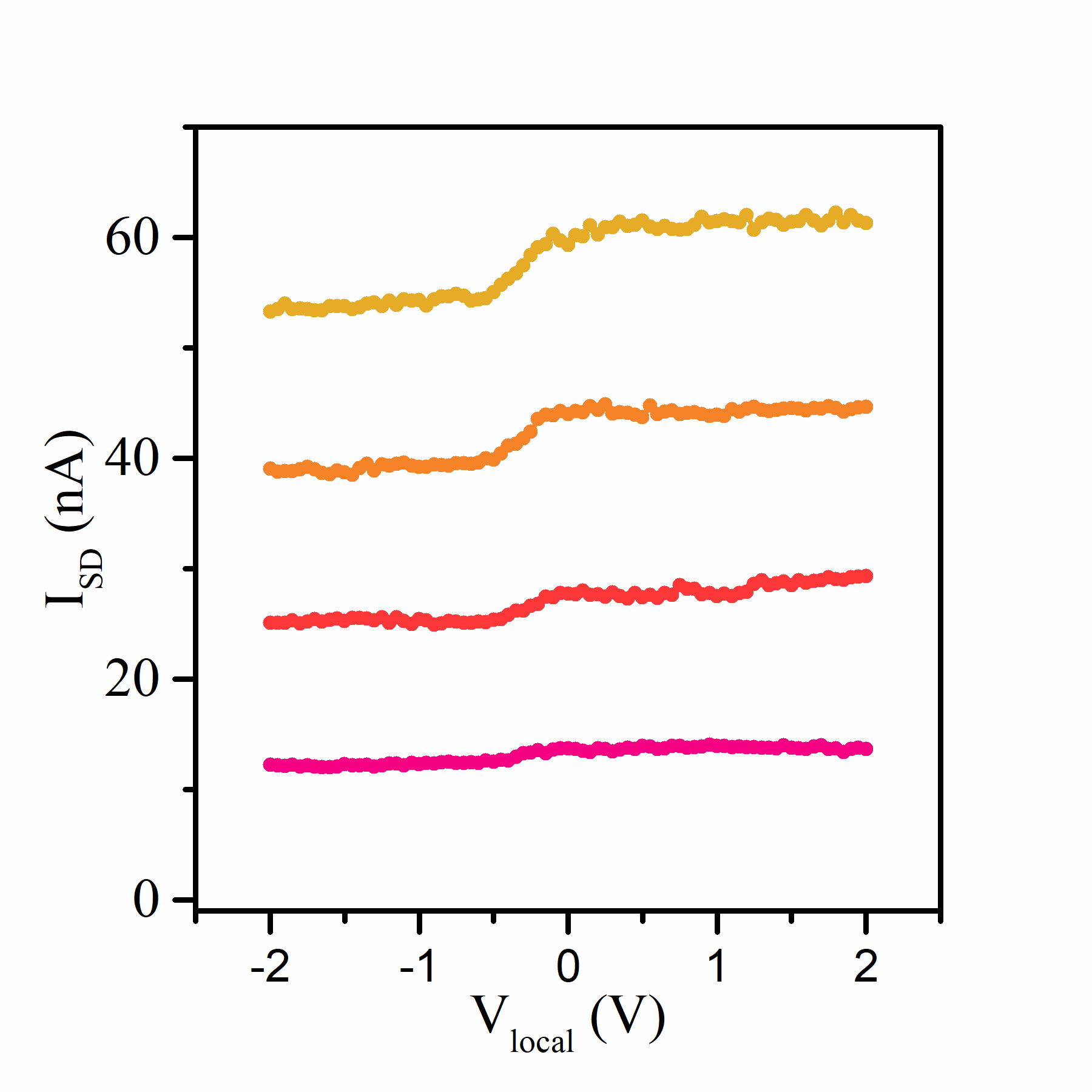
**Ⅲ. Local Gate Width Dependent Charge Transferred based Switching (CTS) Characteristic of the Device**



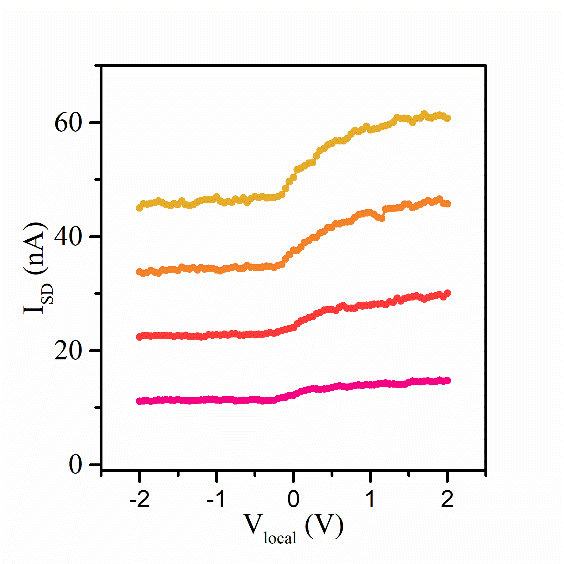
(a)



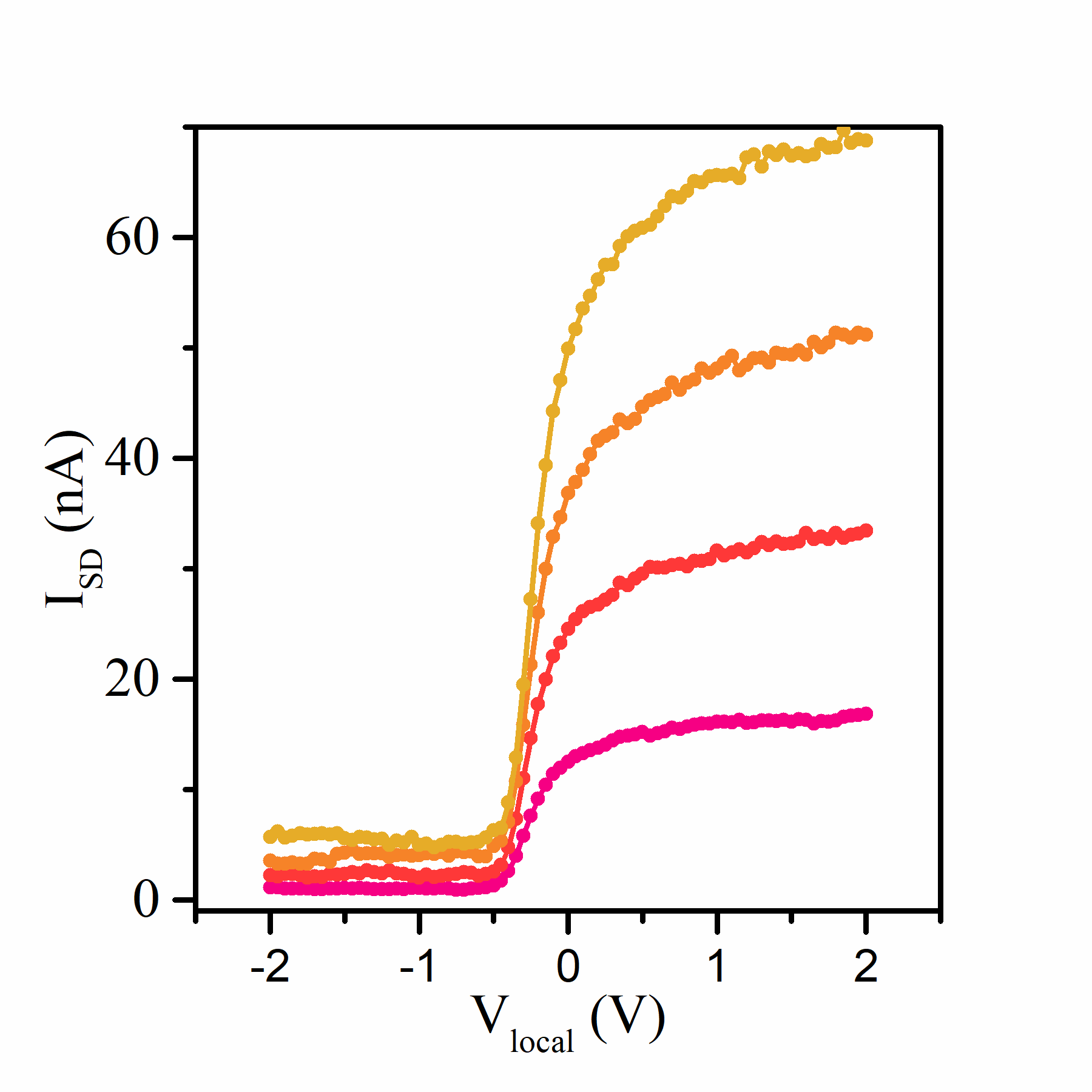
(b)



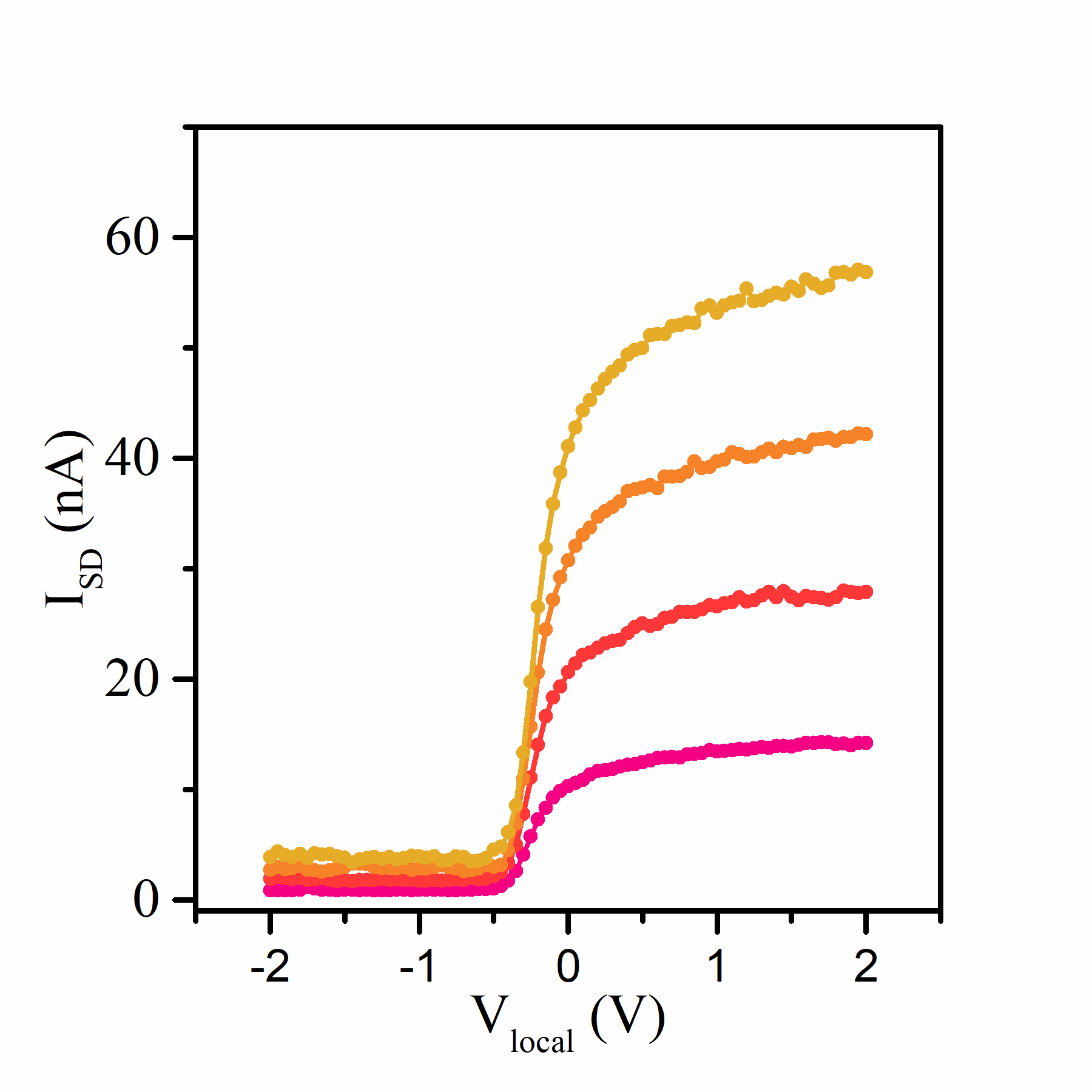
(c)



(d)



(e)

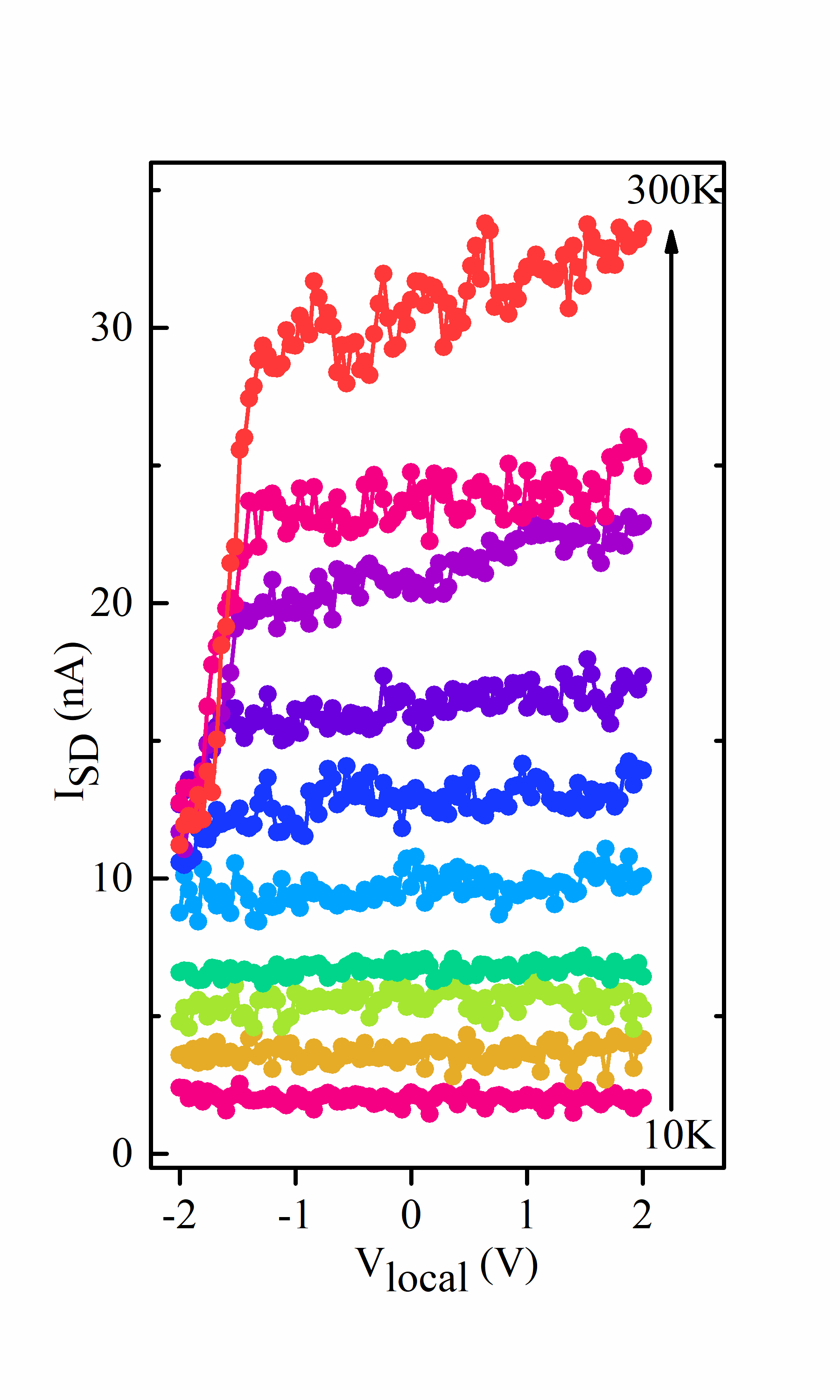


(f)

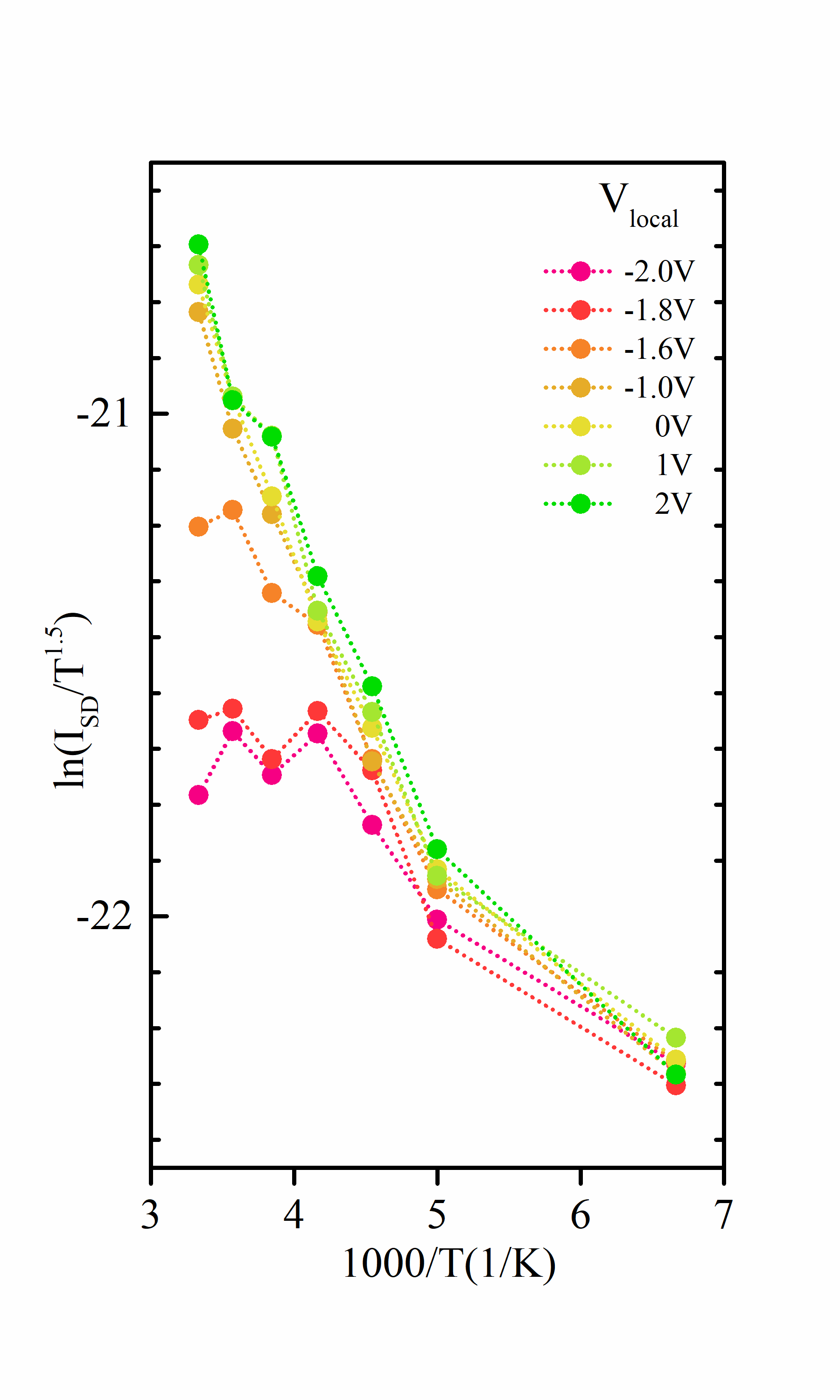
**Figure S3**. Evolution of blocking channel with different width of local gates (a) 50 nm (b) 100 nm (c) 200 nm (d) 500 nm (e) 800 nm (f) 1000 nm for same source-drain bias voltage at room temperature.

The CTS phenomena highly depends on the barrier width which can be seen in Figure S2. We have modulated the local gate width *Wlocal = 50-1000* nm to see the effect of width on channel conductance. Figure S3(a) shows the drain current for different VSD where there is no modulation of current in the channel for 50 nm width. As the width increases, we gradually starting to see the change ISD as shown in Figure S3(b) and (c) for 200 nm width. The complete modulation is observed for higher gate width which can be seen in Figure S3(e) and (f).

**Ⅳ. Temperature Dependent CTS Characteristic of Heterostructure**



(a)



(b)

**Figure S4.** (a) Temperature dependent study of the device for 200 nm width of local gates. (b) Arrhenius plot for different temperature at a fixed source drain bias.

The temperature dependent carrier transport was also done for a *Wlocal =200* nm. The temperature is varied from 10K to 300K for fixed VSD of 1V. The modulation of ISD is observed around 200K and increases with temperature as shown in Figure S4(a). The Arrhenius plot in Figure S4(b) shows the dependence of temperature on drain current with different Vlocal which is deviate at -Vlocal and the modulation occurs near room temperature.

**Ⅴ. Molecular Adsorption calculation of The Device**

A close up of a logo

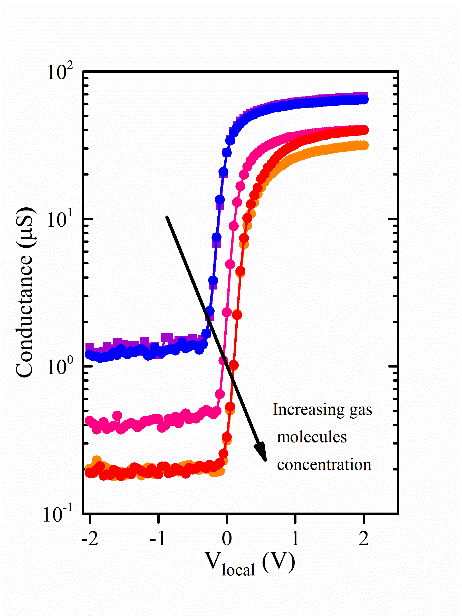
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**Figure S5.** Adsorption rate calculation for 1000 nm local gate width of the device

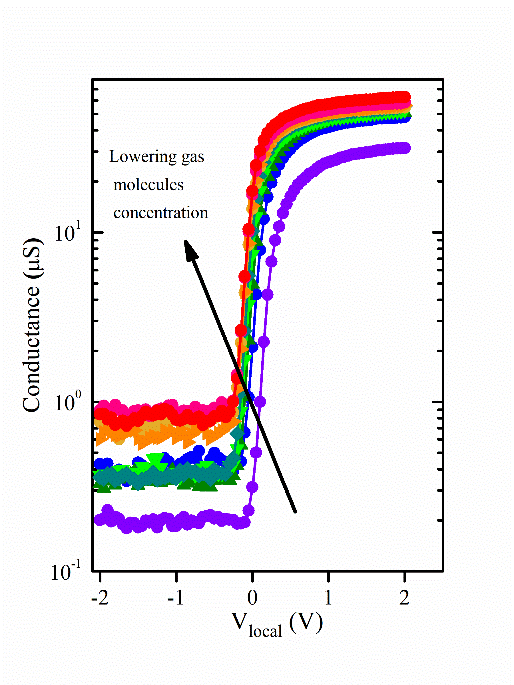
The charge transfer dynamics of the adsorption/desorption of the gas molecules can be understood with a simplified model, . The value of adsorption rate can be extracted by fitting the curve to an equation , where is the number of molecules injected in the system, is the initial adsorption density and is the desorption density in MoS2 and is the adsorption rate. The extracted values of n0pa and 1/a are 7.20×1011 cm2/min and 0.104%/min, respectively, showing molecules adsorption density of 7.20×1011 cm2/min on MoS2 and 0.104% of them desorbing in a minute.

**Ⅵ. Molecular Sensing for Different Gate Width**

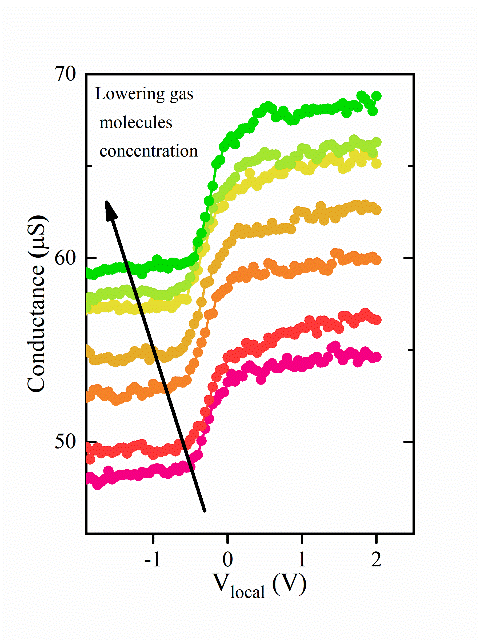
**Figure S6** (a) The molecular switching operation in the D2 for 1000 nm local gate (b) The change in drain before and after molecular exposure for 50 nm local gate. (c) Molecular response for 800 nm width of local gate. (d) Recovery after molecular exposure for 800 nm local gate. (e) Molecular response of the device for 500 nm local gate width (f) Recovery after molecular exposure for 500 nm local gate



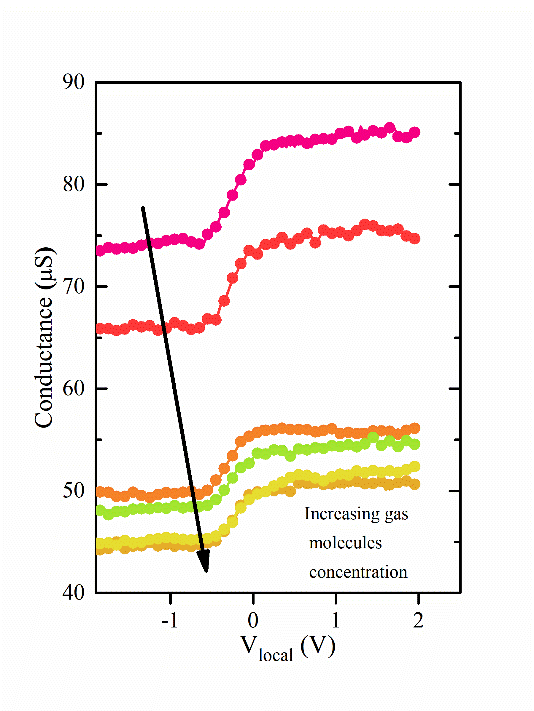
(c)



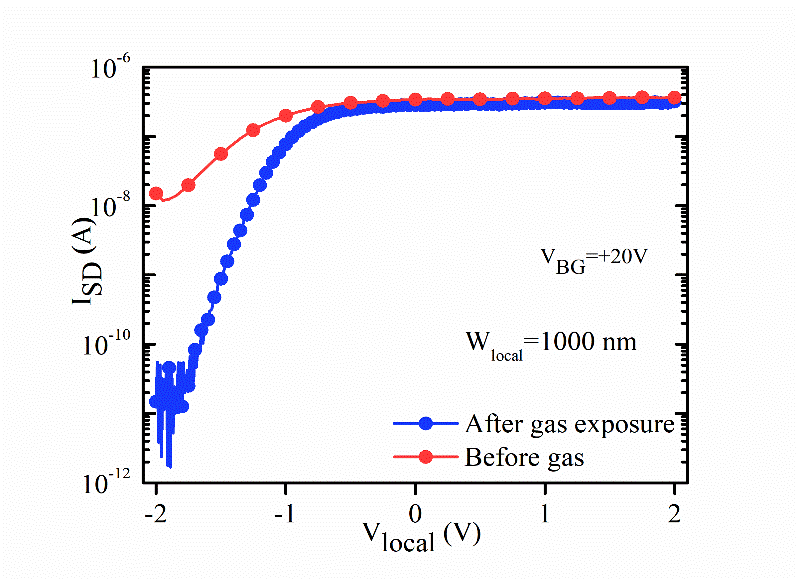
(d)



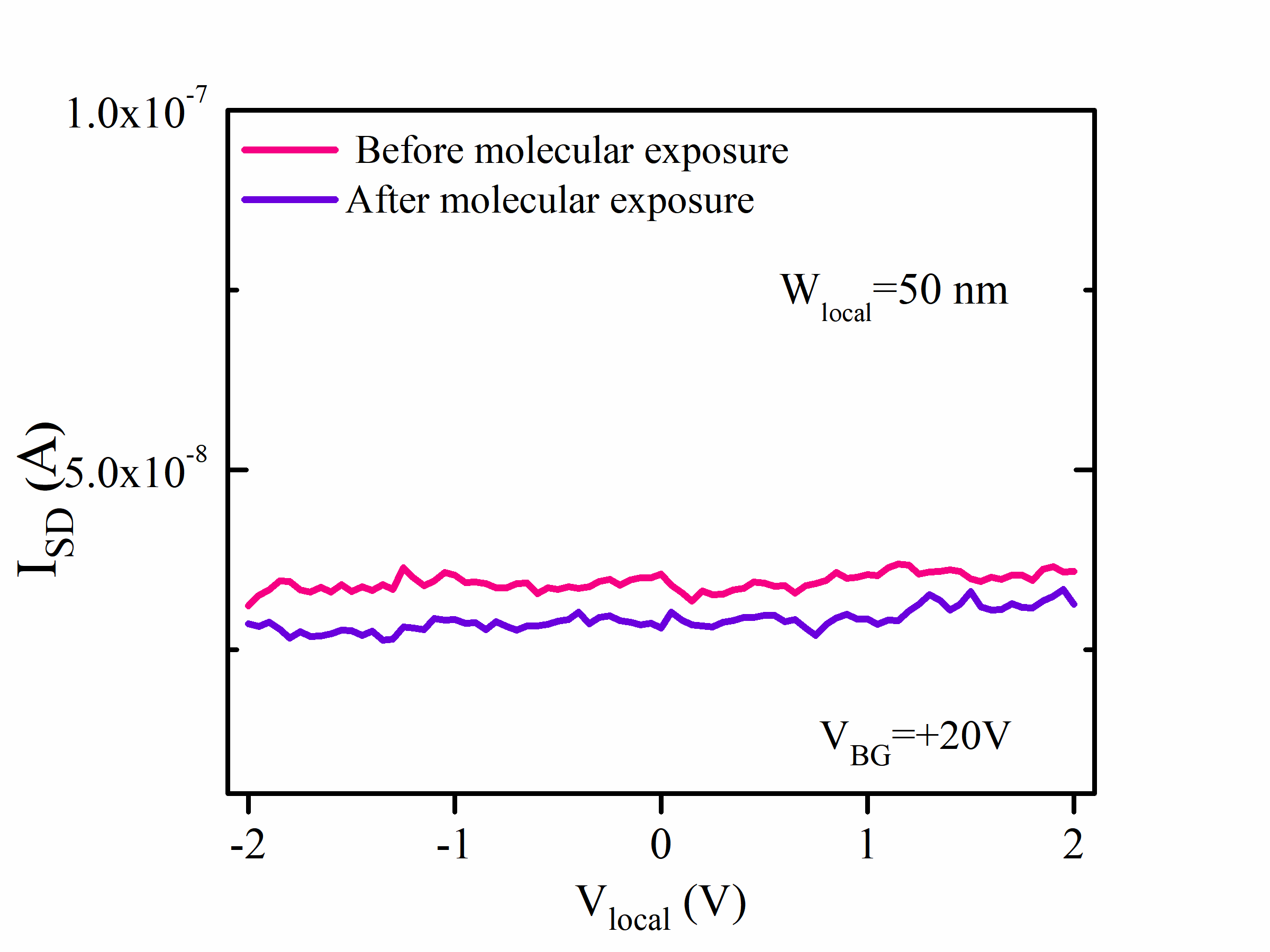
(f)



(e)



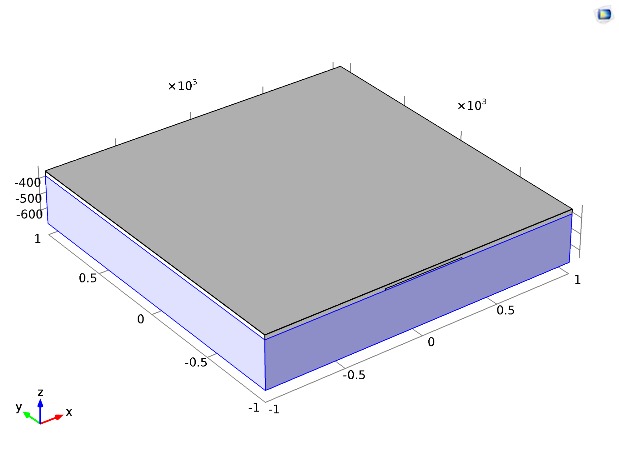
(a)



(b)

Molecular sensing performance was done with different width local to get a clear idea on the effect of the barrier on molecular interaction. The molecular switching for Vlocal=-2V is also observed which is not present in case of +2V Vlocal as depicted in Figure S6(a). The width dependent study of the device was also done in presence of gas molecules. Figure S6(b) shows the change in drain current in case of 50 nm gate width where the molecular switching operation is not possible as discussed earlier. Figure S6(c) shows the molecular interaction for 800 nm local gate width. The change in conductance shows that there is a modulation in conductance with decreasing in conductance value up to 10 order. Figure S6(d) shows an increase in conductance after reducing molecular concentration. Furthermore, the molecular sensing was also done for 500 nm local width and shown in Figure S6(e). A less change in device conductance was observed with molecular exposure and which is found out to be only 2 times without molecular exposure. The value is almost returned to its base value after removing molecular exposure as shown in Figure S6(f). In conclusion the sensitivity of the molecular switching operation is highly dependent on local gate widths and can be tuned using local gate voltages.

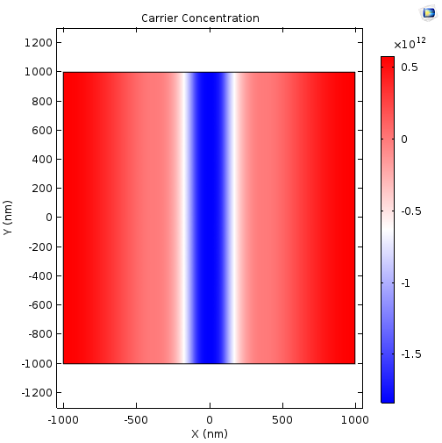
**Ⅶ. COMSOL Multiphysics Simulation for Potential Barrier Simulation**



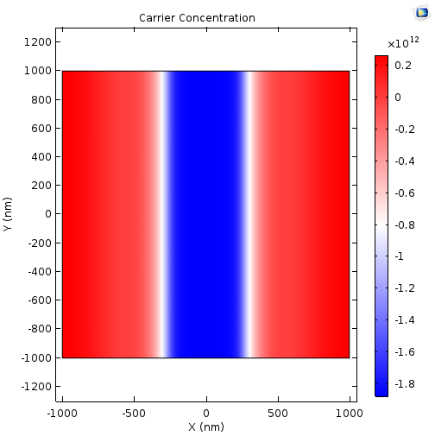
(a)



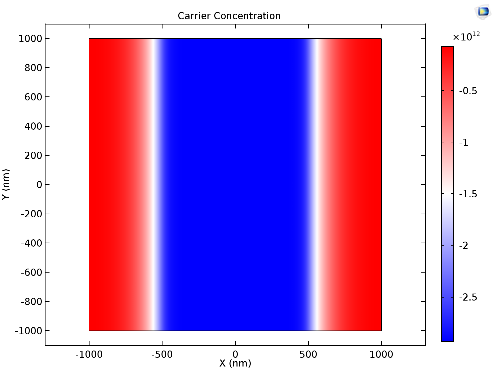
(b)



(c)



(d)



(e)

**Figure S7** (a) Device structure (b) The surface potential plot for a fixed back gate and -4V local gate voltage. The carrier concentration variation with the different width of the local gate electrode (c) 200 nm (d) 500 nm (e) 1000 nm

The barrier potential in MoS2 device was modeled in detail using the finite element analysis software COMSOL Multiphysics 5.2. The dimensions of the local gate and the thicknesses of the SiO2 and h-BN layers are close to those of the measured device which is 300 nm and 25 nm. The material parameters of the Au electrode were obtained from the COMSOL simulation software are used for the finite element analysis. The dielectric constant of h-BN and SiO2 material are taken 3.4 and 4. The MoS2 sheet is modeled by a charge density linked to the electrostatic potential V by the relation of a signum function. The geometry of the simulation is represented in Figure S7(a). A detailed analysis of the electrostatics potentials is done using the electrostatics node in Multiphysics tool with proper boundary conditions as depicted in Figure S7(b). The stationary solution was taken into account for the simulation using Poison’s electrostatic equation with charge conservation. The profile of the potential energy E = −eV across the local gated region is calculated for a fixed back-gate voltage and various local gate voltages and local gate widths which is shown in Figure S7(c), (d) and (e).