

# Astability versus Bistability in van der Waals Tunnel Diode for Voltage Controlled Oscillator and Memory Applications

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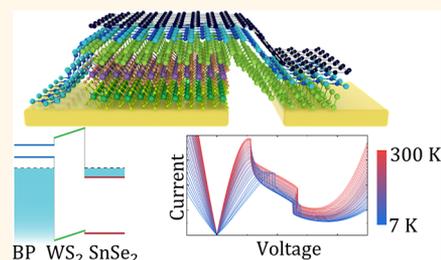
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**ABSTRACT:** van der Waals (vdW) tunnel junctions are attractive because of their atomically sharp interface, gate tunability, and robustness against lattice mismatch between the successive layers. However, the negative differential resistance (NDR) demonstrated in this class of tunnel diodes often exhibits noisy behavior with low peak current density and lacks robustness and repeatability, limiting their practical circuit applications. Here, we propose a strategy of using a 1L-WS<sub>2</sub> as an optimum tunnel barrier sandwiched in a broken gap tunnel junction of highly doped black phosphorus (BP) and SnSe<sub>2</sub>. We achieve high yield tunnel diodes exhibiting highly repeatable, ultraclean, and gate-tunable NDR characteristics with a signature of intrinsic oscillation, and a large peak-to-valley current ratio (PVCR) of 3.6 at 300 K (4.6 at 7 K), making them suitable for practical applications. We show that the thermodynamic stability of the vdW tunnel diode circuit can be tuned from astability to bistability by altering the constraint through choosing a voltage or a current bias, respectively. In the astable mode under voltage bias, we demonstrate a compact, voltage-controlled oscillator without the need for an external tank circuit. In the bistable mode under current bias, we demonstrate a highly scalable, single-element, one-bit memory cell that is promising for dense random access memory applications in memory intensive computation architectures.

**KEYWORDS:** tunnel diode, van der Waals heterostructure, negative differential resistance, voltage controlled oscillator, random access memory



Nonlinear electronic devices play a pivotal role in wide ranging applications including oscillators, amplifiers, switching elements,<sup>1,2</sup> and more recently in neural networks.<sup>3,4</sup> Devices exhibiting negative differential resistance (NDR) characteristics, where a negative correlation exists between device current and voltage, are excellent candidates for these interesting applications. Following the landmark discovery by Esaki,<sup>5</sup> tunnel diodes employing band-to-band tunneling (BTBT) have been an active area of research because of their NDR behavior and ultrafast response due to the tunnelling nature of the carrier transport. Maintaining a sharp junction with a steep doping gradient is a key factor in achieving high tunneling efficiency in a tunnel diode. In this context, two-dimensional layered materials and their van der Waals (vdW) heterojunctions are highly promising<sup>6–17</sup> because of their atomically sharp junctions, which can substantially reduce the process complexity and cost as opposed to bulk semiconductors. The wide collection of layered materials allows us to choose the desirable band offset in a vdW heterojunction without worrying about the lattice mismatch between two successive layers,<sup>18,19</sup> providing a tremendous advantage over bulk semiconductors. In addition, tunnel diodes with the ultrathin layers provide strong gate

tunability,<sup>6–15</sup> a trait that is usually unavailable in conventional tunnel diodes.

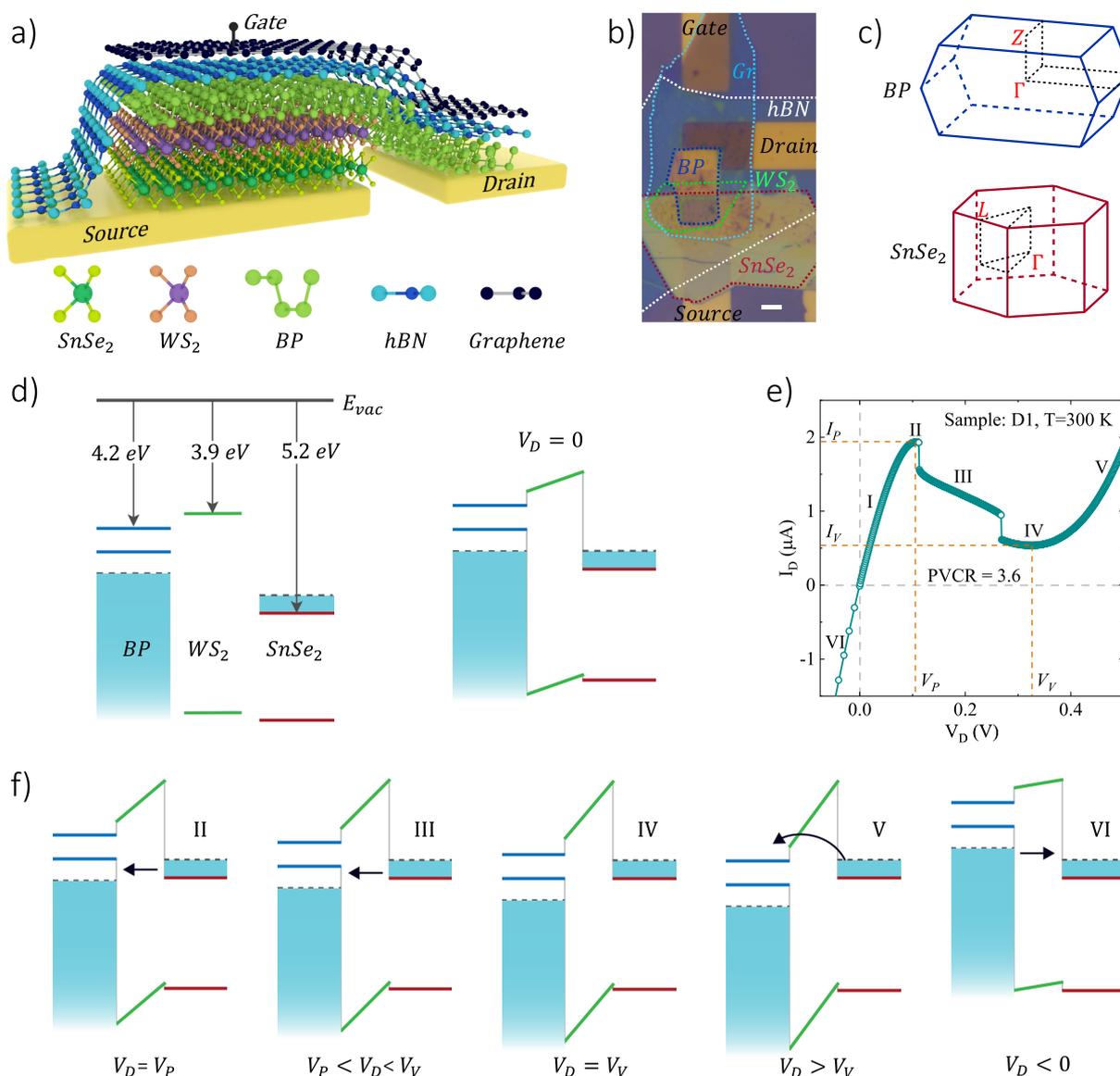
However, in a vdW heterojunction, the absence of a conventional depletion region due to the ultrathin nature of the layers and an atomic sharpness of the interface prevents a voltage drop at the tunnel junction, which degrades the NDR characteristics. This is because, for NDR to be observable, the tunneling current through the p–n junction must be tunable, which requires a voltage modulation of the spectral overlap between the filled states at the conduction band of the n-side and the empty states at the valence band of the p-side. One thus requires the presence of a spatial gap between the n and p regions created during the transfer process or unintentional oxidation or a tunnel barrier that acts like an artificial depletion region to accommodate the required voltage drop at the tunnel

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**Figure 1.** Tunnel diode operation: (a) Schematic illustration of the SnSe<sub>2</sub>/1L-WS<sub>2</sub>/BP tunnel diode with an encapsulating hBN layer and a graphene gate. (b) Representative optical image of the heterostructure outlining the various layers. Scale bar is 5 μm. (c) Brillouin zones for bulk BP (top) and bulk SnSe<sub>2</sub> (bottom). Z and L valleys correspond to valence band maxima of BP and conduction band minima of SnSe<sub>2</sub>, respectively. (d) Energy band alignment of the layers before (left) and after (right) contacting, suggesting broken gap alignment between BP and SnSe<sub>2</sub> with an ultrathin 1L-WS<sub>2</sub> tunnel barrier. (e) Measured output characteristics of the tunnel diode (D1) exhibiting a PVCR of 3.6 at 300 K. Various regions of operation under forward bias (Esaki mode) are marked as I through V, whereas the reverse bias (Zener mode) is shown as region VI. (f) Energy band alignment for different regions of operation (see text for details). Black arrows indicate electron-transport direction.

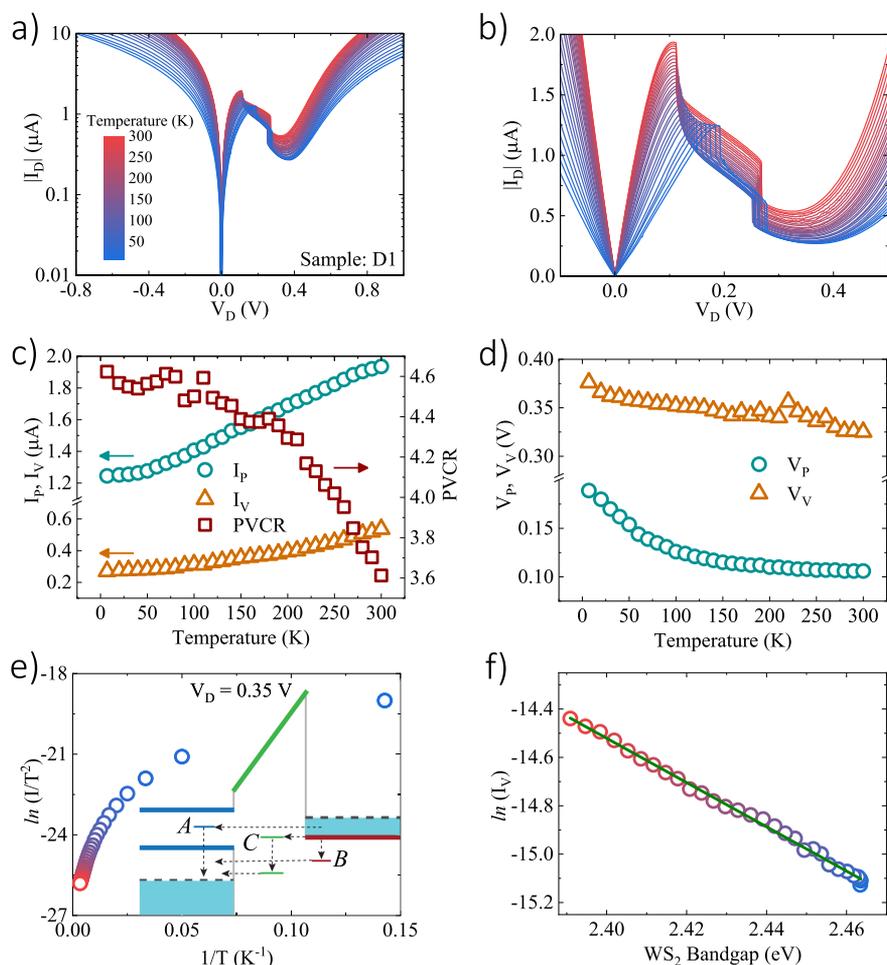
junction. Relying on these processes takes a toll on the device yield, and the achieved NDR characteristics are inferior compared to state of the art Si and III–V semiconductor-based tunnel diodes,<sup>20,21</sup> in terms of limited peak current density, poor repeatability, and large noise present in the tunneling current. This has led to limited efforts to use vdW heterojunction-based tunnel diodes in real-life applications,<sup>6,8</sup> and thus non-Esaki vdW devices are being explored to achieve NDR.<sup>22</sup>

In this work, by optimizing the tunnel barrier layer and using a clean device fabrication technique that maintains the high quality of the interfaces, we demonstrate a SnSe<sub>2</sub>/1L-WS<sub>2</sub>/BP vdW heterostructure-based broken gap tunnel diode that exhibits ultraclean, highly repeatable, and gate-tunable NDR

characteristics with a large peak-to-valley current ratio (PVCR). We also show that the thermodynamic stability of the tunnel diode circuit in the NDR regime can be switched by changing the external constraint from voltage bias to a current bias. This allows us to further demonstrate a reactive-element-free persistent oscillation in an astable mode and a highly scalable memory cell in a bistable mode of operation of the vdW heterojunction tunnel diode.

## RESULTS AND DISCUSSIONS

Architecture of the SnSe<sub>2</sub>/1L-WS<sub>2</sub>/BP tunnel diode is schematically illustrated in Figure 1a. Mechanically exfoliated multilayer SnSe<sub>2</sub> flakes are identified by optical contrast and are dry transferred on to prepatterned Au electrodes. 1L-WS<sub>2</sub>

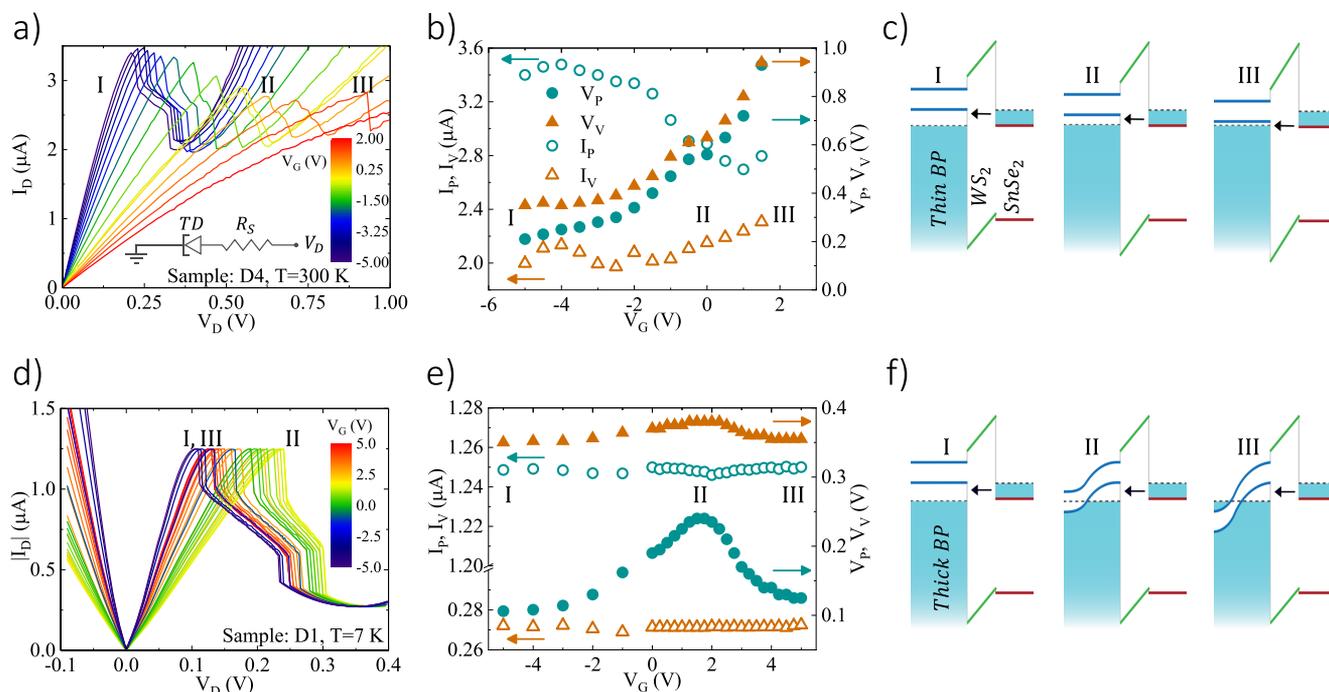


**Figure 2.** Temperature dependence of tunnel diode characteristics: (a)  $I_D - V_D$  curves from sample D1 at temperatures ranging from 7 to 300 K in log scale. (b) Enlarged view of the NDR region in linear scale. (c) Left axis: Extracted peak (circle markers) and valley (triangle markers) currents versus operating temperature. The strong temperature dependence for  $I_p$  suggests a phonon-assisted tunnelling transport. Right axis: PVCR (square markers) of the device at each operating temperature. (d) Variation in peak (circle markers) and valley (triangle markers) positions with temperature. (e) Richardson plot for  $I_D$  near valley ( $@V_D = 0.35$  V) exhibiting a positive slope, indicating an origin of valley current different from thermionic process. Color of the markers are mapped to the measurement temperature. Inset: various transport pathways through gap states for the generation of excess current. (f) Variation in  $I_v$  with a temperature-induced bandgap change of  $WS_2$  (circle markers with color mapped to temperature). Good agreement with the linear fit (green trace) suggests a defect-induced origin of excess current.

and multilayer BP flakes are stacked over the  $SnSe_2$  flake with precise alignment following the same method. The other end of the BP layer is in contact with another Au electrode. The entire stack is immediately capped with a few-layer-thick hBN flake. The hBN flake serves the dual role of a protective capping for the BP flake<sup>23,24</sup> and that of a gate dielectric. The top gate contact is defined using a few-layer graphene flake that is connected to a third Au electrode. The flakes are characterized using Raman spectroscopy as shown in Figure S1. The fabrication approach we employ here utilizing prepatterned contacts does not require any chemical processing step after the flake transfer, and thus preserves the pristine nature of the BP interface. More details of the fabrication process are given in Methods and illustrated stepwise in Figure S2. A representative optical image of the stack is shown in Figure 1b. The Au electrode contacting the  $SnSe_2$  (BP) flake is referred to as the source (drain) contact throughout the text. We measure the drain current ( $I_D$ ) by applying an external voltage ( $V_D$ ) at the drain contact, keeping the source terminal grounded. Seven such tunnel diodes (D1–

D7) are fabricated, and all the devices exhibit repeatable NDR characteristics (summarized in Table S1), pointing to the high yield of the fabrication process.

Band extrema of interest occur at the Z valley for the BP<sup>25</sup> valence band and at the L valley for  $SnSe_2$ <sup>26</sup> conduction band as shown in Figure 1c. The presence of vacancies and impurities induce a large p-type doping in BP<sup>27,28</sup> and a large n-type doping in  $SnSe_2$ .<sup>17</sup> The degenerate doping and large band offsets between BP<sup>6</sup> and  $SnSe_2$ <sup>7,29–31</sup> result in a type-III (broken gap) band alignment at the heterojunction<sup>17</sup> (Figure 1d). Under forward bias, the electrons experience inelastic band-to-band tunneling (BTBT) from the filled states of  $SnSe_2$  conduction band to the empty states of BP valence band through the monolayer-thick  $WS_2$  tunnel barrier. The current-voltage ( $I_D - V_D$ ) characteristics of the tunnel junction D1 at 300 K is shown in Figure 1e, indicating a large current under reverse bias (Zener mode) and conspicuous NDR characteristics under forward bias (Esaki mode)—a direct evidence of BTBT dominated carrier transport.<sup>5</sup> The band alignment in the heterojunction under different regions of operation is



**Figure 3.** Gate modulation of tunnel diode characteristics for thin and thick BP layers: (a)  $I_D$ – $V_D$  curves from sample D4 employing a thin BP layer at 300 K as a function of gate bias ranging from 2 to –5 V. Inset: An equivalent circuit of the heterostructure showing the series resistance of the lateral channel  $R_s$  and the tunnel junction. (b) Left axis: Modulation of peak (empty teal circle markers) and valley (empty orange triangle markers) currents with gate bias. Increase in  $I_p$  is consistent with an increasing p-doping in BP at negative  $V_G$ .  $I_V$  originating from excess current exhibits a weaker dependence on  $V_G$ . Right axis: Peak (solid teal circle markers) and valley (solid orange triangle markers) positions occurring at larger voltages with an increasing drop across  $R_s$  with increasing  $V_G$ . (c) Band alignment corresponding to  $I_p$  at negative  $V_G$  (I), near-zero  $V_G$  (II), and positive  $V_G$  (III). (d)  $I_D$ – $V_D$  curves from sample D1 employing a thick BP layer at 7 K as a function of gate bias ranging from 5 to –5 V. (e) Extracted peak and valley currents (left axis) and positions (right axis) from D1. Invariance of  $I_p$  with  $V_G$  suggests a fixed p-doping at the tunnelling interface.  $V_p$  and  $V_v$  gets modulated according to the variation of  $R_s$  with  $V_G$ . (f) Band alignment at peak configuration corresponding to (I) increased doping at the top interface of the BP channel at negative  $V_G$ , (II) maximum channel resistance at slightly positive gate bias due to the depletion region formed near top of BP, and (III) e–h bilayer formation at the BP layer at further positive  $V_G$  and a subsequent reduction of  $R_s$ .

depicted in Figure 1f. Under forward bias,  $I_D$  increases linearly with  $V_D$  at low bias (region I) to a “peak current”  $I_p$  (point II, at  $V_D = V_p$ ), which is attributed to an increasing overlap between filled states in the  $\text{SnSe}_2$  conduction band and empty states in the BP valence band. With the further increase in  $V_D$ ,  $I_D$  drops abruptly, followed by a gradual reduction (region III) and another abrupt drop and then a slow decrease to a minimum “valley current”  $I_V$  (region IV, at  $V_D = V_v$ ). Such a decrease in  $I_D$  with an increase in  $V_D$  in between the peak and the valley points indicates the presence of NDR in the DC characteristics. This decrease in  $I_D$  is due to a reduction in the overlapping states beyond  $V_D = V_p$ . Beyond the valley point,  $I_D$  again increases with a further increase in  $V_D$  because of an enhancement in the thermionic current over the BP/ $\text{SnSe}_2$  barrier. The diode achieves a high PVCr ( $\frac{I_p}{I_V}$ ) of 3.6 at 300 K. The abrupt drops in the  $I_D$  characteristics has not been observed to date in vdW tunnel diodes<sup>6–17</sup> and indicate the presence of oscillations in the diode<sup>32</sup> which will be explained later.

As explained earlier, BP and  $\text{SnSe}_2$  form a broken gap vdW heterojunction, which is ideally suited for high BTBT current. However, in the absence of the 1L- $\text{WS}_2$  tunnel barrier, because of the high conductivity of such a junction along with its atomic sharpness, there is very little voltage drop across the junction. This forces the quasi-Fermi levels of the BP and the  $\text{SnSe}_2$  sides to be almost aligned at the tunneling interface in

spite of a change in the applied external bias. This degrades the PVCr, with a possibility of complete suppression of NDR characteristics, although the total tunneling current remains high. When we introduce the  $\text{WS}_2$  sandwich layer, it acts like an atomically sharp depletion layer, allowing a larger voltage to drop across it. This effectively depins the BP and  $\text{SnSe}_2$  bands at the tunneling interface, allowing their relative movement, which is crucial in observing the NDR characteristics.<sup>17,20</sup> Clearly, it is critical to optimize the thickness of the barrier layer to achieve the optimum device performance. The results of tunnel diodes fabricated with different barrier layers (no barrier layer (D8), 1L- $\text{WS}_2$  (D1), 2L- $\text{WS}_2$  (D9), and 1L- $\text{MoS}_2$  (D10)) are summarized in Table S2. We observe that the device with no barrier exhibits an order of magnitude higher tunneling current, however, with no NDR signature (Figure S3a). The device with 2L- $\text{WS}_2$  as a barrier layer (Figure S3c) exhibits a PVCr of  $\sim 2$ , but with significantly suppressed tunneling current due to increased barrier width. An annealing step in the fabrication also helps in reducing the interlayer spacing. As can be seen from samples D2 and D3 (Table S1), the current density increases drastically with an annealing step after  $\text{WS}_2$  transfer with no degradation of PVCr. The tunnelling current for 1L- $\text{MoS}_2$  (Figure S3d) and 1L- $\text{WS}_2$  barrier devices are comparable; however, the NDR characteristics are far superior and cleaner in the latter case, likely due to a higher defect density in  $\text{MoS}_2$ .<sup>33,34</sup>

To investigate the current transport mechanisms at different regions of operation, we measure the  $I_D$ – $V_D$  characteristics of the device D1 at various temperatures ranging from 7 to 300 K, as shown in Figure 2a. A magnified view of the NDR region in linear scale is given in Figure 2b. The NDR characteristics and the low-noise nature is maintained in the entire temperature range pointing to the stability of the processes and the high quality of the interfaces. The strong temperature dependence of the peak current points to a phonon-assisted inelastic tunneling process.<sup>35,36</sup> This is in agreement with the fact that conduction band minimum at SnSe<sub>2</sub> being at the *L* point, whereas the valence band maximum of BP is at the *Z* point (see Figure 1d), requiring the assistance of phonon for in-plane momentum conservation during the tunnelling process.<sup>37</sup>

Extracted temperature dependence of the peak and the valley currents and the corresponding voltages are given respectively in Figure 2c, d. Figure 2c shows that with a reduction in temperature,  $I_V$  reduces at a slightly faster rate than  $I_P$ , improving the PVCRC to  $\sim 4.6$  at low temperature. However,  $I_V$  appears to be a much weaker function of temperature than the thermionic process, suggesting a nonthermionic origin of the valley current. To establish the point quantitatively, using the Richardson equation,<sup>38</sup> we plot  $\ln\left(\frac{I_V}{T^2}\right)$  as a function of  $\frac{1}{T}$  in Figure 2e. The positive slope observed clearly suggests that the valley current is not dominated by the thermionic current over the BP conduction band barrier. Such nonthermionic current at the valley is common in the tunnel diode literature<sup>39,40</sup> and is usually attributed to the excess current. The excess current originates from carrier transport through the sub-bandgap states created by structural disorders and impurities, and several possible transport mechanisms are schematically illustrated in inset of Figure 2e. The carriers from either of the degenerate regions of BP or SnSe<sub>2</sub> can lose energy and drop to states in the otherwise forbidden band gap (paths A and B). These carriers then tunnel to the other side resulting in a nonzero valley current. The nonzero defect density present in the WS<sub>2</sub> barrier layer also acts as an intermediate state for the excess current (path C). Considering the bandgap ( $E_G$ ) of 1L-WS<sub>2</sub> as the effective energy gap the carriers need to overcome to generate the excess current, we first map the bandgap of 1L-WS<sub>2</sub> at different measurement temperatures,<sup>41</sup> and then plot  $\ln(I_V)$  as a function of the corresponding  $E_G$  in Figure 2f. The linear trend with negative slope provides further evidence of the defect induced excess current as the primary source of valley current.<sup>39</sup> The nonthermionic origin of  $I_V$  sets a lower bound on the valley current and hence causes the PVCRC to saturate at low temperature, as shown in right axis of Figure 2c. The suppression of the excess current by reducing the defect density through the usage of higher-quality flakes is thus of paramount importance to further reduce  $I_V$  and achieve a PVCRC limit determined by the thermionic current.

In the presence of nonzero series resistance, the external bias required to achieve peak or valley configurations is given by

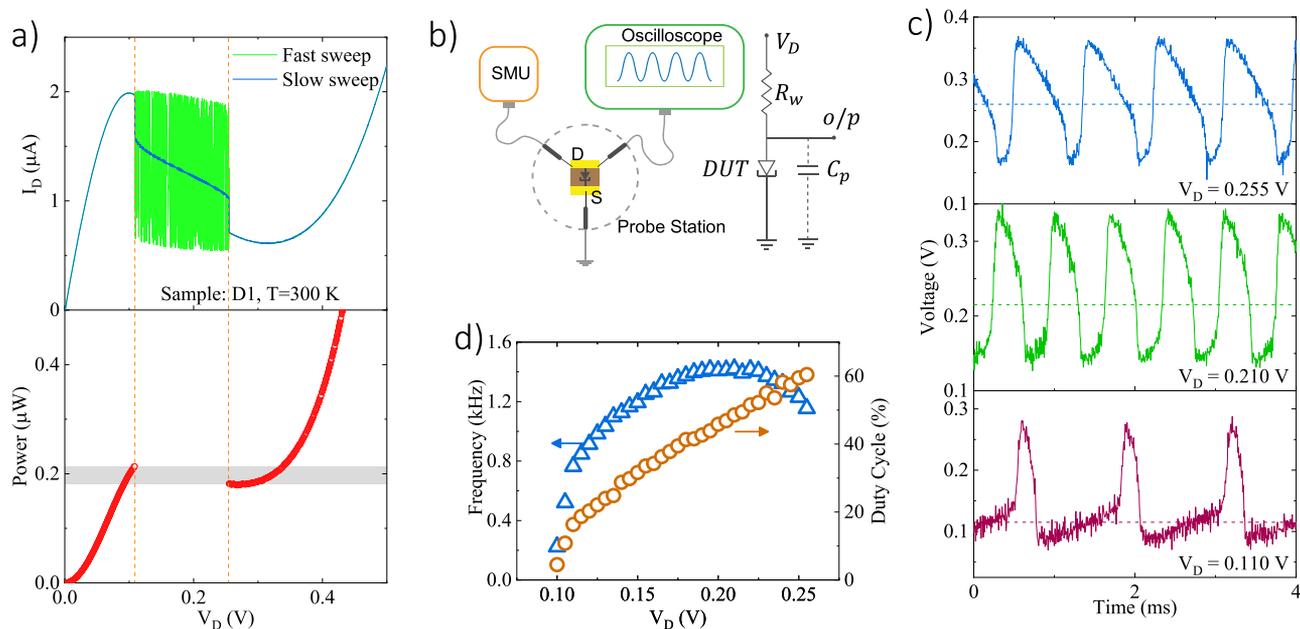
$$V_{p,v}(T) = V_{p,v}^0 + I_{p,v}(T)R_s(T) \quad (1)$$

where  $V_{p,v}^0$  is the drop at the junction at peak or valley, and  $R_s(T)$  is the temperature dependent series resistance. The measured  $V_P$  and  $V_V$  are shown in Figure 2d as a function of the temperature. The increase in  $V_P$  and  $V_V$  with a decrease in temperature results from an increase in  $R_s$  due to a lower injection efficiency at the contact.

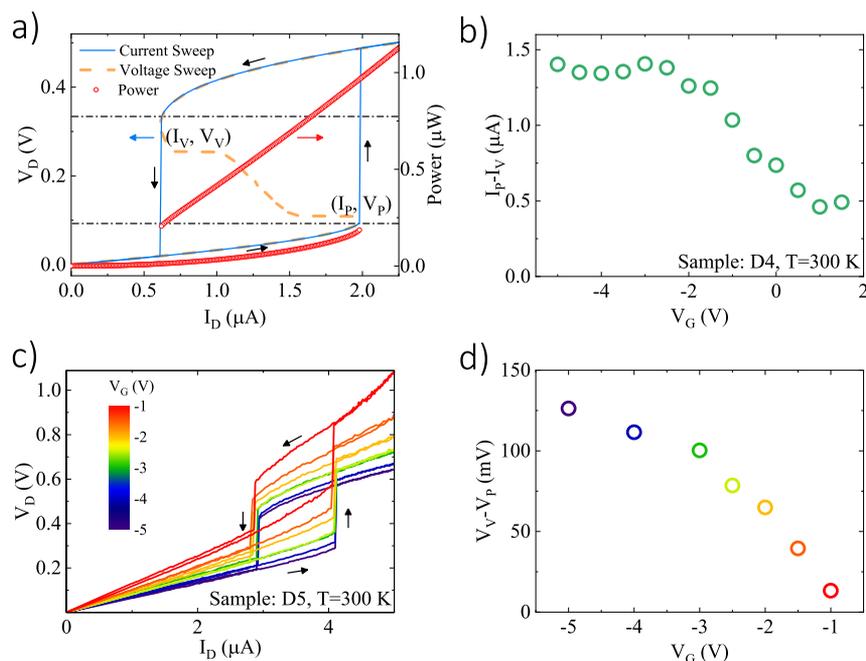
We next measure the characteristics of the tunnel diode by varying  $V_G$  at a fixed temperature.  $V_G$  modulates the device response through two different ways: (1) it changes the extent of the p-doping of the BP layer at the junction and hence modulates the tunneling rate, (2) it tunes the lateral resistance  $R_s$  of the BP channel. For a thin BP layer, both these effects are significant. The response of one such device (sample D4, less than 10 nm thick BP) at 300 K is shown in Figure 3a. Modulation of  $I_P$  and  $I_V$  with  $V_G$  is given in the left axis of Figure 3b.  $I_P$  increases with more negative  $V_G$  due to an enhancement in the p-doping of the BP layer, as illustrated using the band diagram I in Figure 3c. An increased p-doping at the tunneling interface results in a larger overlap between the filled states in the conduction band of SnSe<sub>2</sub> and the empty states of BP valence band and thus a larger  $I_P$ . Similarly, an increasingly positive  $V_G$  results in a reduced p-doping in BP as shown in Figure 3c (II and III), and hence lowers  $I_P$ .  $I_V$  being dominated by the excess current remains largely independent of  $V_G$  as expected. The modulation of the doping also affects the lateral resistance  $R_s$  of the device and causes the peak and valley to occur at a larger voltage with an increase in positive  $V_G$  (right axis of Figure 3b). A similar observation is made for the device response at 4.7 K given in Figure S4.

To decouple the effects of tunneling rate and series resistance, we measure the response from a device employing a thick ( $\sim 20$  nm) BP layer (sample D1) at 7 K, and the results are summarized in Figure 3d–f.  $I_P$  and  $I_V$  and hence the PVCRC remain independent of  $V_G$ , as shown in the left axis of Figure 3e.  $I_P$  being limited by the overlap of the available states for tunneling, its invariance with  $V_G$  suggests that the local hole density near the tunneling interface in the BP layer remains independent of  $V_G$  because of the screening.<sup>42</sup> The shift of  $V_P$  and  $V_V$  with varying  $V_G$  (right axis of Figure 3e) without any change in  $I_P$  and  $I_V$  indicates a change in the series resistance with  $V_G$ . As  $V_G$  becomes more negative, the BP channel becomes more p-doped (region I). This reduces  $R_s$  and hence the external bias required to align the junction for peak current drops, as seen in Figure 3e. On the other hand, a small positive  $V_G$  (region II) reduces the p-type doping in the BP channel and hence increases the lateral resistance, leading to an increase in  $V_P$ . This trend follows until  $V_D \approx 1.5$  V. For larger positive  $V_G$  (region III), the trend turns around and  $V_P$  starts decreasing. Because of the ambipolar nature of BP, at large positive  $V_G$ , the top gate interface of the BP channel turns electron rich, whereas a hole-rich channel near the bottom tunneling interface is retained. This leads to the formation of an electron–hole (e–h) bilayer along the vertical direction,<sup>43</sup> as schematically shown in Figure 3f. In the e–h bilayer, both the layers act as parallel channels of transport, but employing different types of carriers. The carrier can switch its nature by tunnelling across the barriers formed between  $n^+$  and  $p^+$  regions of BP. This process occurs efficiently because of the small and direct nature of the BP bandgap.<sup>44</sup> This effect reduces the lateral resistance at higher positive  $V_G$  and reduces  $V_P$ . Because of the smaller magnitude of  $I_V$ , the relative change in the potential drop across the series resistance is less at the valley position, resulting in a weaker gate modulation of  $V_V$ .

The different rates of modulation for peak and valley positions lead to a gate-dependent NDR window, the importance of which will be explained later in a memory device. This also tunes the slope of the current in the NDR region and hence results in a gate-controllable ac resistance. Such a modulation of the ac resistance is imperative in NDR-



**Figure 4.** Astable operation with intrinsic oscillations: (a) Top:  $I_D$ – $V_D$  curves from D1 at 300 K corresponding to slow (blue trace) and fast (green trace)  $V_D$  sweep exhibiting instability at the NDR region. Bottom: Power delivered to the system at each  $V_D$ . The gray shaded region indicates thermodynamic instability due to multivalued voltage for a given power delivered. (b) Schematic of measurement setup used for observing oscillations along with an equivalent circuit showing the parasitic effects limiting the high frequency operation. (c) Temporal response of the system at three different biases showing variation of duty cycle as well as frequency of oscillation. (d) Measured frequency (left axis, in blue triangle markers) and duty cycle (right axis, in orange circle markers) of oscillations as a function of biasing voltage  $V_D$ .



**Figure 5.** Bistable operation with tunable memory cell: (a) Left axis: Results from a dual current sweep (blue trace) along with a voltage sweep (orange dashed trace) as a reference. Direction of the current sweep is indicated by black arrows. A bistable window between bias of  $I_p$  and  $I_v$  allows storage of information. Upper (lower) branch corresponds to a stored value of logic '1' (logic '0'). Right axis: Power delivered (red circle markers) to the system as a function of the current forced through the system. Multivalued power for a given current bias indicates presence of metastable states separated by an energy barrier. (b) Modulation of the write window from sample D4 at 300 K with  $V_G$ , suggesting a tunable noise performance. (c) Output voltages from current sweep at  $V_G$  ranging from  $-1$  to  $-5$  V from sample D5 with thick BP at 300 K. (d) Extracted read window tunability with  $V_G$  (color mapped to  $V_G$ ) showing highly versatile memory operation.

based amplifier circuits<sup>45</sup> where the gain of the amplifier can be controlled by a gate bias.

NDR devices find widespread application in oscillator circuits, where the negative differential resistance of the device

is used to compensate the stray resistance in the tank circuit, resulting in an undamped oscillation.<sup>46,47</sup> However, the dependency on an external tank circuit to create oscillation is the limiting factor for large output power at high

frequency.<sup>48–50</sup> In the quest for intrinsic oscillator without external reactive elements, the astable nature of the NDR region is explored by measuring the output characteristics with different measurement speeds. The results of a slow (10 samples/s)  $I_D$  measurement as a function of the bias  $V_D$  for D1 is given in the top panel of Figure 4a as the blue trace. On reducing the integration time for each sample point (200 samples/s), we observe an  $I_D$  oscillating between  $I_p$  and  $I_v$  as shown by the green trace in Figure 4a. During the slow measurement, the obtained current is a time average of the fluctuating current. Outside this unstable region, the current measured with both configurations overlap each other perfectly.

The measured average power delivered to the entire system (illustrated in bottom panel of Figure 4a) also shows N-shape characteristics, pointing to the thermodynamic instability in the NDR regime. This results in the multivalued nature of the voltage output for a given power delivered. The interplay between the positive feedback in the unstable regime and the restoring force by the fixed external voltage bias leads to the observed oscillation. Note that the absence of such thermodynamic instability in a device with 2L-WS<sub>2</sub> as the barrier rules out the possibility of sustained oscillation even though it exhibits a comparable PVCR (see Figure S5).

We now bias the tunnel diode at a fixed  $V_D$  in the NDR region and measure the oscillating voltage across the diode using a digital storage oscilloscope as shown in Figure 4b.<sup>32</sup> The nonzero cabling and setup resistance  $R_w$  from the tunnel diode to the SMU allows the voltage across the diode to fluctuate and show up across the oscilloscope probe. The measured temporal response at three different  $V_D$  values is shown in Figure 4c, indicating stable and persistent oscillation. Such an astable operation helps in realizing single element oscillator where the need for integrating reactive elements on chip can be avoided. Proximity of the biasing point to either of peak or valley modulates the duration for which the circuit latches near that particular state, modulating the duty cycle and frequency of oscillation, as shown in Figure 4d. This can be seen as slower initial rise for a bias of  $V_D = 0.110$  V and a slow initial fall for  $V_D = 0.255$  V (bottom and top panels in Figure 4c). The system reaches a maximum frequency when biased in the middle of the NDR region as the restoring forces are maximum. The tuning of the oscillation frequency by the applied bias is shown in Video S1. Note that the large stray capacitance of the cable and the probe station ( $\sim 75$  pF) limits the observed frequency of oscillation, whereas the intrinsic frequency is much higher. A reduction in the stray capacitance in the circuit coupled with an enhancement in the peak current density would help to attain a higher frequency. These oscillations are stable over long duration as observed from different measurements (different panels in Figure S6) and survive at low temperature as well, as shown in Figure S7.

We now investigate the possibility of obtaining a bistable operation from the tunnel diode for random access memory (RAM) applications. This is achieved by forcing  $I_D$  across the tunnel diode terminals and measuring the voltage drop across it, as shown in the left axis of Figure 5a (in blue trace). The forward and reverse sweeps are indicated by the black arrows. The result from a voltage sweep is also shown as dashed orange trace for reference. When the forcing current is increased beyond  $I_p$ , the voltage across the diode jumps to the positive differential resistance branch beyond the valley point. After this jump, when the current bias is reduced, the voltage does not

trace back in the same path, rather remains in the positive resistance branch until a current bias value of  $I_v$ . When current bias is reduced below  $I_v$ , the voltage abruptly drops to the other positive differential resistance branch below the peak point. Hence the output voltage is multivalued for a given range of current bias, and its value depends on the history of the device. This gives the device the ability to store information equivalent of one bit encoded in the voltage across it. The stored value of the junction can be altered by forcing positive or negative current spikes that ride on the biasing current. To retrieve the stored bit value, just monitoring the voltage across the device is sufficient, cutting down the extra elements required in conventional memories. A voltage value above  $V_v$  and below  $V_p$  corresponds to a stored value of logic '1' and logic '0', respectively (Figure 5a).

The thermodynamic origin of the bistable states can be understood from extracting the power delivered to the circuit at each current bias, as shown by the red circles in the right axis of Figure 5a. In between  $I_p$  and  $I_v$ , at a given current bias, there are two metastable states of the system separated by an energy barrier. This is in stark contrast with the previously discussed astable oscillation at a given voltage bias. It is striking that by changing the constraint (voltage or current bias), the thermodynamic stability of the system can be effectively tuned between astability to bistability.

The logic state stored in the memory cell should be less susceptible to external noise sources and the read operation should be able to distinguish the state of the system with confidence. Thus, the threshold for switching between logics '0' and '1' is an important metric. The separation  $I_p - I_v$  corresponds to the maximum allowed peak to peak fluctuation, and determines the stored bit retention. For device D4 with thin BP,  $I_p$  being strongly dependent on  $V_G$ , results in a gate tunable  $I_p - I_v$  as shown in Figure 5b. A negative gate bias is able to enhance the range by  $\sim 180\%$  making the memory cell more immune to external noise. On the other hand, the separation  $V_v - V_p$  indicates the stability against noise during the read operation. Our ability to modulate the series resistance using  $V_G$  allows this separation to be effectively tuned, as shown in Figure 5c, d for device D5 with a thick BP channel. The tunable noise margins thus obtained has a trade off with the operating frequency as well as both the standby and dynamic power consumption. This can be used in designing an intelligent memory architecture that dynamically decides the noise margin providing optimum speed and power consumption.

The proposed memory cell with a junction area of  $400 \text{ nm}^2$  is expected to exhibit a standby power of  $0.33 \text{ pW}$  ( $3.13 \text{ pW}$ ) when retaining logic '0' (logic '1'), which is significantly less compared with the state of the art Intel 22 nm HDC Tri-gate LP SRAM cell ( $\sim 40 \text{ pW}$ ).<sup>51</sup> On the other hand, the single element and vertical design of the heterojunction memory allows us to reduce the footprint per cell dramatically, providing about 100 times higher packing density. The additional possibility of stacking multiple heterojunctions vertically using 3D integration brings about a great density advantage compared to the state of the art SRAM. This is promising for next-generation architectures like memory-intensive computing and bioinspired computing.

## CONCLUSION

In conclusion, we report a broken gap van der Waals heterojunction-based tunnel diode exhibiting clean, repeatable,

and gate-tunable negative differential resistance characteristics with a high peak-to-valley current ratio over a large temperature range. By altering the constraint from constant voltage to constant current bias, the thermodynamic stability of the tunnel diode circuit is tuned from astability to bistability. This allows us to demonstrate multifunctional operations like a reactive-element-less on chip, compact voltage-controlled oscillator, and a highly scalable, single-element random access memory cell for ultradense memory applications. The operations are sustained at very low temperature, making them attractive for cryogenic electronics as well.

## METHODS

**Fabrication.** Au lines are defined by optical lithography using a 360 nm UV source and AZS214E resist spin-coated on an Si/SiO<sub>2</sub> substrate with 285 nm thick oxide formed by dry chlorinated thermal oxidation and forming gas annealing. A 20 nm thick Ni film followed by a 40 nm thick Au film is deposited via DC magnetron sputtering and lifted off by acetone/iso-propyl alcohol rinse to form the bottom contact. The SnSe<sub>2</sub> flakes are exfoliated from bulk crystals using Scotch tape and are subsequently transferred to a poly dimethyl-siloxane (PDMS) sheet. Flakes of thickness ~50 nm are identified by optical contrast and transferred onto the Au line forming source contact using a dry transfer technique. This process is performed underneath a microscope using controlled translation and rotation for desired positioning of the flakes with respect to the prepatterned substrate. This process is repeated for monolayer WS<sub>2</sub>. The SnSe<sub>2</sub>/WS<sub>2</sub> stack is annealed at 70 °C for 2 min in ambient for devices D1, D2, D4, and D6. BP of thickness ~20 nm is transferred next, contacting another Au line forming drain contact. The stack is immediately encapsulated with hBN following the BP transfer. For devices D3 and D5, the stack is annealed after hBN transfer. Few-layer graphene is transferred to form the gate contact. The layers in the whole device fabrication process do not undergo any chemical treatment and hence maintain their pristine quality and clean interfaces.

**Characterization.** The devices are loaded into a closed cycle He probe station Lakeshore CRX-6.5K or are wire bonded to a closed cycle He cryostat and characterized using a Keithley 4200A SCS parameter analyzer for DC measurements and a Tektronix MDO3000 digital storage oscilloscope for frequency measurements. All the measurements were done in vacuum with a pressure <1 × 10<sup>-4</sup> Torr.

## ASSOCIATED CONTENT

### Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsnano.0c06630>.

Raman characterization of flakes; fabrication steps; summary of results from multiple devices and different barrier layers; gate dependence of output characteristics of sample D4 at 4.7 K; absence of oscillation for heterostructure with thick barrier layer; persistence and stability of oscillations; astable operation at 7 K (PDF) Video S1 showing modulation of oscillation frequency as a function of bias voltage (oscillations are observed when the bias  $V_D$  enters the NDR region for both sweep directions and gets modulated with magnitude of  $V_D$ ; signal observed on the oscilloscope is the inverted version of the original signal) (MP4)

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## Notes

The authors declare no competing financial interest.

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