

Characterization system for Large Area Electronic Systems

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Abstract— Large area electronic systems use either an active or passive matrix sensory back plane as the major component in the system design. These backplanes are vulnerable to interconnection errors and poor device performances. Hence reliability studies pertaining to the systems of these order are relevant. In this paper we discuss the development of a sensor array characterization system which can not only detect interconnect faults, but also characterize the access switches in the array. Switched capacitor circuits based on n channel MOSFETs and RC networks are used for demonstrating the utility of the system in active addressing and passive addressing schemes respectively. In Switched capacitor circuit based backplane, an approximate transfer characteristics is obtained by measuring the time averaged current through the MOSFET in response to an applied gate voltage, while time constant estimation is done for characterizing the RC networks.

Keywords— Active matrix, passive matrix, testing, characterization

I. INTRODUCTION

An array of sensory elements are found to be the backbone of many commonly found large area systems [1]–[10]. The sensory array of elements in fact can be either arranged in passive matrix format without any access devices or with an active matrix format with three terminal active device elements for accessing the sensor units [11]–[13]. For example a passive image sensor array comprising of photo conductor sensors is shown in Fig. 1. Here one of the row lines is sequentially addressed with a fixed voltage and the gathered information is read through the column lines. Information gathered by the sensors are thereby transferred to the periphery of the array through the column lines. On the other hand, access elements in the active matrix are given appropriate control voltages during the write and read operations to gather the information as shown in Fig. 2. Sensory backplane found in many large area systems are prone to several faults[9]. It can be due to the interconnection related short and open faults. Open faults can make the sensory data inaccessible while the short condition can cause the flow of larger loop currents. Moreover faults attributed to the variation in the electrical parameters of the access elements also cause reliability issues pertaining to the operation of these large area systems [3]. It is generally beneficial in to detect faults in these sensory back planes before deploying the entire system in field operation.

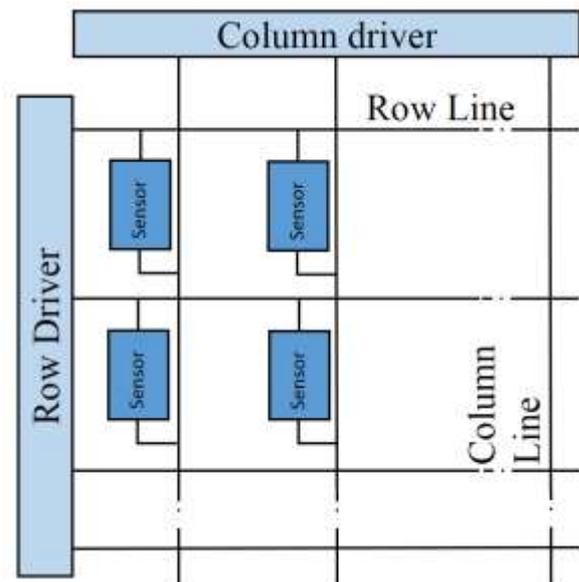


Fig. 1. Architecture of passive matrix sensor backplane.

In this paper we propose an automated system that not only identifies interconnect related faults but also enables the characterization of the access devices present in the back plane. Capacitive sensor elements are commonly found in large area pressure sensing and thermal imaging circuits [14]–[15] with an active access element incorporation. Here we use a switched capacitor architecture shown in Fig. 3, that consists of a MOSFET switch in series with a storage capacitor, C_S as the platform to demonstrate the utility of the system in estimating the characteristics of access devices. It is to be noted that the capacitor itself can also act as a sensor.

The proposed characterization system incorporates a technique in which the array points are addressed first write voltage into the storage capacitor while the MOSFET is addressed by a fixed gate bias and then read the already written voltage out with the MOSFET at a variable gate bias. A time averaged current is estimated from the measurement of the charge transferred from the array capacitor to an integration capacitor used in the charge sensing circuit. The time averaging along with double sampling is expected to remove measurement related noise significantly. An RC network

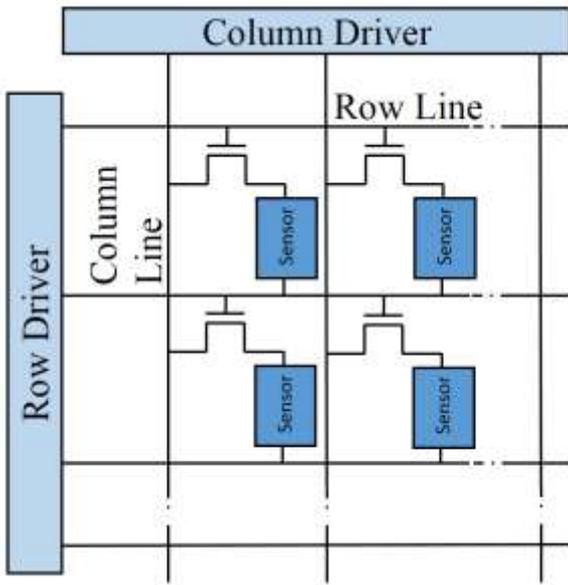


Fig. 2. Architecture of active matrix sensor backplane.

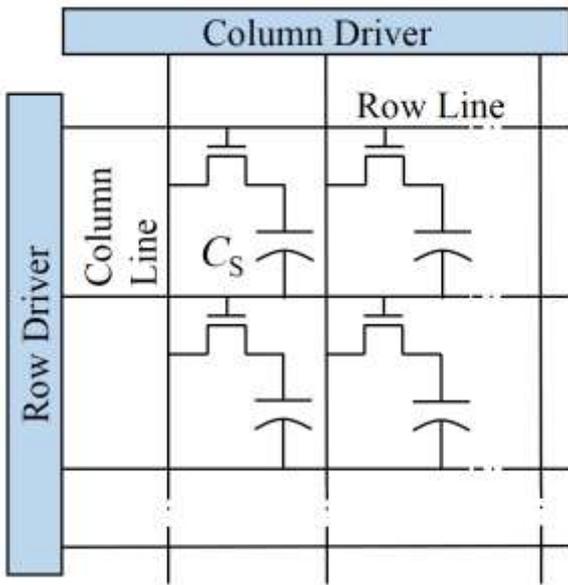


Fig. 3. Switched capacitor structure.

platform is also tested with the system to show its application in passive matrix sensory backplane.

II. DESIGN OF THE SYSTEM

A. Test Algorithm

This back plane testing scheme employs multiple sequences of write and read events to extract the characteristics of the access MOSFET switch. Block diagram and the operational schemes are shown in Fig. 4. An approximate transfer characteristics is obtained by measuring the time averaged current through the MOSFET with an increasing sequences of gate voltage used during the read phase of operation.

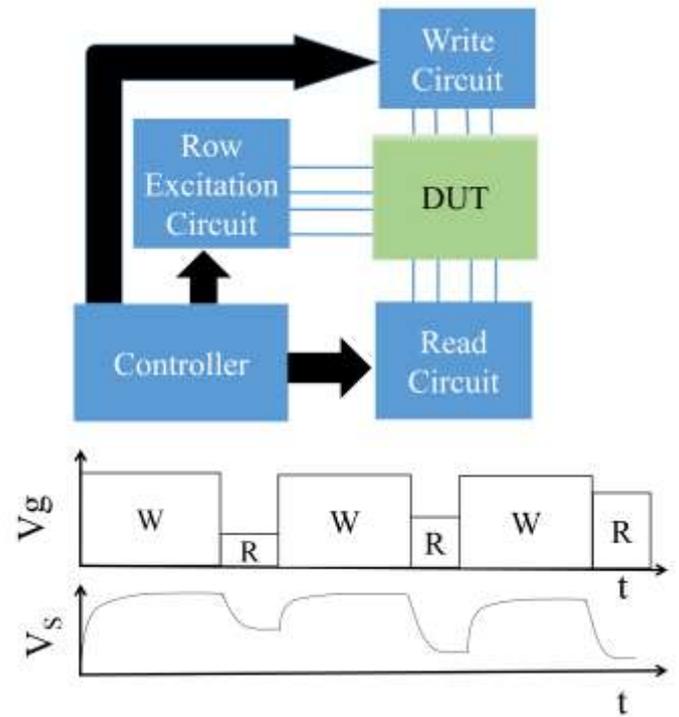


Fig. 4. System Block Diagram and Operational steps for switched capacitor circuit with Gate line voltage (V_g) and Voltage across Capacitor (V_s).

During the Write operation, the storage capacitor is charged to a fixed drain voltage V_d with the MOSFET in linear region. The gate voltage V_g to turn the MOSFET on and the value of V_d are maintained at constant values for all write operations. After the Write operations, an electrical isolation is momentarily done between the addressed pixel and the write circuit (small leakage current error is expected). And the Read operation is done by reading out the charge on storage capacitor using a trans-impedance amplifier at a gate signal V_{g1} applied to the MOSFET switch. Charge measured is used to obtain the average current I_{Avg1} through the MOSFET. After the first Read operation, a second write operation is performed to make the storage capacitor again charged to V_d . Subsequently a second Read operation is performed with a gate signal V_{g2} , where $V_{g2} = V_{g1} + \delta V_g$ and the average current I_{Avg2} is also obtained. The sequence of Write Read operations are continued until a read operation is performed with gate signal V_{gn} (the largest gate read voltage) and the corresponding average current I_{Avgn} is noted.

A measurement of n time averaged current data values ($I_{Avg1}, I_{Avg2}, \dots, I_{Avgn}$) corresponding to a sequence of n applied gate voltages ($V_{g1}, V_{g2}, \dots, V_{gn}$) is recorded. This represents an equivalent measure of the transfer characteristics of the access transistor. An equally spaced increasing sequence of V_{g1} , is obtained by keeping $\delta V_g = (V_{gn} - V_{g1} + 1) / n$. It is to be noted that the data obtained here is not the exact transfer characteristics of the MOSFET since the current recorded is not an instantaneous value at a fixed drain voltage, but an average value (averaged over a read interval, T_r) with a time varying drain voltage due to the discharge of the storage capacitor.

Nevertheless this characteristics can be used to extract the percentage variation in device performance across the array.

B. Design and Working

Characterization system outlined in Fig. 4 is designed as shown in Fig. 5. The four major sub modules are Write circuit, Row excitation circuit, Read circuit and the Controller.

The Write circuit is used to issue a constant voltage to the column lines of the backplane. In the case of switched capacitor array, the storage capacitor gets charged up to this voltage value V_d . A low leakage column switch array is used to select the column lines. The Row Excitation circuit is used to apply, fixed or variable voltages to the row lines in the sensor backplane. In the case of active matrix approach, the row signals are used to excite the control inputs of the access devices present in it. For example, in the switched capacitor structure, the gate lines of the MOSFET are given fixed gate voltages during write and variable gate sequences during read. Row signals are issued to the backplane via row select switch (ADG 5434). The control of the switch was done with a shift register. A bidirectional Digital to Analog Convertor(DAC)

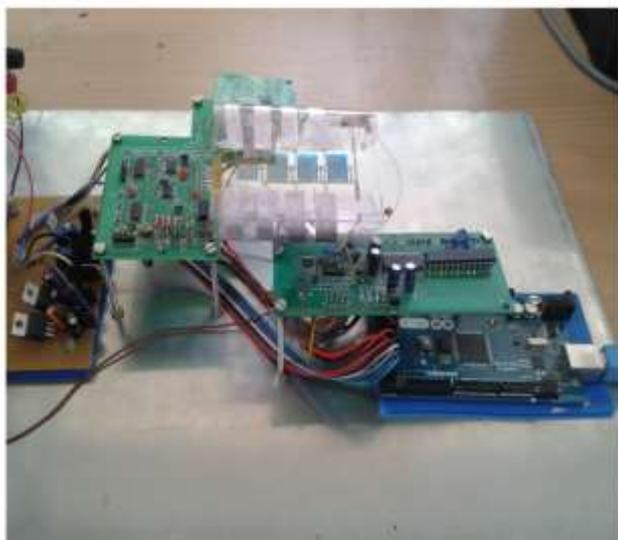
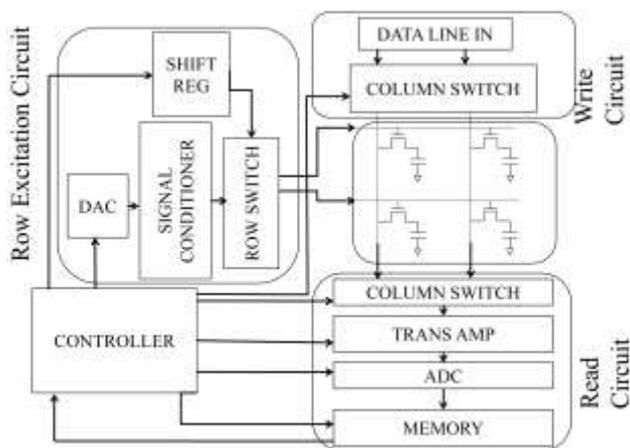


Fig. 5. Characterization system.

operating between +18V to -18V was used to generate the row signals. The bi-polar row signals enables the characterization system to test both n and p type switches.

Fig. 6 portrays the Read operation. The Write Circuit is kept disconnected during the Read operation. And the column line addressed is connected to the Read circuit. In the Read circuit, input current was measured precisely using a trans impedance amplifier(IVC 102) with a gain equal to T_{int} / C_{int} , where T_{int} is the integration interval and C_{int} is the feedback capacitor. In the active matrix platform, the row excitation voltage, which happens to be the gate voltage V_g in the switched capacitor circuit is set to the appropriate read voltage value(where $V_{g1} \leq V_g \leq V_{gn}$). During the read operation, the storage capacitor is allowed to discharge through the switch and the discharge current is used to charge C_{int} . The amplifier operation is controlled by switches S1 and S2. The integration operation of the charge draining out of the storage capacitor is commenced by closing S1. The charge integrated on the charge amplifier is due to the current through the MOSFET switch being addressed as well as the leakage current. This leakage current, i_{leak} , is due to leakage from all the unaddressed array points along the same column as well as leakage from the write circuit. For an applied gate voltage, V_g , if $i(t)$ is the instantaneous current through the MOSFET, then

$$V_{out} = -\frac{1}{C_{int}} \int_0^{T_r} (i(t) + i_{leak}(t)) dt \quad (1)$$

where T_r is the integration interval. The voltage obtained at the output of the charge amplifier is digitized with a 12 bit Analog to Digital Converter (ADC). The data output from the ADC is stored intermittently in a memory element before transferring to computer. Switch S2 is kept open during integration and is closed to reset C_{int} after the read operation. The output of the amplifier is measured twice, one before closing S1 (V_{out1}) and second (V_{out2}) after the read time T_r . The difference between these values are used to obtain the average current. With a known value of C_{int} and T_r , the average current for a gate

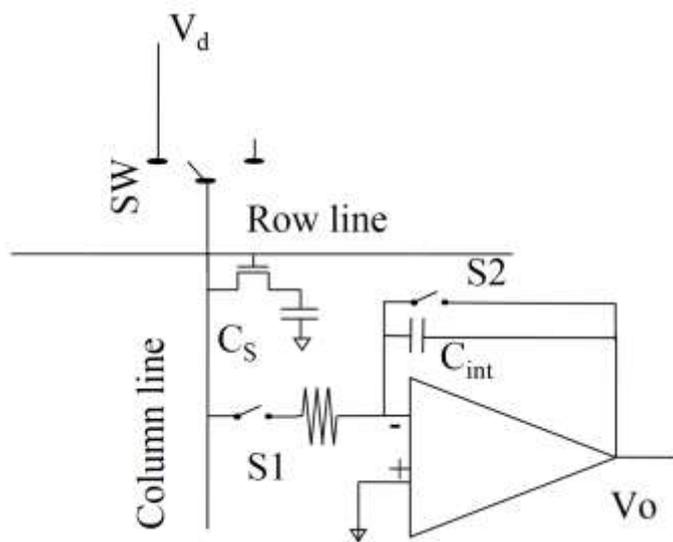


Fig. 6. Read Operation

excitation can be calculated using (2), where $V_{Rout} = V_{out2} - V_{out1}$. These current values so obtained are used to characterise the switches in the array.

$$I_{Avg} = -C_{int}V_{Rout} / T_r \quad (2)$$

Low dropout regulators were used in the power supply. Digital ICs and ADC were operated at +5V, while the analog switches and signal conditioning circuits employed $\pm 18V$. Digital and analog ground were interconnected and shorted to the common supply ground. An overall power consumption of 1.5W was estimated for the operation.

III. EXPERIMENTS

A. Active Matrix Array characterization

For experiments, a 4 by 4 array of switched capacitor circuit shown in Fig. 7a, using n channel MOSFET ALD1116 was fabricated. Open line fault conditions in the second column and third row were introduced along with a point fault (open)

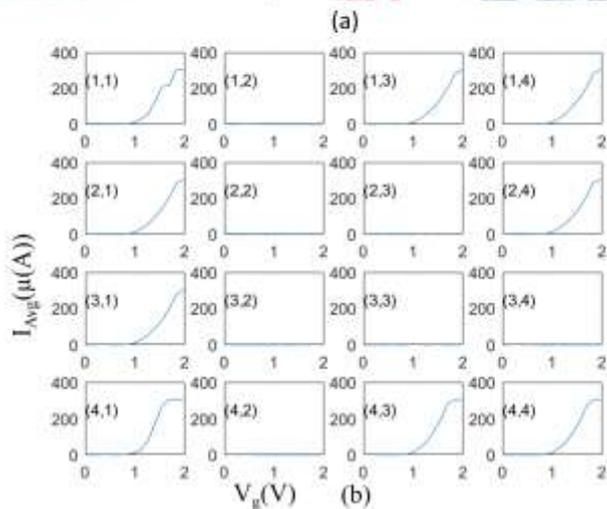


Fig. 7 (a). Switched capacitor array. (b). I_{Avg} versus V_g plots.

corresponding to pixel (2,3). A plot of time averaged current versus gate voltage was obtained by sweeping the gate voltage from 0 to 2 V. The I_{Avg} versus V_g plots of the access switches across the array were obtained as shown in the Fig. 7b. The current measured can be seen to be one order less than the actual current specified in the data sheet of the device. This is because the current measurement done with the system, is an average measurement with an exponentially decaying potential applied to the drain terminal of the device during the read interval. The faulty interconnects caused the column 2 and pixels (2,3), (3,3) and (3,4) inaccessible. A fault map showing good and bad array points can be found with relatively less number of write read operations. These fault map can serve as direct indication of the interconnect faults seen in an array. The predefined open faults in the switched capacitor array, identified by the system is shown as a fault map in Fig. 8, with dark patches denoting faulty array points and grey patches showing good points.

B. Passive Matrix Array characterization

For these experiments RC circuits were designed, so that the proposed system can be used to estimate the Time Constant (TC) of the RC circuits shown in Fig. 9. RC circuits with known TC values are connected to the system without any access switches are charged for approximately five times their TC using the column lines by keeping row select voltage at



Fig. 8. Fault map in matrix due to line and point interconnect faults (Black shade shows faulty points).

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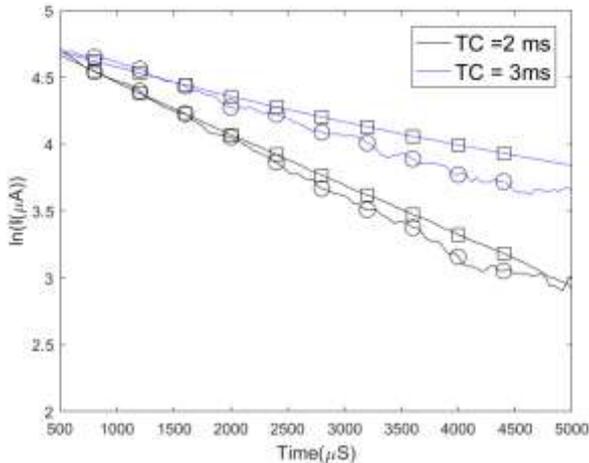


Fig. 9. RC characterization of Passive matrix circuit.

ground. The charge retained by the capacitor was allowed to discharge through the read circuit during the read phase of operation. The discharge current was sampled at regular intervals up to five times TC to record the discharge profile of the RC circuit. The results obtained with the developed system is compared with the values obtained using Cathode Ray Oscilloscope (CRO). The curves with square markers denote the plot obtained using the developed system, while the plots with circular markers correspond to readings observed with CRO. It can be seen that the proposed system is able to extract the TC reliably.

IV. CONCLUSION

The paper discussed the development of a system that can be used to characterize a sensor backplane in a large area electronics system. The proposed characterization system was tested with switched capacitor circuits and RC networks for proof of concept. The design described in this paper supports the measurement from one pixel at a time due to the use of one trans impedance amplifier for all the pixels. This implies total measurement time have a linear dependency with number of pixels. On the other hand multiple channel for readout can significantly reduce the delay. Secondly, the system should be calibrated against the leakage currents for precise characterization

In conclusion, the developed system can be utilized for reliability studies in sensor array backplanes of either active or passive addressing schemes. The system can generate a fault map corresponding to interconnect faults as well as a characterization map of the access switches.

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