A Self-Biased High Performance Folded Cascode CMOS Op-Amp

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Abstract

Cascode CMOS op-amps use a large number of external bias voltages. This results in numerous drawbacks, namely, an area and power overhead, susceptiblity of the bias lines to noise and cross-talk and high sensitivity of the bias point to process variations. In this paper we present a self-biasing technique for folded cascode CMOS op-amps that uses no additional devices and no bias voltages other than the two supply rails. The resulting self-biased op-amps are free from the above mentioned drawbacks and exhibit the same performance as existing folded casode op-amps, except for a small reduction in slew rate. This is achieved by following transistor sizing constraints derived through detailed circuit analysis. The technique is applied to an existing high performance op-amp. Simulation results show that the high performance is maintained while nine bias voltages are eliminated.

1. Introduction

In a wide variety of applications such as A/D converters [1] and switched-capacitor filters [2], speed and accuracy are determined by the settling behavior of the op-amps. The settling speed depends on the unity gain frequency and a single pole settling behavior whereas high settling accuracy requires high d.c. gain of the op-amps.

Folded cascode op-amps have the important property of single pole settling behavior with a large unity gain frequency. But a simple folded cascode op-amp fails to provide high gain which is required for high settling accuracy. To overcome this limitation, the gain boosting technique introduced by Hosticka [3] has been applied for a folded cascode op-amp [4]. But a major drawback of this gain boosted op-amp is that it needs a number of external bias voltages [5].

In an analog circuit different active devices should be properly biased to get high performance. For instance, most of the transistors in a CMOS op-amp should be biased in the saturation region of operation. Usually a separate bias circuit is used to bias the transistors in an op-amp. The main disadvantage of using a separate bias circuit is that it requires long wires for broadcasting the bias voltages from the bias circuit to the main op-amp circuit. These wires not only consume a considerable amount of area but, what is worse, are also susceptible to noise and cross talk. As has been observed in [5], the requirement of a large number of bias voltages may limit the use of gain boosted folded cascode op-amps.

There have been some efforts to overcome this biasing problem of op-amps. In [6] self-biased CMOS op-amps are proposed. But some of the transistors in these self-biased op-amps are biased in the linear region of operation which causes drastic reduction of some important a.c. performances, like gain, CMRR and PSRR. In [7] a self-biased transistor like circuit block, called super MOS transistor, is introduced. This super MOS transistor can be used to construct a folded cascode op-amp to get very high performance. But each one of the super MOS circuit blocks consists of as many as 12 transistors.

We propose a CMOS op-amp self-biasing technique which, without any extra devices, keeps all the transistors in the saturation region of operation. This self-biasing technique is used to bias a very high performance folded cascode op-amp which has 100 dB gain and 100 MHz unity gain frequency. The self-biased op-amp requires only the two supply rails, V_{dd} and V_{ss}. Thus, the area and power overhead of biasing is eliminated. Further, the operating point is less sensitive to process variations, since in this approach the bias point is determined by size ratios only. While self-biasing has a number of performance advantages, the cost is a small sacrifice in slew rate. This slew rate reduction is

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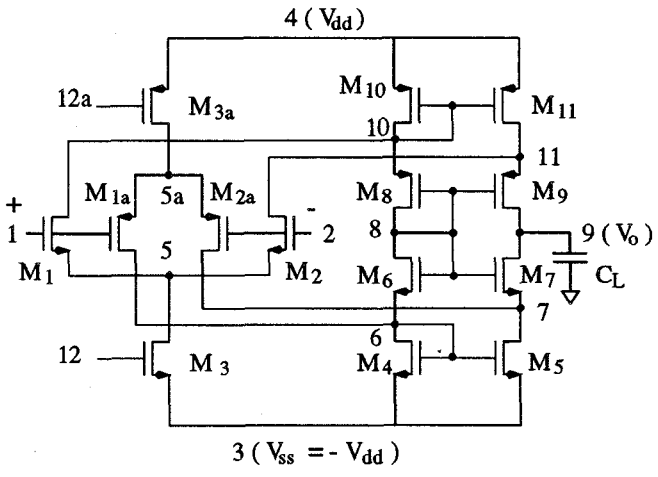

Figure 1. Externally biased folded cascode op-amp

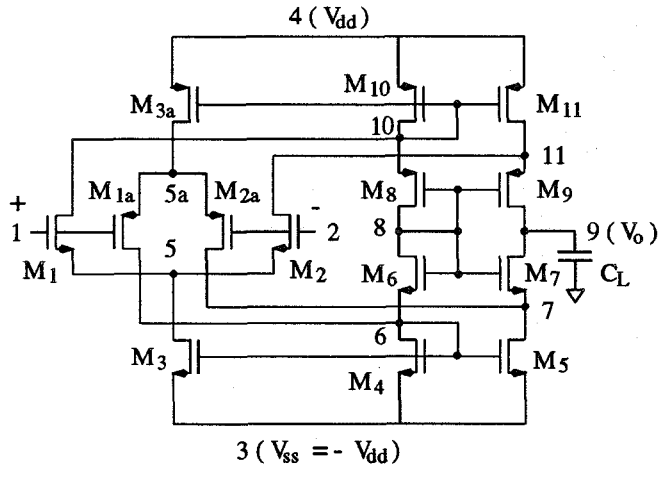

Figure 2. Self-biased folded cascode op-amp

analytically predicted and minimized.

The paper is organized as follows. Section 2 deals with a self-biased fully complementary folded cascode op-amp. In the same section we present the design analysis of the op-amp and we compare the performance of the op-amp with an externally biased op-amp. The analysis that is provided is used to pick the transistor sizes so that all devices are biased in saturation and the slew rate is high. Section 3 discusses the self-biasing of a very high performance op-amp. Simulation results are given in Section 4. Section 5 summarizes the work.

2. Self-Biasing of Folded Cascode Op-Amps

In this section we describe the self-biasing technique by applying it to the fully complementary folded cascode op-amp shown in Fig. 1 [8]. However, the technique can be applied to any folded cascode op-amp.

The op-amp circuit shown in Fig. 1 has large common mode range, high slew rate and, with appropriate transistor sizes, symmetric transient response for rising and falling inputs. In this circuit, the two tail current source transistors M_3 and M_{3a} are externally biased. However, these two transistors can be biased by using the internal current source formed by the transistors M_4, M_6, M_8 and M_{10}. In particular, nodes 6 and 10 can provide the gate bias of M_3 and M_{3a} respectively. The resulting self-biased op-amp circuit is shown in Fig. 2.

In the self-biased op-amp the gate biases of the transistors M_3 and M_{3a} form two feedback paths. But because of the diode connected transistors M_4 and M_{10} the two nodes 6 and 10 are a.c. attenuated. So effectively no signal comes through the feedback paths. Hence, at a given design and bias point, except the transient response, all other performances of the externally biased and the self-biased op-amps are the same.

Apart from the transient response the other difference between the externally biased and the self-biased op-amp is the difference in the design technique needed to keep the transistors M_3 and M_{3a} in saturation. In the following subsection first, we find the potential design variables and then we give a design guideline to keep all the transistors in the op-amps in saturation. In the subsequent subsection we compare the step response of the two op-amps.

2.1. Design Analysis

We take L and β ($=k'W/L$) of the transistors as primary design variables. The quiescent current through a transistor M_i is denoted by I_{Di}. As is typical with op-amps, all of the primary variables are not independent variables. There are a number of matched

pair transistors in the op amps. They are the following: M_1, M_2; M_{1a}, M_{2a}; M_4, M_5; M_6, M_7; M_8, M_9 and M_{10}, M_{11}. Note that, any two matched devices have the same quiescent current.

The fully complementary op-amps have a large common mode range. Over some portion of the common mode range only the input transistors M_1 and M_2 are active, while over some other portion only M_{1a} and M_{2a} are active. So to get uniform performance over the common mode range and to get symmetric step response for rising and falling inputs, the following equalities are taken:

$$\beta_{1a} = \beta_1, \beta_8 = \beta_6, \beta_{10} = \beta_4 \quad (1)$$

$$L_{1a} = L_1, L_8 = L_6, L_{10} = L_4 \quad (2)$$

$$\text{and } I_{D3a} = I_{D3} \quad (3)$$

The total quiescent current drawn by the op-amp is $I_{D3a} + 2I_{D10} = I_{D3} + 2I_{D4}$. So the equality (3) can be satisfied by taking,

$$\frac{I_{D3a}}{I_{D10}} = \frac{I_{D3}}{I_{D4}} = q \text{ (say)}. \quad (4)$$

Note that, this equality also gives

$$I_{D10} = I_{D4}. \quad (5)$$

In the self-biased op-amp the current ratio I_{D3}/I_{D4} can be controlled by the size ratio of the transistors M_3 and M_4. Hence, we impose the following constraints:

$$L_{3a} = L_{10}, L_3 = L_4 \quad (6)$$

$$\text{and, } \frac{\beta_{3a}}{\beta_{10}} = \frac{\beta_3}{\beta_4} = q \quad (7)$$

From the equalities (1) (2), (6) and (7) we are left with L_1, β_1, L_4, β_4, L_6, β_6 and q as the design variables.

Based on the matching information of the transistors and from KCL,

$$I_{D4} = I_{D6} + I_{D3}/2 \quad (8)$$

It therefore follows that $I_{D4} > I_{D3}/2$. Hence, from (4) the range of q is (0,2).

To get high performance all of the transistors in the op-amp should be in saturation. Because of the diode connection of the transistors M_4, M_6, M_8 and M_{10} all of the transistors M_4–M_{11} are always in saturation. In quiescent condition the node voltages V_8 and V_9 are close to zero. So the node voltages V_6 and V_7 are negative (since the transistors M_6 and M_7 are in saturation). Hence, the transistors M_{1a} and M_{2a} are in saturation. Similarly, the two transistors M_1 and M_2 are also in saturation.

In the externally biased op-amp the gate voltages of the transistors M_3 and M_{3a} can be easily chosen to bias them in saturation. However, in the self-biased op-amp the gate voltages of the two transistors depend on the sizes of the other transistors. In the self-biased op-amp, the design constraint,

$$\frac{\beta_6}{\beta_1} \leq \frac{2}{q} - 1 \quad (9)$$

keeps the two transistors in saturation. This inequality can be obtained by first expressing the gate and the drain voltages of the two transistors in terms of different transistor sizes. Then, the node voltage inequalities for keeping the transistors in saturation are imposed, resulting in the inequality (9).

2.2. Performance Comparison

As previously mentioned, for performance comparison we need only to compare the slew rate of the self-biased op-amp with that of the externally biased op-amp. The slew rate is determined by the load current which charges or discharges the load capacitor. This transient load current can be increased at the cost of the total quiescent current drawn (hence, power dissipation). So to compare the performance of the two op-amps we have taken the ratio of the transient load current and the total quiescent current as the performance metric.

It is important to note that the fully complementary op-amps have symmetric transient response for rising and falling inputs. So for our comparison we consider only the positive step response. Besides facilitating a comparison of the op-amps, the analysis also provides the value of the parameter q at which the slew rate is maximized.

The transient load current for both of the op-amps is,

$$i_o = i_{D3} + min\{i_{D6}, i_{D3a}\} \quad (10)$$

where i_{Dj} denotes the transient current through the transistor M_j. For the externally biased op-amp the transient load current can be well approximated by,

$$i_{o1} = [1 + min\{1, (1/q - 0.5)\}] I_{D3} \quad (11)$$

while for the self-biased op-amp the transient load current is,

$$i_{o2} = 4[1 + \min\{1/q, (1+q)\}] \times \left[\frac{1 + \sqrt{(1 - q/2)\theta}}{1 + 2\sqrt{\theta} + \sqrt{1+q}}\right]^2 I_{D3} \quad (12)$$

where $\theta = \beta_4/\beta_6$.

Now the total quiescent current drawn by the main op-amp circuit is,

$$\begin{aligned} I_{tot} &= I_{D3} + 2I_{D4} \\ &= \left(\frac{2+q}{q}\right) I_{D3} \end{aligned} \quad (13)$$

From equations (11) and (13) the ratio of the transient load current of the externally biased op-amp and its total quiescent current is,

$$\frac{i_{o1}}{I_{tot}} = [1 + min\{1, (1/q - 0.5)\}] \frac{q}{(2+q)} \quad (14)$$

From equations (12) and (13) we get the ratio metric for the self-biased op-amp as,

$$\begin{aligned} \frac{i_{o2}}{I_{tot}} &= [1 + \min\{1/q, (1+q)\}] \frac{4q}{(2+q)} \\ &\times \left[\frac{1 + \sqrt{(1 - q/2)\theta}}{1 + 2\sqrt{\theta} + \sqrt{1+q}}\right]^2 \end{aligned} \quad (15)$$

The ratio metric i_{o2}/I_{tot} is maximum at $q = 0.618$. This maximizer can be obtained by equating the two parts of the *min* function in (15). The maximum value of the ratio metric is quite insensitive to θ. On the other hand, the ratio metric i_{o1}/I_{tot} reaches its maximum value of 0.5 at $q = 2/3$. For larger values of q the ratio metric remain the same. So for simulation comparison (given is Section 4) we took $q = 2/3$. With this value of q and with $\theta = 1$ the value of i_{o2}/I_{tot} is 0.45. In other words, with equal power dissipation (in the main op-amp) the self-biased op-amp has 10% less slew rate than that of the externally biased op-amp. This analytical prediction is well matched by simulation results as is shown in Section 4. Further, when the current in the bias circuit of the externally biased op-amp is also accounted for, simulation measurements show that the performance metric is actually 12% better for the self-biased op-amp.

3. Self-Biasing of High Performance Op-Amp

In this section we describe a self-biased folded cascode op-amp which has both high d.c. gain and high unity gain frequency. The self-biased folded cascode op-amp discussed in the last section has high unity gain frequency. To enhance its gain, the gain boosting technique given in [4] can be applied to this op-amp. The gain boosting technique is shown in Fig. 3. The gain of the simple amplifier can be increased by the additional

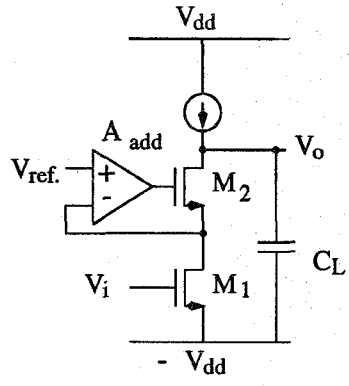

Figure 3. Gain boosted cascode amplifier stage

amplifier circuit A_{add} by increasing the cascoding effect of the transistor M_2.

Fig. 4 shows the gain boosted self-biased fully complementary folded cascode op-amp. Because of the full complementarity, this op-amp has rail to rail common mode range. It also has rail to rail minus two threshold voltage of output swing. The gain boosting amplifiers, A_1 and A_2 are shown in Fig. 5. Note that the two non-complementary boosting amplifiers are also self-biased.

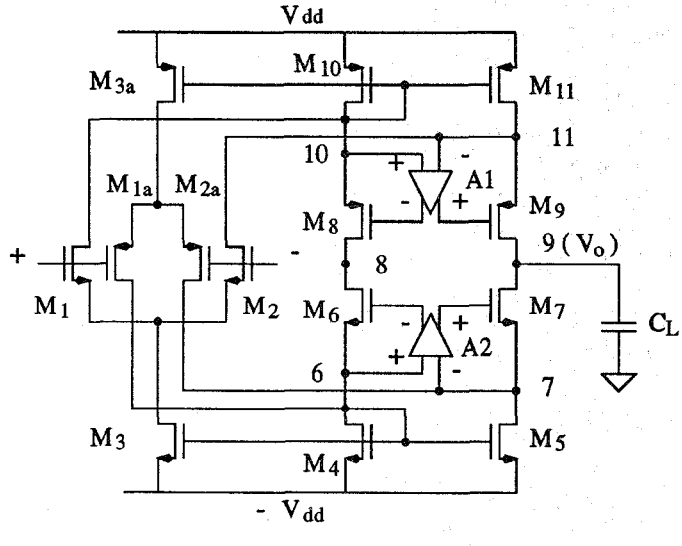

Figure 4. Gain boosted self-biased fully complementary folded cascode op-amp

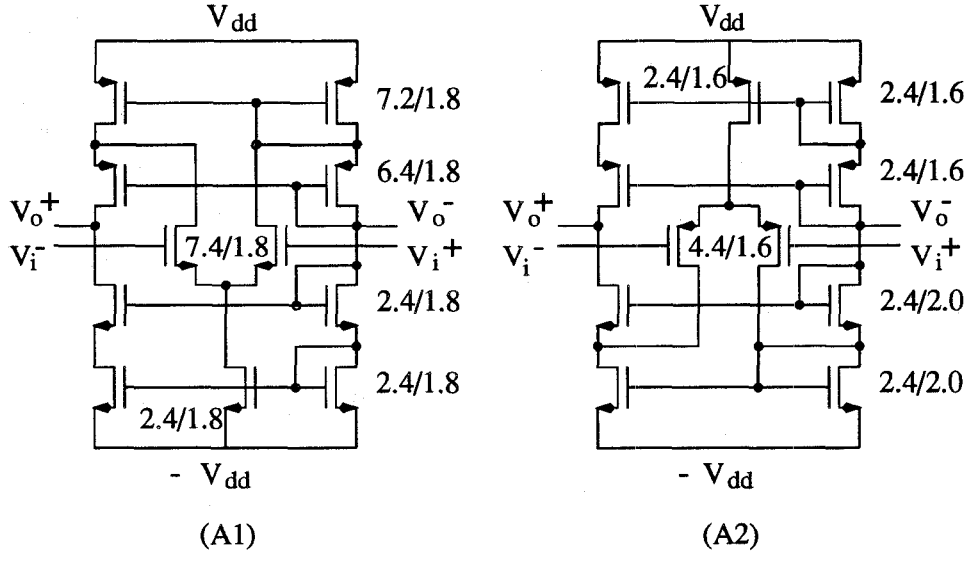

Figure 5. Gain boosting amplifiers

Since the negative output of the gain boosted op-amp (Fig. 4) is not used, the a.c. attenuated output (negative output) of the amplifiers A_1 and A_2 are used to provide the gate bias of the transistors M_8 and M_6 respectively. In the gain boosted op-amp, the d.c. voltages at the nodes 6 and 7 are the same while the a.c. signals at the two nodes are in opposite phase. Hence, instead of using an external voltage for the reference input (positive input) of the boosting amplifier A_2 (as in [4]), the input is connected to the node 6. Similarly, the positive input of the amplifier A_1 is connected to the node 10. This completes the self-biasing of the high performance op-amp. Note that, the gain boosted op-amp uses only the V_{dd} and $-V_{dd}$ supply rails for biasing. This is in contrast to the op-amp in [4] which requires 3 additional bias voltages for the main op-amp and for each of the gain boosting amplifiers.

The design guideline for stability given in [4] is valid for this op-amp also. For single pole settling behavior, the unity gain frequency of the boosting amplifiers should be larger than the bandwidth of the closed loop op-amp and smaller than the second pole of the original op-amp.

4. Simulation Results

The performances of both the self-biased and the externally biased non-boosted op-amps and the self-biased gain boosted op-amp are predicted through Spice simulation. For this simulation, level-2 MOS model for a 1.6μ process [9] was used. In Section 2 the design variables of the fully complementary folded cascode op-amps are given. For our simulation comparison of self-biasing with external biasing we took the design point which is given in Table 1. The same design point was taken for the boosted op-amp also. The transistors in the gain boosting amplifiers are appropriately sized (as shown in Fig. 5) to satisfy the stability condition given in [4]. The load capacitance was $1pF$ and the supply was ± 3 volts.

Variables	Value
W_1/L_1	50.0/3.2
W_3/L_3	16.0/1.6
W_4/L_4	24.0/1.6
W_6/L_6	24.0/1.6
q	2/3

Table 1. Value of the design variables at the simulation point

The simulation results are given in Table 2. Unity gain frequency (UGF) and phase margin (PM) are effectively the same for all of the three op-amps. D.C. gain (A(0)) of the two non-boosted op-amps are the same while it is doubled (in dB) in the boosted op-amp. Because of the high gain, CMRR and PSRR of the gain boosted op-amp are better than those of the non-boosted op-amps.

Slew rate (SR) of the self-biased op-amps are 10% less than that of the externally biased op-amp. For the

Performance	Ext.-Biased	Self-Biased	Self-Biased with Gain Boosting
$A(0)$ (dB)	50	50	99
UGF (MHz)	106	106	109
PM (deg.)	75	74	71
$PSRR$ @ 0 Hz (dB)	53.16	57.01	100.13
$PSRR$ @ 1 MHz (dB)	53.03	56.82	83.29
$CMRR$ @ 0 Hz (dB)	82.29	83.8	111.3
$CMRR$ @ 1 MHz (dB)	57.54	57.09	56.74
SR (V/μsec.)	234, 216	209, 197	210, 198
0.1% ST (nsec)	35.1, 35.0	36.7, 36.4	37.5, 37.5
PD (mW)	4.83	3.91	4.43

Table 2. Spice simulation results

settling time measurement we used the feedback circuit configuration given in [4], with the feedback factor of 0.5. Due to self-biasing, the power dissipation (PD) of the non-boosted op-amp is reduced by 19%. The power dissipation of the boosted op-amp is also less than that of the non-boosted externally biased op-amp.

Finally, the ratio i_o/I_{tot} was measured to be 0.50 and 0.46 for the externally biased and self-biased op-amps, respectively. This is very close to the theoretical prediction given by the equations (14) and (15).

5. Summary

A self-biasing technique for folded cascode CMOS op-amps is presented. The biasing technique uses no additional devices and no bias voltages other than the two supply rails. Nevertheless, all transistors are biased in saturation and hence, the high performance of the op-amps is maintained. This is achieved by appropriate use of a.c attenuated internal nodes to provide the gate bias of the transistors and following transistor sizing constraints derived through detailed circuit analysis. Thus, self-biasing eliminates the area and the power overhead of the bias circuitry and it also removes the long biasing wires which are susceptible to noise and cross-talk.

While self-biasing has a number of performance advantages the cost is a small reduction in slew rate. Through detailed circuit analysis the slew rate is predicted and with proper transistor sizing its reduction is minimized.

The self-biasing technique is applied to a gain boosted folded cascode op-amp which can provide 100 dB gain and 100 MHz unity gain frequency with single pole settling behavior. Simulation results show that the high performances is maintained while nine bias voltages are eliminated.

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