Power Converter Based Impedance Emulation of Passive Loads for Anti-Islanding Tests

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***Abstract*—A passive RLC load is essential for conducting anti-islanding tests of inverter based grid connected distributed generator (DG) systems. A variable load is desirable if the tests need to be carried out over a range of operating conditions and on multiple DG based inverters of different ratings. Use of a physical load results in increased cost and space requirements, particularly when the rating of the DG under test increases. This paper presents power converter based impedance emulation technique to actively implement such a parallel RLC load. The dynamic and steady-state response of the load are synthesized using closed loop control of the passive load emulation converter (PLEC), such that the terminal behaviour of the converter matches the passive RLC load characteristics closely. The proposed technique is verified using simulations and experiments that consist of proposed PLEC working in tandem with a current controlled 3ϕ DG based inverter on a 5 kVA hardware prototype in laboratory.**

***Index Terms*—Anti-islanding, distributed generator (DG), equipment under test (EUT), front end converter, impedance emulation, passive load emulator, passive load emulation converter.**

List of Symbols

V_g	Per phase grid voltage
V_{pcc}	Per phase voltage at PCC
V_{dc}	DC link voltage
I_{dg}	DG current
I_g	Grid current
I_o	Output current of PLEC
I_i	Input current of PLEC
I_{FEC}	FEC current
I_{dc}	DC link current
L_f	Inductive filter of PLEC
C_f	Capacitve filter of PLEC
R_f	Damping resistance
L_{FEC}	Inductive filter of FEC
C_{dc}	DC link capacitor
$S1$	Grid side breaker
$S2$	DG side breaker

I. Introduction

The number of installations of renewable energy based distributed generators (DG) has rapidly increased owing to decentralization of energy production [1]. A voltage source inverter (VSI) is typically used as a power electronic interface that facilitates DG interconnection with the grid. Anti-islanding tests of such a grid connected inverter based DG are essential to evaluate its performance in detecting grid discontinuity [2]. Also unintentional islanding [2]–[4], which is undesirable because of safety concerns, damage to utility equipment and to the DG [5], can be subsequently prevented using such tests of inverter based DG.

As per IEEE Std. 1547-2018, the equivalent circuit model, as shown in Fig. 1(a), is considered for anti-islanding tests, which consists of a parallel RLC load, grid and the DG functioning in current controlled mode forming the equipment under test (EUT). Having a physical RLC load for this purpose results in several disadvantages in terms of cost and space requirements, especially when the rating of the DG under test increases. Also, tuning requirements of load parameters to suit the specifications of tests lead to additional design difficulties [6]. In addition, cooling arrangements are required because of the heat dissipation in the resistive branch.

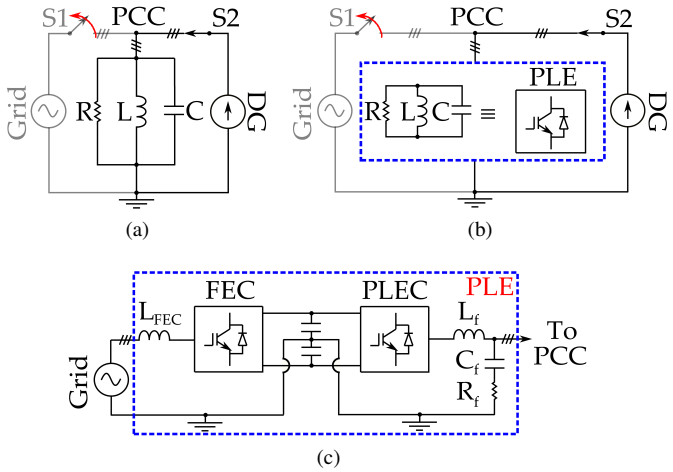

Fig. 1: (a) Equivalent circuit used for anti-islanding tests (b) Proposed impedance emulation technique where passive RLC load is replaced by PLE (c) Power circuit schematic of the passive load emulator (PLE) consisting of a front end converter (FEC) and the passive load emulation converter (PLEC).

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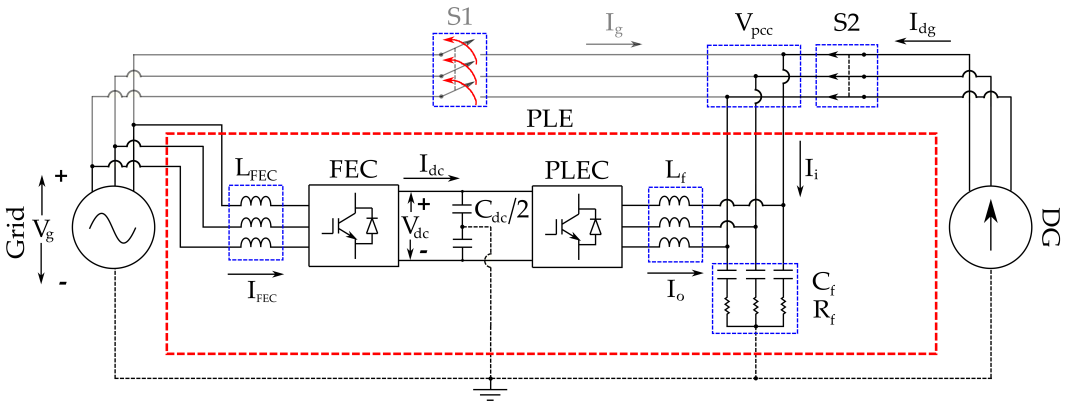


Fig. 2: Circuit schematic of the anti-islanding test-bench consisting of a grid, DG and the PLE.

On the other hand, power converter based impedance emulation technique brings several benefits such as lower cost, compact design and no power dissipation as the load is virtual [7]. Impedance emulation technique is often used with the help of different types of control strategies to replace the passive load present in the circuit [8]. All the control strategies basically focus on drawing a specific amount of power from the source, which can be a grid or a DG, such that the relationship between voltage and current at the terminal of the converter resembles the passive load [5].

In this paper, the passive load emulator (PLE) as shown in Fig. 1(b) is used for RLC load emulation. The setup consists of two 3ϕ converters connected in back-to-back configuration constituting a bidirectional front end converter (FEC) and the passive load emulation converter (PLEC), as shown in Fig. 1(c). Islanding tests are conducted in accordance with IEEE Std. 1547-2018, where the inductive and capacitive branches present in the parallel RLC load are compensated by each other. So, the proposed architecture controls the PLEC such that it draws only active power from the source during emulation. This active power drawn by PLEC is fed back to the grid by FEC, which leads to minimal power dissipation. A digital signal processor (DSP) platform is employed on which the proposed control is implemented. Different load parameters are obtained by appropriately changing the control parameter values in DSP.

II. Proposed Control Architecture

In the anti-islanding test-bench, initially both grid and DG are connected to PCC through switches S1 and S2 respectively as shown in Fig. 2. During islanding, S1 is opened while S2 remains closed [9]. The control architecture thus has to emulate the RLC load at first in the presence of grid and afterwards in its absence. Thus, the control architecture considers two operating modes of operation as follows.

A. Impedance emulation during grid connected mode of operation :

When a parallel RLC load is connected to the grid and DG both, it draws a specific amount of current and emulation is achieved by drawing the same amount of current using the current controlled 3ϕ PLEC. The proposed control architecture is shown in Fig. 3, where the PLEC is operated in current controlled mode using an inner current loop consisting of a proportional resonant controller ($G_{pri}(s)$) operating in stationary reference frame [10] and an outer reference generator block providing the required current reference derived from the sensed grid voltage. The bode plots of loop transfer function ($G_{pri}(s).G_i(s)$) and closed loop transfer function of current loop are shown in Fig. 4.

During grid connected mode of operation, PLEC is connected to the grid which is a voltage source having very small series impedance. So, the capacitive filter does not provide any filtering. Thus for the current loop design calculations, capacitive filter can be ignored. But the capacitive filter contributes in achieving the desired capacitance in the emulated RLC load, therefore the total capacitance that should be synthesized by PLEC is correspondingly lower [5].

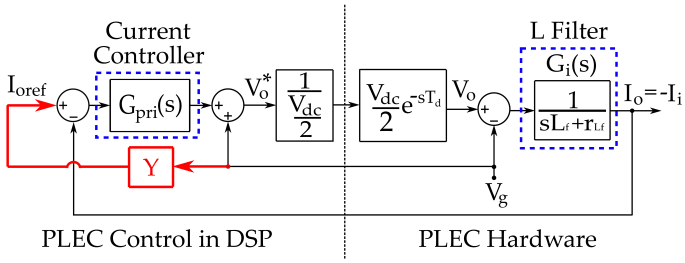


Fig. 3: Current loop and reference generator block during grid connected mode of operation.

From Fig. 3,

$$G_{pri}(s).G_i(s) = K_{pri}\left(\frac{s^2+\frac{K_{iri}}{K_{pri}}s+(\omega_o)^2}{s^2+(\omega_o)^2}\right)\left(\frac{1}{sL_f+r_{Lf}}\right)$$

When $\omega = \omega_{gci}$, taken as one-tenth of switching frequency,

$$|G_{pri}(j\omega).G_i(j\omega)|_{\omega=\omega_{gci}} = \frac{K_{pri}}{\sqrt{(\omega_{gci}L_f)^2+(r_{Lf})^2}}$$

But $|G_{pri}(j\omega).G_i(j\omega)|_{\omega=\omega_{gci}} = 1$

$$\Rightarrow K_{pri} = \sqrt{(\omega_{gci}L_f)^2+(r_{Lf})^2} \quad (1)$$

Calculation of K_{iri} is done by assuming that a band of $\pm\triangle\omega_o$ rad/sec around ω_o rad/sec in magnitude plot of $G_{pri}(s)$ always has a gain of K_i [10].

Gain of $G_{pri}(s)$ at $s = j(\omega_o \pm \triangle\omega_o)$ can be calculated using the assumption that $\frac{\triangle\omega_o}{\omega_o} << 1$.

$$\Rightarrow K_i = K_{pri} \times \sqrt{1 + \left(\frac{K_{iri}}{2K_{pri} \times \triangle\,\omega_o}\right)^2}$$

$$\Rightarrow K_{iri} = 2\,\triangle\,\omega_o \sqrt{(K_i)^2 - (K_{pri})^2} \tag{2}$$

For a parallel RLC load,

$$Y^* = \frac{1}{R} + \frac{1}{sL} + sC$$

So to emulate the load,

$$\frac{I_i}{V_g} = Y^*$$

$$\Rightarrow \frac{I_o}{V_g} = \frac{-I_i}{V_g} = \frac{YG_{pri}(s)}{sL_f + r_{Lf} + G_{pri}(s)} = -Y^*$$

At 50 Hz, $|G_{pri}(s)|$ is very high,

$$\Rightarrow Y = -Y^* \tag{3}$$

TABLE I: Current controller parameters.

S.N.	Parameter	Value
1	K_{pri}, K_{iri}	31.4, 596.5
2	ω_{gci}	$2\pi\times1000$ rad/sec
3	Phase margin	90.1°

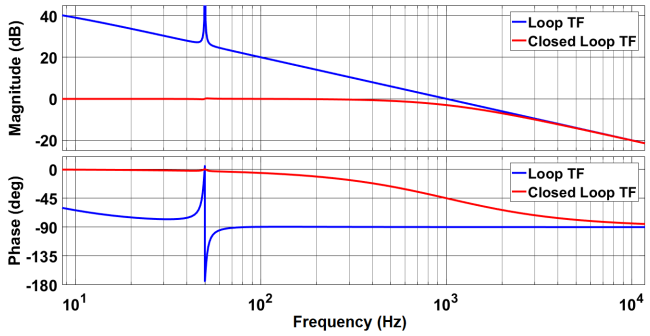


Fig. 4: Bode plots of loop transfer function and closed loop transfer function of current loop.

B. Impedance emulation during islanded mode of operation :

When a parallel RLC load is connected to the DG after grid disconnection, a specific amount of voltage is maintained at PCC and emulation is achieved by maintaining the same amount of voltage using the voltage controlled 3ϕ PLEC.

Two control strategies are proposed for RLC load emulation during islanded mode of operation. The first one is a two-loop control strategy and the second one is a single-loop control strategy as mentioned below.

1. Two-loop control : Desired voltage can be maintained at PCC by making use of the two-loop control architecture as shown in Fig. 5, where the PLEC is operated in voltage controlled mode using an inner voltage loop consisting of proportional resonant controller ($G_{prv}(s)$) and an outer reference generator block providing the required voltage reference derived from the sensed DG current. Voltage loop is designed to be four times slower than the current loop. So, for the voltage loop design calculations, current loop can be considered to be unity. The bode plots of loop transfer function ($G_{prv}(s).G_v(s)$) and closed loop transfer function of voltage loop are shown in Fig. 6.

Voltage loop comes into effect when islanding occurs. So, communication is required between grid side breaker and PLEC control. This is disadvantage of two-loop control strategy.

From Fig. 5,

$$G_{prv}(s).G_v(s) = K_{prv}\left(\frac{s^2 + \frac{K_{irv}}{K_{prv}}s + (\omega_o)^2}{s^2 + (\omega_o)^2}\right)\left(\frac{1}{sC_f} + R_f\right)$$

Calculation of K_{irv} is done by assuming that a band of $\pm\triangle\omega_o$ rad/sec around ω_o rad/sec in magnitude plot of $G_{prv}(s)$ always has a gain of K_v.

Gain of $G_{prv}(s)$ at $s = j(\omega_o \pm \triangle\omega_o)$ can be calculated using the assumption that $\frac{\triangle\omega_o}{\omega_o} << 1$.

$$\Rightarrow K_v = K_{prv} \times \sqrt{1 + \left(\frac{K_{irv}}{2K_{prv} \times \triangle\,\omega_o}\right)^2}$$

$$\Rightarrow K_{irv} = 2\,\triangle\,\omega_o \sqrt{(K_v)^2 - (K_{prv})^2}$$

As the bandwidth of voltage loop is low, $K_v >> K_{prv}$.

$$\Rightarrow K_{irv} = 2\,\triangle\,\omega_o \times K_v \tag{4}$$

When $\omega = \omega_{gcv}$, taken as one-fourth of current loop bandwidth, that is one-fortieth of switching frequency,

$$|G_{prv}(j\omega).G_v(j\omega)|_{\omega=\omega_{gcv}} = \left(\frac{K_{prv}}{(\omega_o)^2 - (\omega_{gcv})^2}\right)$$

$$\left(\sqrt{\left((\omega_o)^2 - (\omega_{gcv})^2\right)^2 + \left(\frac{\omega_{gcv}K_{irv}}{K_{prv}}\right)^2}\right)\left(\sqrt{(R_f)^2 + \left(\frac{1}{\omega_{gcv}C_f}\right)^2}\right)$$

But $|G_{prv}(j\omega).G_v(j\omega)|_{\omega=\omega_{gcv}} = 1$

$$\Rightarrow K_{prv} = \sqrt{\frac{1}{(R_f)^2 + \left(\frac{1}{\omega_{gcv}C_f}\right)^2} - bigg(\frac{\omega_{gcv}K_{irv}}{(\omega_o)^2 - (\omega_{gcv})^2}\right)^2} \tag{5}$$

For a parallel RLC load,

$$\text{Impedance} = Z^* = R \;||\; sL \;||\; \frac{1}{sC}$$

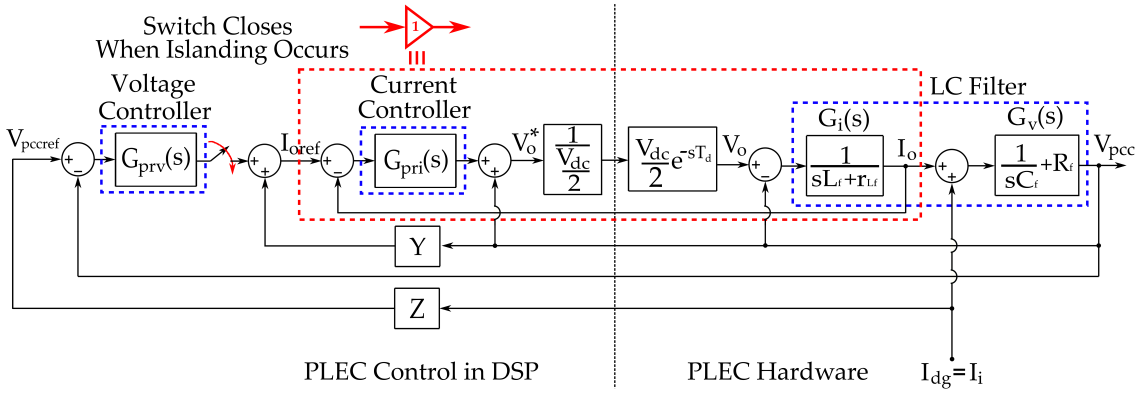


Fig. 5: Two-loop control strategy showing voltage loop and reference generator block during islanded mode of operation.

So, to emulate the load,

$$\frac{V_{pcc}}{I_{dg}} = Z^*$$

$$\Rightarrow \frac{V_{pcc}}{I_{dg}} = \frac{ZG_{prv}(s)\left(\frac{1}{sC_f}+R_f\right)}{1+G_{prv}(s)\left(\frac{1}{sC_f}+R_f\right)} = Z^*$$

At 50 Hz, $|G_{prv}(s)|$ is very high,

$$\Rightarrow Z = Z^* \tag{6}$$

TABLE II: Voltage controller parameters.

S.N.	Parameter	Value
1	K_{prv}, K_{irv}	0.015, 6.28
2	ω_{gcv}	$2\pi \times 250$ rad/sec
3	Phase margin	78.86°

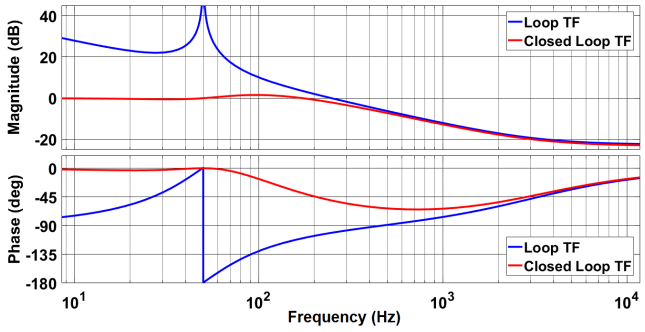


Fig. 6: Bode plots of loop transfer function and closed loop transfer function of voltage loop.

2. Single-loop control : Desired voltage is maintained at PCC by making use of the existing current loop mentioned in grid connected mode as shown in Fig. 7(a). So the current in grid connected mode and the voltage in islanded mode are controlled using a single control loop.

As single control loop is used for both grid connected mode and islanded mode, the control strategy needs no communication from grid side breaker regarding time of islanding. This is advantageous over two-loop control strategy.

From Fig. 7(a),

$$\frac{V_{pcc}}{I_{dg}} = \frac{\left(\frac{1}{sC_f}+R_f\right)}{1-\left(\frac{1}{sC_f}+R_f\right)\left(\frac{G_{pri}(s)\times Y}{sL_f+r_{Lf}+G_{pri}(s)}\right)}$$

At 50 Hz, $|G_{pri}(s)|$ is very high,

$$\Rightarrow \frac{V_{pcc}}{I_{dg}} = \frac{\left(\frac{1}{sC_f}+R_f\right)}{1-\left(\frac{1}{sC_f}+R_f\right)\times Y}$$

But $Y = -Y^*$,

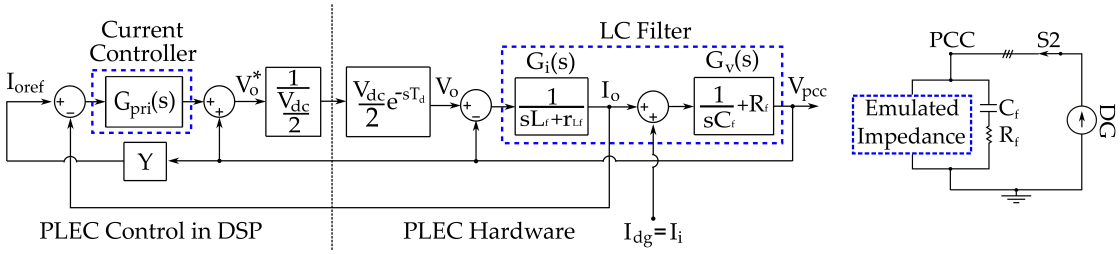
$$\Rightarrow \frac{V_{pcc}}{I_{dg}} = \frac{\left(\frac{1}{sC_f}+R_f\right)}{1+\left(\frac{1}{sC_f}+R_f\right)\times Y^*}$$

But $Z^* = \frac{1}{Y^*}$,

$$\Rightarrow \frac{V_{pcc}}{I_{dg}} = \frac{\left(\frac{1}{sC_f}+R_f\right)\times Z^*}{\left(\frac{1}{sC_f}+R_f\right)+Z^*} \tag{7}$$

Relationship between V_{pcc} and I_{dg} gives the impedance equivalent to parallel combination of capacitive filter and Z^* as shown in Fig. 7(b). So, the PLEC has to emulate lower value of capacitance in the emulated RLC load as mentioned in grid connected mode of operation.

Bode plots of the emulated impedance with different bandwidth values of the current loop are shown in Fig. 8. The bode plots of the emulated impedance close to 50 Hz frequency are shown in Fig. 9, where it can be observed that the accuracy of the emulated impedance improves as the bandwidth increases.



(a) (b)

Fig. 7: (a) Single-loop control architecture, (b) Effect of capacitive filter in impedance emulation.

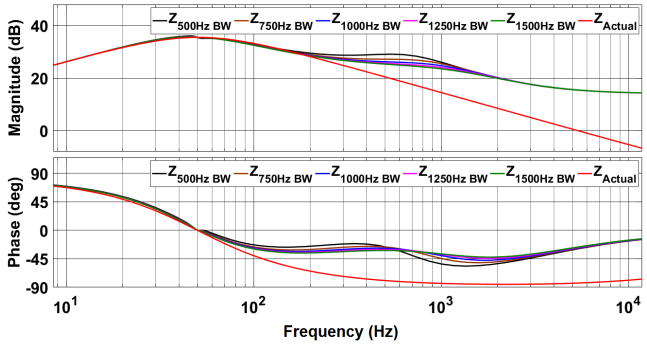


Fig. 8: Bode plots of the emulated RLC load with different bandwidth values and actual passive load with R=60 Ω, L=0.34 H, r_L=1 Ω, C=30 μF, r_C=0.1 Ω.

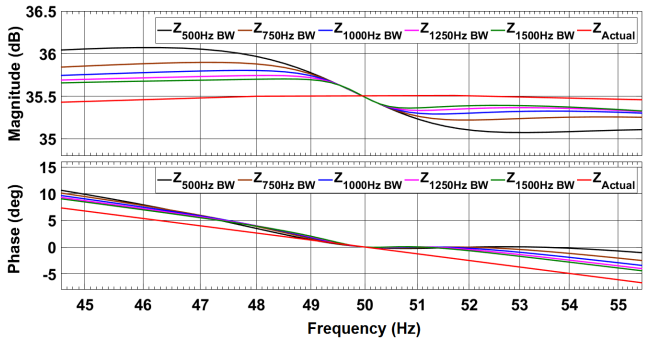


Fig. 9: The bode plots of the emulated RLC load close to 50 Hz frequency with different bandwidth values and actual passive load with R=60 Ω, L=0.34 H, r_L=1 Ω, C=30 μF, r_C=0.1 Ω.

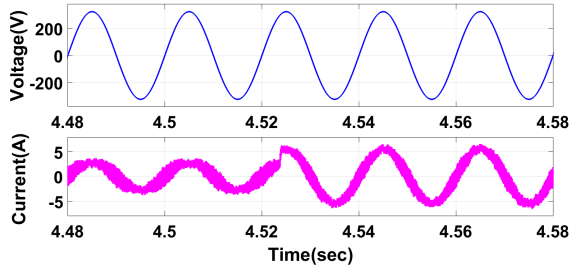
III. Simulation and Experimental Results

Simulations and experiments are done in accordance with IEEE Std. 1547-2018. Parameters of the proposed anti-islanding test-bench are mentioned in Table III.

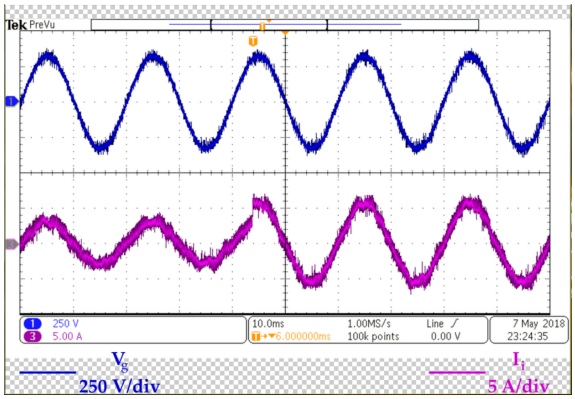
Fig. 10 shows the step change of input current of the PLEC due to step change of emulated resistance from 120 Ω to 60 Ω during grid connected mode of operation. It can be observed that the current tracks the change instantaneously because of the high current loop bandwidth.

TABLE III: Anti-islanding test-bench parameters.

S.N.	Parameter	Value
1	PLEC power rating	2.64 kVA
2	Grid voltage rating	230 V
3	DG current rating	3.8 A
4	Grid and DG power factor	1
5	DC link voltage	800 V
6	Switching frequency	10 kHz
7	Filter parameters	L_f=5 mH, C_f=10 μF, R_f=5 Ω
8	Load parameters	R=60 Ω, L=0.34 H, r_L=1 Ω, C=30 μF, r_C=0.1 Ω
9	Load quality factor	1

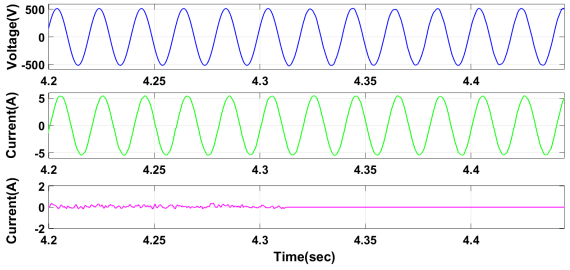


(a)

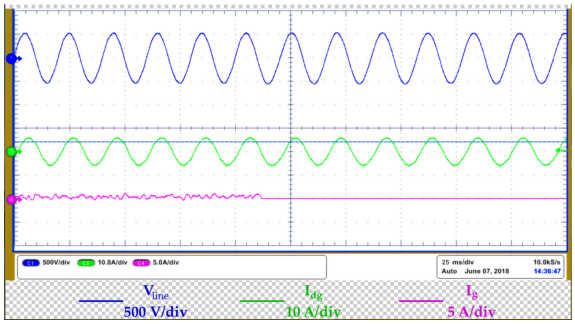


(b)

Fig. 10: (a) Simulation and (b) Experimental results of R phase grid voltage and input current of PLEC which show the step change of current from 0.5 pu to 1 pu due to step change of emulated resistance from 120 Ω to 60 Ω during grid connected mode of operation.

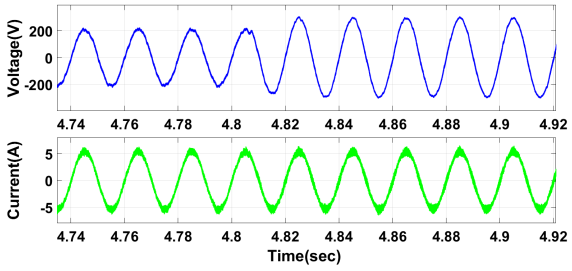


(a)

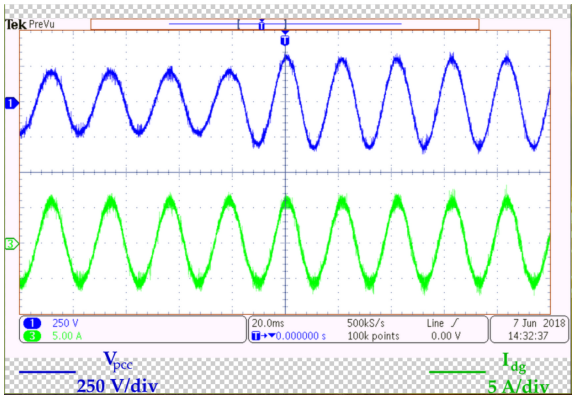


(b)

Fig. 11: (a) Simulation and (b) Experimental results of line voltage at PCC (R-Y), DG current and grid current which show the transition from grid connected mode to islanded mode.



(a)



(b)

Fig. 12: (a) Simulation and (b) Experimental results of R phase voltage at PCC and DG current which show the step change of voltage from 0.7 pu to 1 pu due to step change of emulated resistance from 42 Ω to 60 Ω during islanded mode of operation.

Fig. 11 shows the transition from grid connected mode of operation to islanded mode of operation. It can be observed that the grid current is completely zero after islanding because of opening of the grid side breaker. Also, there is no effect of islanding on the DG current and voltage at PCC. So, the control architecture emulates the RLC load properly during grid connected mode as well as islanded mode.

Fig. 12 shows the step change of R phase voltage at PCC due to step change of emulated resistance from 42 Ω to 60 Ω during islanded mode of operation. It can be observed that the voltage tracks the change instantaneously for both the simulation and experiment as the DG current is held constant.

IV. Conclusions

Power converter based passive RLC load emulation is proposed for anti-islanding tests. Two control architectures are proposed that emulate the load in both grid connected mode and islanded mode. Emulation is verified at 50 Hz as well as over a wide range of frequency with the help of simulations. Experiments are done on 3ϕ, 5 kVA hardware setup along with a current controlled grid tied inverter that verify the high performance achieved by the proposed passive load emulator.

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