A Simple Indicator based PLL for Distorted Grid Conditions

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***Abstract*—This paper proposes a simple indicator based phase lock loop (PLL) which is capable of producing distortionless reference waveforms in case of the presence of unbalance and harmonics in the grid. The proposed configuration also has a faster dynamic response thus catering to phase jumps as well. Unlike the existing research works, this proposal doesnt make use of filtering, signal modifications or advanced algorithms. The simplest form of synchronous reference frame (SRF) PLL is retained and effectively made use of in the simplest way to achieve the objectives. The proposed concept makes use of the idea of controlling the instantaneous acceleration between the point of common coupling (PCC) space vector and the existing $d-q$ frame by adding the error to the PLL. This addition is activated or disabled depending on the conditions like phase jump, unbalance and harmonics leading to the acceleration. Separate algorithms indicate the condition. The proposed concept is validated with sufficient simulation results.**

***Index Terms*—PLL, Grid connected converters, Unbalance, Harmonics.**

I. Introduction

The increased demand for energy supply as well as the depletion of conventional energy resources have opened up the possiblity of using renewable energy resources like solar, wind etc. Consequently a number of power electronic converters which interface these distributed energy resources are being added to the exisisting power grid. Synchronization of these power electronic converters with the grid is a crucial aspect that needs to be taken care of while integrating to the grid. The most common technique that is employed for grid synchronization is the phase lock loop (PLL).

One of the most robust and simplest PLL configurations for a three phase converter is the synchronous reference frame (SRF) PLL [1]. The conventional SRF PLL however suffers from the drawback that in the presence of unbalanced and harmonic voltages in the grid, the PLL output gets distorted thus affecting the quality of the injected current into the grid. It has also become a mandatory requirement in most of the countries that the converter stays connected to the grid and deliver the required amoout of power without distortions in case of a fault conditions [2], [3]. The conventional SRF PLL exhibits serious limitations under such conditions as well. A low bandwidth (BW) proportional integral (PI) can be used in the conventional SRF PLL to solve this. But this affects the transient response of the converter in conditions like a phase jump.

Researchers have tried to adddres this issue by resorting to several techniques. One of the attempts is to use open loop PLLs which are devoid of PIs [4], [5]. These methods make use of Fourier transform processing, space vector filtering, weighted least square estmation etc. Inspite of the clear references these methods provide under distorted grid conditions, they are suitable only for a particular operating frequency. Frequency shifts and phase jumps cannot be suitably addressed by these methods. Above all the complexity of the algorithms increases the computational burden.

In the closed loop methods in which the SRF PLL falls, in loop implementation of filters is a common approach prevalent in the literature [6], [7]. The in loop filtering techniques suffer from the issue of complexity due to higher order and selective filters as well the diffculty to model such PLLs. The other approach in the close loop method is the pre filtering technique. The pre techniques refer to extraction of the positive sequence components of the grid volatge space vector. The extracted positive sequence component is fed to the loop of the SRF PLL. Double SRF PLL and Decoupled Double SRF PLL are the popular configurations in this category [8], [9]. These methods make use of two synchronously rotating frames in the opposite direction to extract the sequences. Apart from the complexity, the dynamics of the such PLLs in conditions of phase jumps and frequency shifts are not satisfactory. More advanced structures like a single integrator based SRF PLL and double second order generalized integrator (DSOGI) PLL also fall in the category of pre loop filtering [10], [11]. The complexity and the algorthmic burden of these techniques overshadows the performance advantages. Complex pre signal reforming techniques have also appeared in the literature [12]. Like the in loop filtering models, the modelling of prefiltering based PLLs are also difficult [13].

This paper proposes a simple indicator based PLL which works like the conventional SRF PLL with a very high transient response and at the same time rejecting the harmonic and unbalance components. The PLL structure is maintained at the simplest level. The proposed configuration is desribed in section II. Some results are provided in section III and in section IV, the paper is concluded.

II. Proposed Configuration

The proposed configuration is presented in Fig. 1. The conventional SRF PLL is indicated by the marked portion. The rest of the section is the new addition. The BW of PI

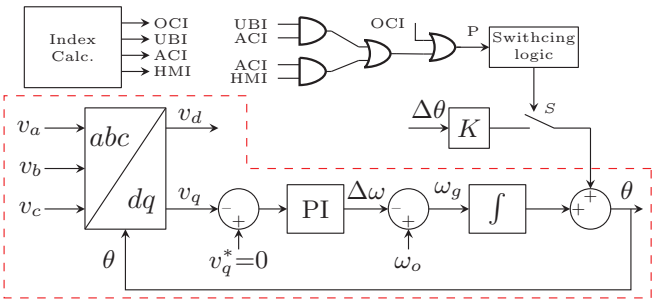


Fig. 1: Proposed configuration

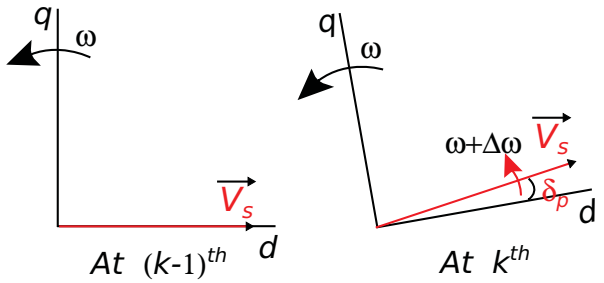


Fig. 2: Working of Acceleration Indicator

in the PLL is made low in the proposed configuration. The newly added part consists of an index calculator block which outputs four indicators interlinked through a logic function. The indicators are the Overcurrent indicator (OCI), the Unbalance Indicator (UBI), the Acceleration Indicator (ACI) and the Harmonic Indicator (HMI). These indicators are designed and implemnted in such a manner that the presence of one of the factors namely overcurrent caused due to a phase jump in PCC space vector, unbalance in PCC space vector, acceleration of the PCC space vector or harmonics in PCC space vector is notified by the respective indicators. Depending on the basis of this information, the switching function block is activated which produces the switching signal for the switch (S). The switch passes the instantaneous angular difference ($\Delta\theta$) of the PCC space vector with respect to the PLL $d-q$ frame as an enhancement term to the conventional PLL. The concept of enhancement of PLL and switching logic has been presented previously in [14].

A. The Acceleration Indicator (ACI)

The acceleration indicator (ACI) forms the coordinating indicator for the UBI and HMI. ACI is based on the idea that whenever there is an acceleration of the PCC space vector with respect to the current working frame ($d-q$) of reference, an indication is given to the logic circuitry by making the output of ACI block = 1. The acceleration of the PCC space vector with respect to the current $d-q$ frame can happen in the event of a phase jump in the PCC space vector, unbalance in the PCC space vector and due to presence of harmonic space vectors in PCC.

Consider the Fig 2. At the $k-1$ th instant, the PCC space vector ($\overrightarrow{V_s}$) is aligned along the d axis of the $d-q$ frame and the system is rotating at a speed of ω. At the k th instant

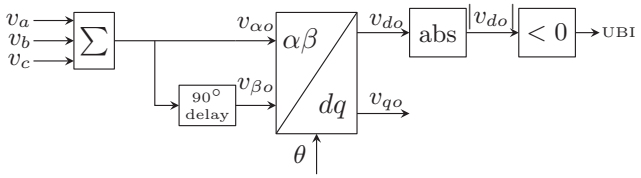


Fig. 3: Proposed algorithm for unbalance indications

$\overrightarrow{V_s}$ undergoes an acceleration which manifests as an angular difference δ with respect to the unchanged $d-q$ frame.

The instantaneous relative acceleration of the PCC space vector with respect to the current frame ($\frac{d\delta_p}{dt}$) can be expressed as given by (1) , where $\delta_p(k)$ is the position of the PCC space vector at the kth instant with respect to the current working frame of reference, v_d, v_q are instantaneous d and q values of the PCC voltage space vector and T_s is the sampling time period.

$$\begin{aligned} \frac{d\delta_p}{dt} &= \frac{\delta_p(k)-\delta(k-1)}{T_s} \\ \delta_p(k) &= tan^{-1}\frac{|v_q(k)|}{|v_d(k)|} \\ \delta_p(k-1) &= tan^{-1}\frac{|v_q(k-1)|}{|v_d(k-1)|} \end{aligned} \tag{1}$$

In the steady state operation, $\frac{d\delta_p}{dt}$ will be 0. When there is an acceleration, the output of the ACI is made 1 based on the condition

$$\frac{d\delta_p}{dt} \geqslant limit \Longrightarrow ACI = 1 \tag{2}$$

In the case of a phase jump, the ACI output will be 1. But this is passed on to the next ORing stage depending only on the UBI and HMI outputs. However, in the event of a phase jump, a high overcurrent will be introduced in the system and this causes the OCI output to be 1. The detailed working of OCI is given in [14]. The OCI output being 1 activates the switching block which appropriately produces a switching function for the switch S.

B. The Unbalance Indicator (UBI)

The presence of unbalance in the grid space vector reflects as a second harmonic term in the d and q values of voltage. This can be understood from the following. Consider the set of unbalanced phase voltages as given by (3).

$$\begin{aligned} v_a(t) &= kV_m cos\left(\omega t\right), \\ v_b(t) &= V_m cos\left(\omega t - \tfrac{2\pi}{3}\right), \\ v_c(t) &= V_m cos\left(\omega t - \tfrac{4\pi}{3}\right) \end{aligned} \tag{3}$$

The stationary axis voltages can be written as (4)

$$\begin{aligned} v_\alpha(t) &= (k+0.5)V_m cos\left(\omega t\right), \\ v_\beta(t) &= 1.5V_m sin\left(\omega t\right) \end{aligned} \tag{4}$$

The equivalent d and q values can be written as given by (5).

$$v_d = (k+0.5)V_m cos\,(\omega t)\,cos\,(\omega t) + 1.5V_m sin\,(\omega t)\,sin\,(\omega t)\,,$$
$$v_q = -(k+0.5)V_m cos\,(\omega t)\,sin\,(\omega t) + 1.5V_m sin\,(\omega t)\,cos\,(\omega t) \tag{5}$$

Mathematically manipulating, equation (5) can be rewritten as (6).

$$v_d = 1.5V_m + \frac{k-1}{2}V_m + \frac{k-1}{2}V_m cos\,(2\omega t)\,,$$
$$v_q = \frac{1-k}{2}V_m sin\,(2\omega t) \tag{6}$$

The presence of the second harmonic term introduces a relative acceleration between PCC space vector and the working frame as given by (1). As a result the ACI output is made 1. The UBI is designed in such a way that the UBI ouput has to be made 0 on the presence of unbalance. This will prevent the ACI output from activating the switching function block and hence the PLL output (θ) to be devoid of the second harmonics.
The algorithm shown in Fig. 3 is implemented as a 'UBI to acheive the desired function. The algorithm is derived from the basic trignometric condition that under an unbalance condition the instantaneous sum of phase voltages is equivalent to a non zero sinuoid of fundamental frequency as given by (7). Equation (3) is considered again for deriving the condition for (7)

$$v_a(t) + v_b(t) + v_c(t) = (k-1)V_m cos\,(\omega t) \tag{7}$$

The amount of unbalance propotional to $(k-1)V_m$ can be transformed on to synchronously rotating frame with speed ω. Consequently the DC component can be given by (8) refering to the algorithm shown in Fig 5.

$$v_{do} = (k-1)V_m cos\,(\omega t)\,cos\,(\omega t) + (k-1)V_m sin\,(\omega t)\,sin\,(\omega t) \tag{8}$$

Equation (8) can be equivalentaly written as (9)

$$v_{do} = (k-1)V_m \tag{9}$$

From (9), the condition for UBI can be easily derived as given by (10).

$$UBI = \begin{cases} 1, & \text{if } |v_{do}| = 0 \\ 0, & \text{if } |v_{do}| > 0 \end{cases} \tag{10}$$

C. The Harmonic Indicator

In case of the presence of an nth harmonic space vector at PCC, the d and q axes values will have $(n-1)$ th or $(n+1)$ th frequency terms. Consider the set of phase voltages having nth harmonic as given by (11)

$$v_a(t) = V_m cos\,(\omega t) + kV_m cos\,(n\omega t)\,,$$
$$v_b(t) = V_m cos\left(\omega t - \tfrac{2\pi}{3}\right) + kV_m cos\left(n\omega t - \tfrac{2\pi n}{3}\right), \tag{11}$$
$$v_c(t) = V_m cos\left(\omega t - \tfrac{4\pi}{3}\right) + kV_m cos\left(n\omega t - \tfrac{4\pi n}{3}\right)$$

The stationary axes voltages for (11) can be written as follows

$$v_\alpha(t) = 1.5V_m cos\,(\omega t) + 1.5kV_m cos\,(n\omega t)\,,$$
$$v_\beta(t) = 1.5V_m sin\,(\omega t) \pm 1.5kV_m sin\,(n\omega t) \tag{12}$$

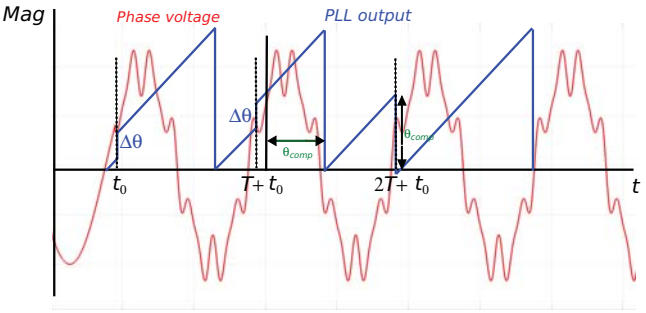


Fig. 4: Concept of harmonic indications

TABLE I: Quadrant determination

$v_d(k)$	$v_q(k)$	Quadrant
+	+	I
-	+	II
-	-	III
+	-	IV

The d and q equivalent values for the above can be given by (13)

$$v_d = 1.5V_m + 1.5kV_m cos[(n\pm1)\omega t],$$
$$v_q = \pm 1.5kV_m sin[(n\pm1)\omega t] \tag{13}$$

$$\Delta\theta = \begin{cases} tan^{-1}\dfrac{|v_q(k)|}{|v_d(k)|}, & \text{for Quadrant I} \\ 180 - tan^{-1}\dfrac{|v_q(k)|}{|v_d(k)|}, & \text{for Quadrant II} \\ 180 + tan^{-1}\dfrac{|v_q(k)|}{|v_d(k)|}, & \text{for Quadrant III} \\ 360 - tan^{-1}\dfrac{|v_q(k)|}{|v_d(k)|}, & \text{for Quadrant IV} \end{cases} \tag{14}$$

The presence of $n\pm1$ frequency terms in the d and q axes values introduces a relative acceleration between PCC space vector and the working $d-q$ frame. This causes the ACI output to go to 1 as there is a relative acceleration between the existing $d-q$ frame and the PCC space vector. The normal state of HMI O/P will be 1. Hence the switching function block is activated and the angular difference ($\Delta\theta$) at the instant of harmonic introduction (say at $t = t_0$) will added to the PLL. The angle caluclation is done based on the table I and equation (14). The angle calculation block informs the HMI block of the angle added.
Consider the Fig. 4. A harmonic phase voltage is shown. At $t = t_0$, the ACI output goes to 1 and the angular difference ($\Delta\theta$) is added to the PLL. The HMI is informed of the angular addition by the PLL enhancement block. As soon as there is an angular addition, the HMI block checks for the zero crossings of the PLL output (θ) and the phase voltage to which the PLL output is the reference. If the zero crossing of both the signals coincide and the angle calculated at the

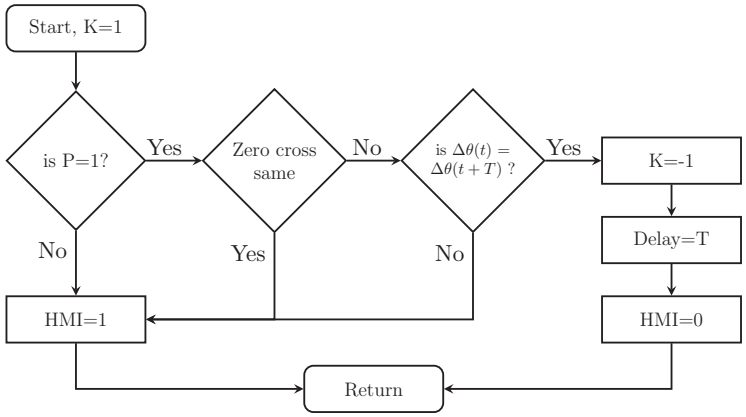


Fig. 5: Complete algorithm for harmonic indications

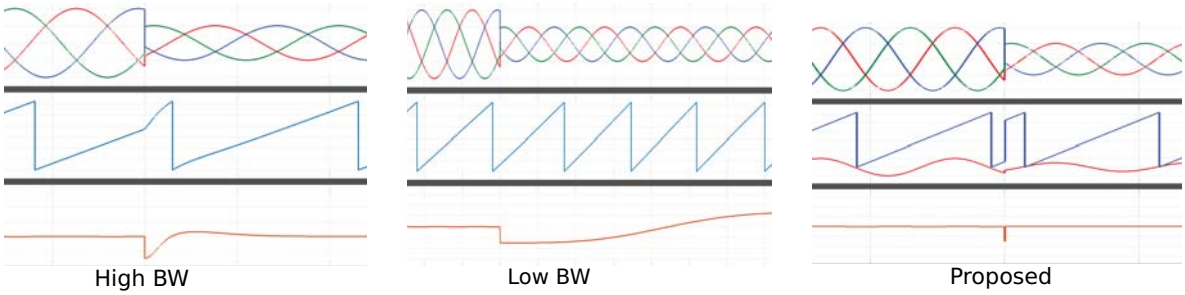


Fig. 6: Case of a phase jump - Ch1).Phase voltages. Ch2).PLL output. Ch3).v_q output

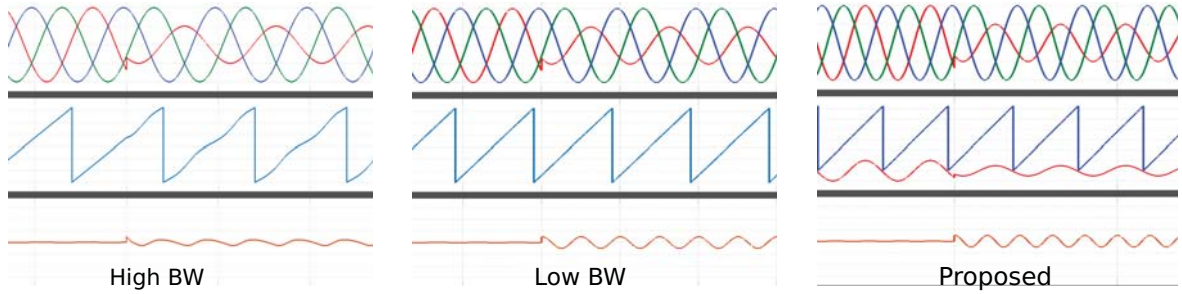


Fig. 7: Case of unbalance - Ch1).Phase voltages. Ch2).PLL output. Ch3).v_q output

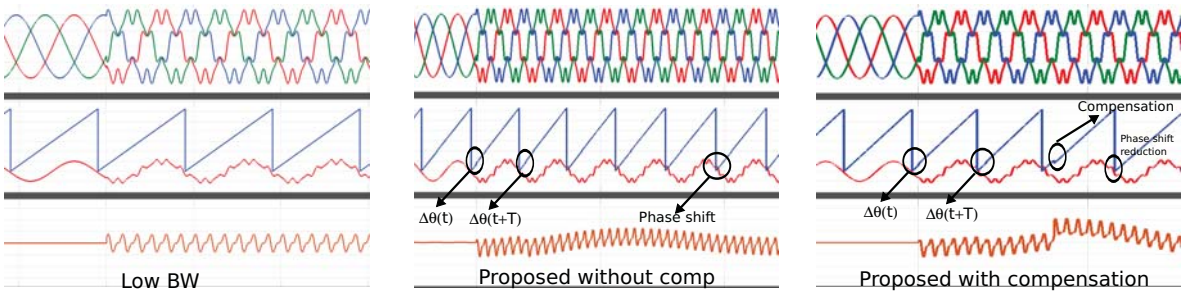
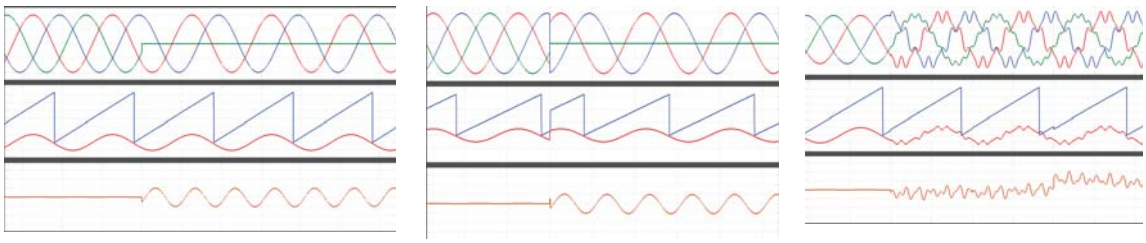


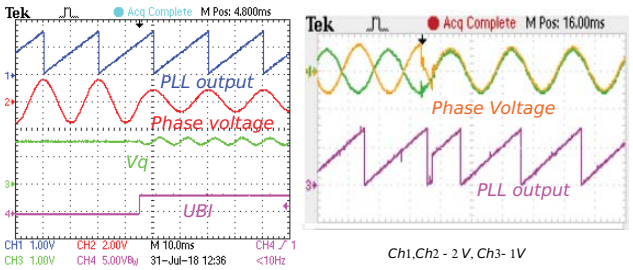
Fig. 8: Case of harmonics - Ch1).Phase voltages. Ch2).PLL output. Ch3).v_q output

periodic instant (t_0+T) is 0, the HMI O/P remains at 1. If the zero crossings of the signals differ and $\Delta\theta(t_0+T) \approx \Delta\theta(t_0)$, it is an indication of harmonics. Note that here T is the time period equivalent to $\frac{1}{\omega}$. The periodicity of the harmonics results in the same $\Delta\theta$ after the fundamental time period. From Fig. 4, it can be seen that the same angle $(\Delta\theta)$ is added after a time equal to $(t_0 + T)$. As the harmoincs presence is confirmed, the phase difference between the PLL output and the phase voltage needs to found out. The angular difference between the 180^o point of the PLL output and the



a.Single faulting b.Single faulting and phase jump c. Unbalance and harmonics

Fig. 9: Extreme conditions-Ch1).Phase voltages. Ch2).PLL output. Ch3).v_q output



a. Unbalance b. 180 degree phase jump

Fig. 10: Experimental results

negative zero crossing of the phase voltage gives a measure of the phase difference. A counter can be implemented to estimate the time difference between these two points. The time difference translates into an equivalent phase difference as given by (15) where θ_{comp} is the compensating phase and Δt is the time difference estimated by the counter.

$$\theta_{comp} = \omega \Delta t \tag{15}$$

This compensating phase difference is fedback to the angle calculation block as the enhancment for the next switching instant. A delay of T is intrdouced in the HMI block for the addition of this error. After the delay the HMI O/P is made 0 which deactivates the switching function block. The entire algorithm is expressed as a flow diagram in Fig. 5.

III. Results

A simulation study for the proposed configuration is done in Matlab/Simulink. Three cases ie . a case of phase jump, an unbalanced sitution and the presence of harmonics are taken for study. More complex cases like the combination of these situiations are not dealt with here. The proposed PLL is compared with a lowbandwidth and a high bandwidth PLL.

1) Case 1: PhaseJump: The test case where a phase jump happens is considered first. In the case of a phase jump, the highbandwidth PLL immediately tracks the phase jump. This can be seen from Fig. 6. The PLL output undergoes a sudden change on the occurence of the phase jump. The v_q voltage is also seen to settlr down quickly. In the case of a low bandwidth PLL, the tracking time is very large. It can be seen from the result that the q axis voltage takes several line cycles to settle. The proposed algorithm is much faster than both the high bandwidth and the lowbandwidth as can be seen. This is due to the quick angle addition on occurence of an acceleration of the PCC space vector. The controller dynamics doesnt come into picture for the proposed one for a phase jump.

2) Case 2: Unbalance: In Fig. 7, the test results for the case of an unbalance is considered. On the introduction of an unbalance, the high bandwidth PLL introduces a double frequency component in the PLL output. The higher bandwidth tries to compensate for the double frequency component introduced in the q axis voltage. The double frequency oscillation in the q axis voltage is seen to be less in this case. The low bandwidth PLL however cuts off the double frequency component from being passed through and hence the PLL output is clean whih is desirable. The proposed configuration can be seen to possesing the same performance as that of a low bandwidth PLL. The presence of the unbalance is detected by the UBI and the angle enhancement is disabled.

3) Case3: Harmonics: The high bandwidth PLL behaves the same way as that in the case of an unbalanced condition. The harmonic content is passed on to the PLL output. However in the case of a low bandwidth PLL, the harmonic content is rejected and the PLL output is clean. In the case of the proposed configuration,, it can be seen from Fig. 8, that an angle addition happens on the introduction of harmonics. On the detection of harmonics, the angle addition is disabled. It can be seen from Fig. 8 that if the phase angle compensation is not done, the PLL output will have a phase shift introduced due to the multiple angle additions due to the relative acceleration till the harmonics is confirmed. The result also shows the condition with the compenstion added.

4) Case4: Extreme Conditions: A simulation excercise to evaluate the proposed PLL in case of extreme conditions is also carried out. Three conditions have been considered. A condition where single faulting happens is taken initailly. From Fig. 9a, it can be seen that in case of a phase outing also, the proposed PLL sails through generating the required reference. Single phasing is a case of extreme unbalance and the same logic for the unbalance case is activated here also. In Fig 9b, the multiple condition of single phasing and phasejump is taken. Here also it can be seen that the proposed PLL addresses both the conditions and generates a clean reference for the converter. The condition where an unbalance is occuring as well as the presence of harmonics is also analysed. The unbalance indicator deactivates the angular addition where as the harmonic indicator is activated after a couple of cycles only. It can be seen that once the harmoinc indicator is activated, the compensation is added and the PLL

generates the required reference waveform.

5) Experimental results: A few experimental results are also presented for the proposed PLL. In Fig 10a, the case of unbalance is shown. It is to be noted that only one phase volatge is shown. The phase shown undergoes a magnitude change as indicated in the result. The other phases continue to remain at the same peak magnitude which results in an unbalance. This can be seen from the v_q waveform. As soon as the unbalance ocurs, the unbalance indicator (UBI) goes to 1 and decativates the acceleration indicator which prevents the addition of the acceleration angle to the PLL. The PLL can be seen to be generating a clean reference. The case of phase jump is shown in Fig 10b. It can be seen that at a particular instant the phase voltage undergoes a jump of 180 degrees. The phase jump is immediately addressed by the proposed PLL to generate the clean reference.

IV. Conclusion

A simple indicator based PLL was proposed in the paper. The proposed algorithm indicates the presence of phase jumps, unbalance or harmonics in the grid voltage. Based on these indications, instantaneous angluar additions to the SRF PLL arising due to the relative acceleration between the grid space vector and the existing $d-q$ frame due to the above said conditions are enabled or disabled. The proposed algothim thus achieves the objective of instantaneous response to phase jumps and distortionless performance in the case of unbalance and harmonic conditions existing in the grid. The presented algorithm doesnt make us of any explicit filtering techniques and is simple to implement. At the same it achieves a performance comparable to those techniques. The proposed algorithm is validated with sufficient simulation results.

V. Acknowledgement

This research is based upon work supported by the Department of Science and Technology (DST), India, for the project entitled UK India Clean Energy Research Institute (UKICERI) (Sanction No. DST/RCUK/JVCCE/2015/02).

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