e-Battery for Energy Storage Systems

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***Abstract*—This paper presents the concept of electronic battery (e-Battery) for energy storage systems. The proposed e-Battery is a combination of ultra capacitor bank and power electronic converters. This paper looks at issues related to chemical batteries and proposes the concept of an e-Battery. The proposed e-Battery overcomes many of the drawbacks of a conventional chemical battery. The control strategy developed for the closed loop operation of the proposed e-Battery is also presented in this paper. The performance of the proposed e-Battery is verified through detailed time domain simulation in PSCAD/EMTDC. A hardware prototype is built to validate the performance of the proposed e-Battery experimentally.**

***Index Terms*—Battery, electric vehicle, energy storage, ultra capacitor**

I. Introduction

Batteries have been traditionally used as energy storage systems in various applications that include uninterruptible power supplies (UPS) [1], photo voltaic systems [2], electric and hybrid electric vehicles [3], [4] and micro grids [5]–[7]. But batteries have certain disadvantages which include lower power densities, finite depth of discharge, longer charge and discharge times, incapability of handling surge currents and less number of life cycles.

Ultra capacitors can overcome all the disadvantages mentioned above. Based on data sheets, a 500F, 16V ultra capacitor [8] is compared with a 12 V, 7Ah battery [9] in terms of various parameters and the performance specifications are listed in TABLE I. It can be observed that ultra capacitors indicate significantly better values for the parameters with respect to chemical batteries. These include higher power densities, high peak discharge currents, low values of equivalent series resistance (ESR), more number of life cycles, longer shelf life and wider operating temperatures. Therefore, ultra capacitors show much promise in being considered as energy buffers for the proposed e-Battery solution. Thus, ultra capacitors are proposed as a possible solution to energy storage that overcomes many of the disadvantages of a chemical battery.

Ultra capacitors cannot be directly interfaced to the dc-link point of the power circuit. They need to be appropriately interfaced for voltage compatibility. Ultra capacitors are available as low voltage modules, and it is very desirable to have a non-isolated very high gain dc-dc converter to match the low voltage ultra capacitors to the high voltage dc link. This gain requirement may be in excess of 20 in many applications.

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TABLE I
COMPARISON OF ULTRA CAPACITOR(UC) WITH A BATTERY

Parameter	Units	Battery	UC
Voltage rating	V	12	16
Power density	kW/kg	0.26	2.6
Energy density	Wh/kg	31.7	2.9
Peak discharge current	A	75	2000
ESR	mΩ	25	1.9
Life cycles	-	1,000	10,00,000
Shelf life	years	1	2
Operating temperature	°C	-15 to 60	-40 to 65

Traditional converters will not be able to achieve this without the help of an isolation transformer. However, it is desirable to avoid the isolation transformer from cost, size and efficiency points of view. High gain dc-dc converter topology [10] is used as a part of the proposed e-Battery solution.

Another issue that will crop up is the series and parallel connection of batteries that may become necessary to achieve required capacity for the applications. Charge equalization circuits for series connection and interface circuits for parallel operation of even eutectic combination of energy buffers is proposed as part of the e-Battery solution.

The control strategies developed for the high gain converter, series and parallel charge equalisation circuits are also presented in this paper.

The paper is organised as follows. Section II discusses about the concept of e-Battery including the description of high gain DC-DC converter, series and parallel charge equalisation circuits. The control strategy for the closed loop operation is discussed in section III. Simulation and experimental results of the proposed e-Battery are presented in section IV to validate the performance of the proposed e-Battery and the paper is finally concluded in section V.

II. Proposed e-Battery

Fig. 1 shows the topology of the proposed e-Battery that consists of ultra capacitor bank cascaded with high gain DC-DC converter [10]. Ultra capacitor bank is realized using series and parallel combination of ultra capacitors. Each string consists of 'm' capacitors in series and 'n' such strings are connected in parallel. Since ultra capacitors are available in smaller voltage ratings, a series combination is used to increase the voltage rating and parallel combination of series strings is used to increase the capacitance of the overall bank.

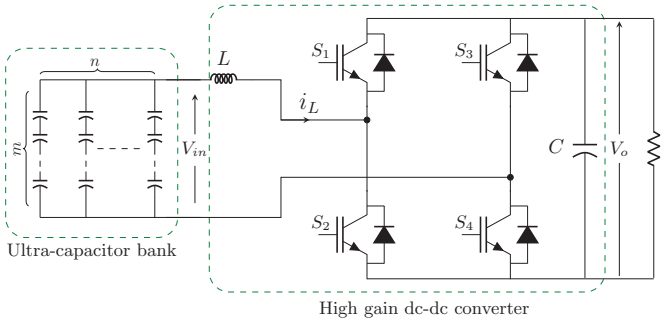

Fig. 1. Configuration of the proposed e-Battery

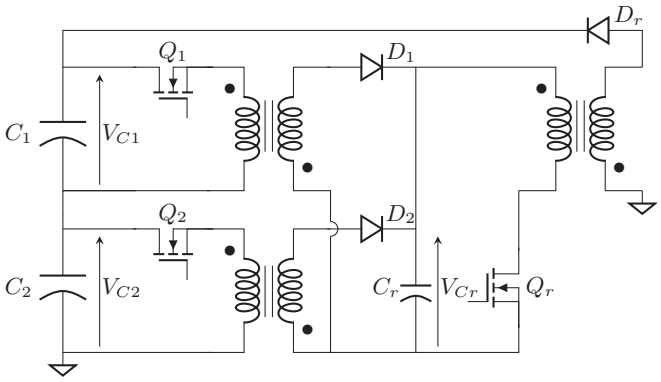

Fig. 2. Series charge equalization circuit

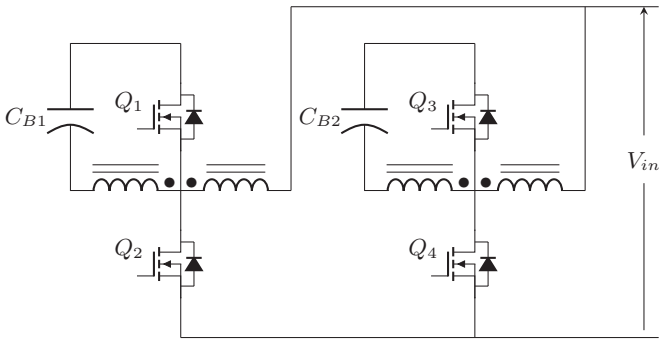

Fig. 3. Paralleling of ultra capacitor strings

A. High gain Converter

High voltage gain bi-directional DC-DC converter proposed in [10] is used as it results in the lesser value of ultra capacitor bank voltage (V_{in}), thus making the ultra capacitor bank compact in size. The high gain converter consists of two half bridges. Series combination of ultra capacitor bank voltage (V_{in}) and inductor (L) is connected across the midpoints of both the legs. Output capacitor and load resistance are represented by C and R respectively.

The converter pumps power to the load from ultra capacitor bank when the switches S_2 and S_3 are turned on for dT_s duration. Here d and T_s represent the duty of operation and switching time period respectively. During (1-d)T_s duration, switches S_2 and S_3 are turned off, which allows the inductor to freewheel through the body diodes of switches S_1 and S_4. By controlling the switches S_2 and S_3, the converter is made to pump the power back into the ultra capacitor bank.

The ideal voltage gain expression for the high gain converter is given as

$$\frac{V_o}{V_{in}} = \frac{1}{(1-2d)} \tag{1}$$

It is seen from (1) that the converter provides high gains when operated at duty ratios close to 0.5. However the practical gain of the converter reduces from its ideal value due to non-idealities [10].

B. Series charge equalization

When a number of ultra capacitors are connected in series, there can be unbalance in the voltages of ultra capacitors due to different internal parameters of each ultra capacitor. This can result in unequal charge distribution and also sometimes in the degradation of ultra capacitors. Hence series charge equalization circuit [11], is employed as shown in Fig. 2. The equalization circuit is shown for two ultra capacitors C_1 and C_2 and the circuit can be generalized for any number of ultra capacitors.

The capacitors C_1 and C_2 are connected as inputs to two flyback converters, with their corresponding switches as Q_1 and Q_2 respectively. The output diodes D_1 and D_2 of both the flyback converters is connected to a reservoir capacitor (C_r), which is connected to another flyback converter. The output diode D_r of this converter is connected to the main ultra capacitor bank.

C. Paralleling of ultra capacitor strings

When a number of ultra capacitor strings are in parallel, there can be circulating currents due to mismatch between voltages of each of the strings. To overcome this issue, parallel interface circuit as shown in Fig. 3 is used [12]. Ultra capacitor strings of different voltages also can be interfaced to the same dc link using this circuit.

The topology in Fig. 3 is shown for two ultra capacitor strings with their equivalent capacitances represented as C_{B1} and C_{B2}. It has two flyback converters, both connected to the same DC link. Each converter consists of two bi-directional switches.

III. Control Strategy

A. Control strategy for Series Charge Equalization

The control block diagram for series charge equalization of ultra capacitors is shown in Fig. 4. V_{Ci} represents the i^{th} capacitor voltage for i = 1,2,....,m where 'm' denotes the number of series ultra capacitors present in each string. V_{avg} represents the average of these ultra capacitor voltages which is given by

$$V_{avg} = \frac{V_{C1} + V_{C2} + ... + V_{Cm}}{m} \tag{2}$$

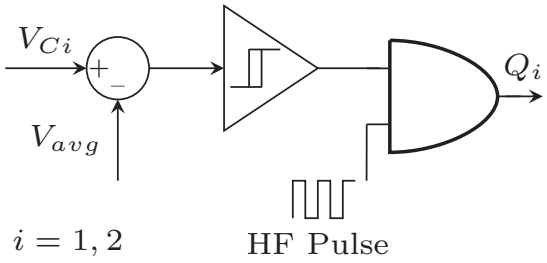

Fig. 4. Control of individual ultra capacitor voltage (V_{Ci}) in the series charge equalization circuit

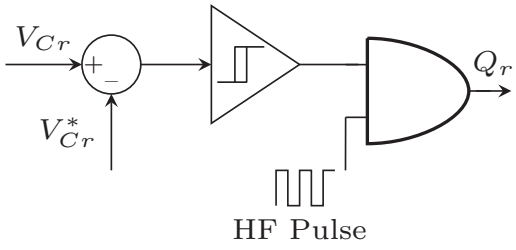

Fig. 5. Control of reservoir capacitor voltage (V_{Cr}) in the series charge equalization circuit

V_{Ci} is compared with V_{avg} and the difference is passed through hysteresis comparator. The output of comparator and high frequency pulses (HF pulses) of 50% duty ratio are passed through AND gate, whose output is given to the gate drive of i^{th} switch (Q_i). Thus, when $V_{C_1} > V_{avg}$, Q_1 is turned on. This removes the excess charge from C_1 and puts into reservoir capacitor (C_r). Similarly when $V_{C_2} > V_{avg}$, Q_2 is turned on to put the excess charge into C_r.

Thus, all the excess charge removed due to the unbalances created in each of the ultra capacitor voltages will be dumped into the reservoir capacitor. The control block diagram for reservoir capacitor is shown in Fig. 5. When the voltage of reservoir capacitor (V_{Cr}) reaches a set reference value (V^*_{Cr}), Q_r is turned on to remove excess charge from C_r and put it back into ultra capacitor bank.

B. Control strategy for Parallel Charge Equalization

The parallel combination of two ultra capacitor strings is shown in Fig. 3. For the forward power flow (i.e., from C_{B1} or C_{B2} to V_{in}), switches Q_1 and Q_3 are turned ON while the switches Q_2 and Q_4 are turned OFF. For the reverse power flow (i.e., from V_{in} to C_{B1} or C_{B2}), switches Q_2 and Q_4 are turned ON while the switches Q_1 and Q_3 are turned OFF. The duty ratio of the switches can be varied to adjust the power flow [12].

C. Control strategy for e-Battery

The closed loop block diagram of the proposed e-Battery is shown in Fig. 7. It consists of an outer voltage loop to control the DC link voltage (V_o) and an inner current loop to control the inductor current (i_L).

The DC link voltage (V_o) of the output capacitor (C) is compared with reference (V^*_o). The error is passed through PI controller to generate current reference for inductor current (i^*_L), which is compared with the actual inductor current (i_L) to produce current error. This error is passed through PI controller to generate the modulating signal (m). This is compared with triangular carrier to produce required duty ratio (d) for the closed loop operation. This duty d is given to the switches S_2 and S_3 of the high gain converter.

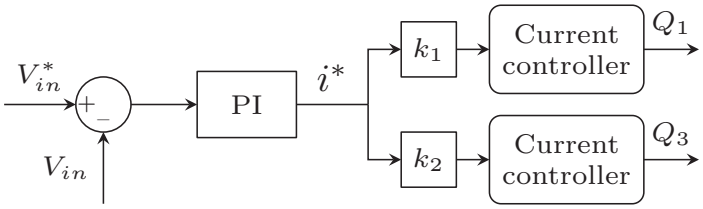

Fig. 6. Control block diagram for the paralleling of ultra capacitor strings

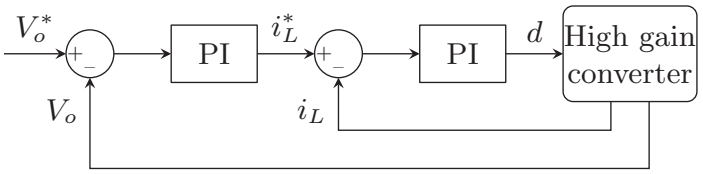

Fig. 7. Block diagram showing the closed loop control of e-Battery

IV. Results and discussion

A. Simulation Results

To verify the performance of e-Battery, a detailed time domain analysis is carried out. The following cases were simulated to verify the performance of e-Battery.

1) Charge equalization: The circuit given in Fig. 2 is modelled. To create an unbalance between the impedance of two capacitors, a parallel resistor of 50 Ω is connected across capacitor C_2. The voltage across the two capacitors are shown in Fig. 8. At t = 5 sec, the charge balance algorithm is disabled and enabled back at t = 5.3 sec. From the figure it is clear that, till t = 5 sec, the voltage across the two capacitors were same, and when the algorithm is disabled, the two voltages diverge. It is also seen that the two voltages converge at t = 5.3 sec, when the charge balancing algorithm is re-enabled.

2) Transient performance: In order to show the power density of ultra capacitor, the circuit given in Fig 1, is simulated. At t = 0.4 sec, the load connected to the e-Battery is doubled. The sudden loading results in a dip in the DC link voltage. Since the ultra capacitor has high power density, the demanded current is delivered within few milliseconds as shown in Fig. 9.

B. Experimental Results

A hardware prototype is built to verify the performance of charge equalization circuit and high gain DC -DC converter.

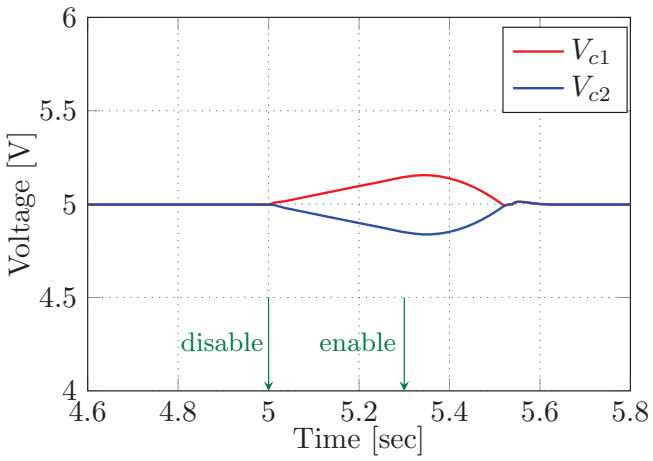

Fig. 8. Simulation results showing the operation of series charge equalization circuit.

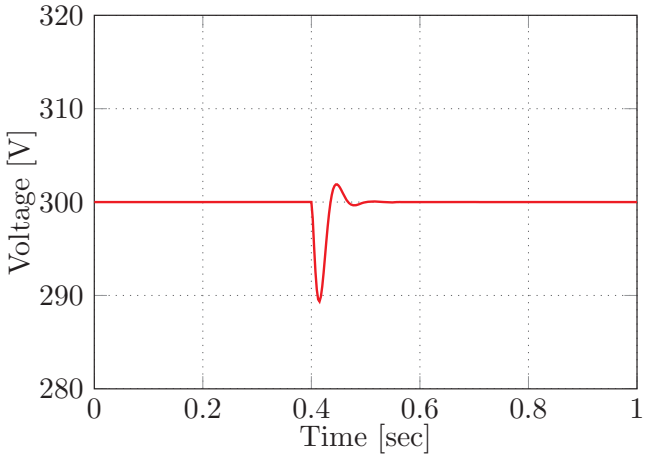

Fig. 9. Simulation results showing the transient response of the proposed e-Battery system to sudden load change

The control algorithm is implemented on TMS320F28335 DSP. The converter is switched at a frequency of 10 kHz. The switches in the proposed e-Battery system are realized using three half bridge IGBT modules (SKM100GB128D).

Fig. 10 shows the effectiveness of charge equalization control. Fig. 11 shows the variation of output voltage (V_o) for a step change in duty cycle from d = 0.3 to d = 0.475. The input voltage considered is 10 V. A gain of 10 is achieved with this converter topology when operated at a duty ratio of 0.75. The gain achieved is less than the ideal gain due to the non-idealities of the converter.

V. Conclusion

This paper presents the concept of e-Battery. The proposed e-Battery can over come most of the disadvantages of conventional chemical batteries. The high gain converter employed can make ultra capacitor bank compact, thereby

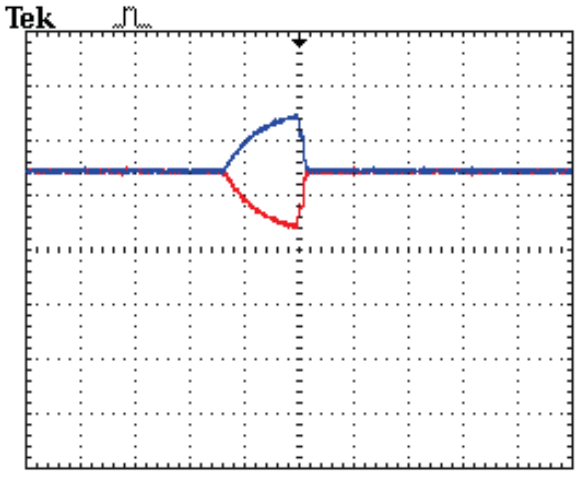

Fig. 10. Experimental results showing the operation of series charge equalization circuit where blue trace indicates voltage of capacitor C_1 (V_{C1} : 5 V/div) and red trace indicates voltage of capacitor C_2 (V_{C2} : 5 V/div) ; time scale : 100 ms/div.

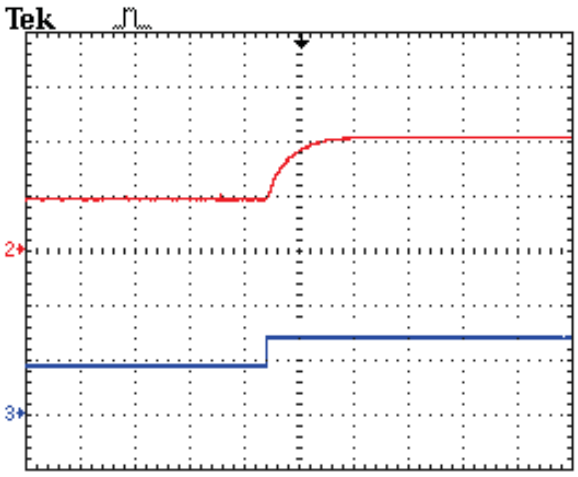

Fig. 11. Experimental results showing the operation of high gain converter where red trace indicates output voltage (V_o : 50 V/div) and blue trace indicates duty ratio (d : 0.33/div) ; time scale : 250 ms/div.

resulting in higher volumetric efficiency of the ultra capacitor bank. Series and parallel charge equalisation circuits which are part of the proposed e-Battery system are presented along with their closed loop control strategies. Detailed time domain simulations are performed to verify the power handling capability of e-Battery for sudden changes in load. The high gain converter and charge equalization circuits are also verified through experimental results.

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