Design and Performance Evaluation of a General Purpose Device Characterization Setup

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***Abstract*—Semiconductor switches of distinct underlying device technologies but with identical ratings are commercially available from a range of manufacturers. Selection of appropriate device for a given power conversion application is critical for meeting the trade-off between cost and performance objectives. This paper discusses the design of a PCB based general purpose discrete device characterization setup using which comparative study of switching and short-circuit behavior of TO-247 devices is performed at room and elevated case temperatures in the range from 120°C to 160°C . The design ensures that the test fixture safely handles the abnormal levels of current stress occurring in the event of a catastrophic device failure. Experimental studies conducted on 1200V, 40A silicon (Si) and 1200V, 50A silicon carbide (SiC) devices from varied manufacturers verify the performance of the characterization setup. The distinctions in their respective switching behavior at nominal and fault conditions, along with the deviations in their characteristics observed at elevated operating temperatures are reported in this work.**

***Keywords*—Double Pulse Test, Short circuit test, Device Characterization, Heat Spreader.**

I. Introduction

Insulated Gate Bipolar Transistors (IGBTs) are widely used in medium and high power applications due to its superior performance at higher voltages and currents [1]. Choice of IGBT for a given application becomes easier when a comparative study is performed on similar rated competing devices of distinct technologies from varied manufacturers. Double-pulse (DP) and short-circuit (SC) tests are standard characterization tests performed on semiconductor switches [2]–[7].

In [5], [6] device characterization setup is discussed for module based silicon (Si) and silicon carbide (SiC) switches. While a PCB based approach for discrete device characterization is discussed in [2]–[4]. Static and dynamic performance evaluation of parallel connected Si IGBT and SiC MOSFET are presented in [8], [9]. [10] compared the switching characteristics of SiC MOSFET with Si-IGBT in various dc-dc converter topologies. It is important to study the deviations in device switching characteristics with temperature variation [11] and compare the same with loss budget calculation.

Also, it is important to design a system that can reliably function as a characterization setup while handling a catastrophic switch and/or board failure during the tests. Hence, passives design, PCB design and layout aspects need to be factored in during the design stage.

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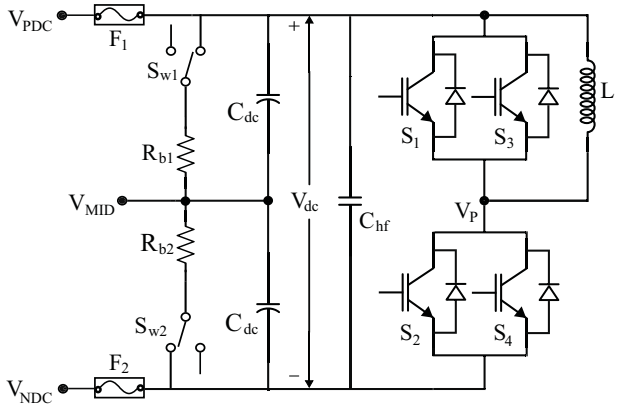


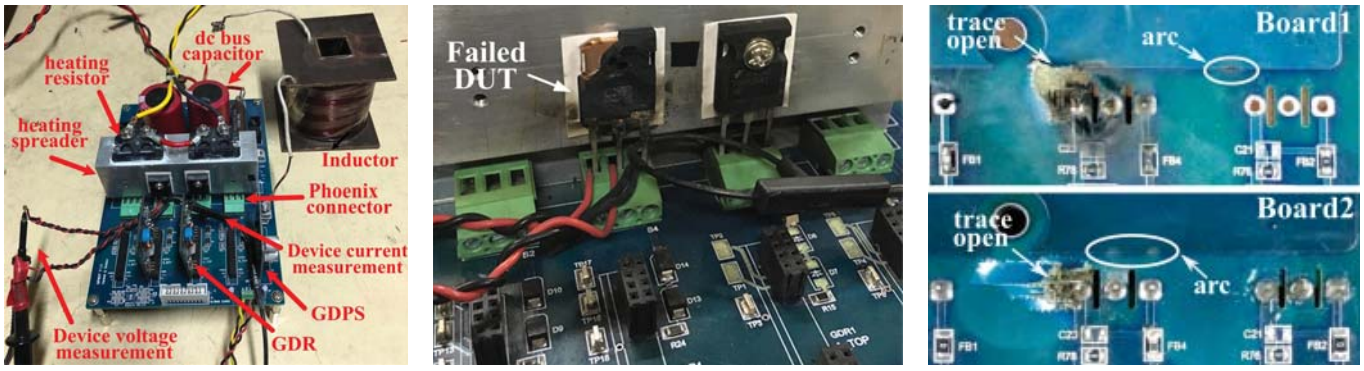
Fig. 1: GPDCS circuit schematic

In this paper, the design of a PCB based general purpose setup is discussed for TO-247 package based semiconductor device characterization at desired operating case temperatures. A heat spreader design and characterization method is presented that facilitates tests at elevated temperatures. The PCB based design although carries minimal circuit parasitics, also inherently carries the risk of a catastrophic circuit board failure in the event of a device failure which can happen in practice especially during elevated temperature tests, for which the underlying mechanism is explained in this paper.

Section II provides a brief description of the General Purpose Device Characterization Setup (GPDCS) that is suitable for studying both Si and SiC discrete devices. Section III describes the GPDCS design and Section IV presents the experimental results that compare 1200V, 40A device characteristics from different manufacturers at elevated temperatures, for recommended operating conditions and gate resistance.

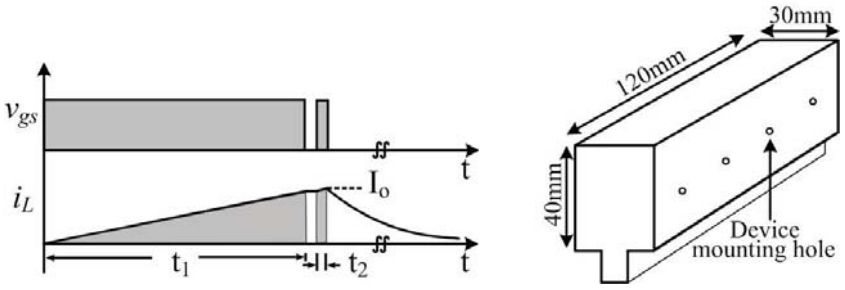
II. Description of GPDCS Circuit

The GPDCS is a half bridge inverter leg mounted on the heat spreader (HS), as shown in Fig. 1. Heating resistors are mounted on the HS that enable setting of the HS temperature to the desired value prior to the test. The top and bottom devices comprise of two switches in parallel, which not only facilitates study of parallel IGBT operation, but also enables carrying out Type-II short-circuit test under load for fault characterization [12]. TI 28377S based digital controller along with opto-isolated gate drivers (GDR) [13] are employed to drive the devices. The device current is measured using a Rogowski PEM CWT1 Ultra Mini current probe [14], and device voltages are measured by passive probes [15] with a twisted wire pair arrangement, as shown in Fig. 2(a). Double-pulse test



(a) (b) (c)

Fig. 2: (a) Experimental setup of the GPDCS (b) Catastrophic device failure due to thermal overstress and (c) corresponding PCB failure



(a) (b)

Fig. 3: (a) DP test waveforms and (b) HS geometry

TABLE I: GPDCS System Ratings

Item	Value
Max dc voltage V_{dc}	800 V
Max load current I_o	50 A
Voltage dip ΔV	16 V (2%)
Current rise ΔI	2.5 A (5%)
1^{st} pulse t_1	(0 - 125) μs
2^{nd} pulse t_2	5 μs
Load inductor L	2 mH
dc capacitor C_{dc}	235 μF
R_{ESR}	50 mΩ
R_{trace}	2 $m\Omega$

along with Type-I short-circuit tests have been conducted at 800V, 40A and at temperatures 25°C, 125°C and 155°C. The setup can also be utilized to obtain safe operating area (SOA) characterization.

III. GPDCS Design

Double-pulse test is performed on the bottom device forming the device under test (DUT) and the top device is treated as free-wheeling diode (FWD). DP test is carried out with only the on-board dc capacitors C_{dc} that are pre-charged to the desired voltage level V_{dc}. As can be seen from Fig. 2(a), the device is mounted on HS through SIL pad as thermal interface material on a Phoenix connector with minimal parasitic inductance insertion. The advantage of using such connector is that the device need not be soldered and the device can be changed as the need be. The first pulse t_1 allows the load inductor L to attain the desired current level followed by the second pulse t_2 where characterization is performed.

A. Load Inductor and dc Capacitor Design

The inductor value is chosen such that only 5% current rise ΔI is permitted during t_2 as shown in Fig. 3(a), while capacitor design is based on 2% voltage dip ΔV caused by charge transfer during the entire test period. For a dc-bus voltage V_{dc} = 800V and load current I_o = 50A, inductance L and capacitance C_{dc} are calculated as,

$$L = \frac{V_{dc} t_2}{\Delta I} \Rightarrow L = 2\ mH \quad (1)$$

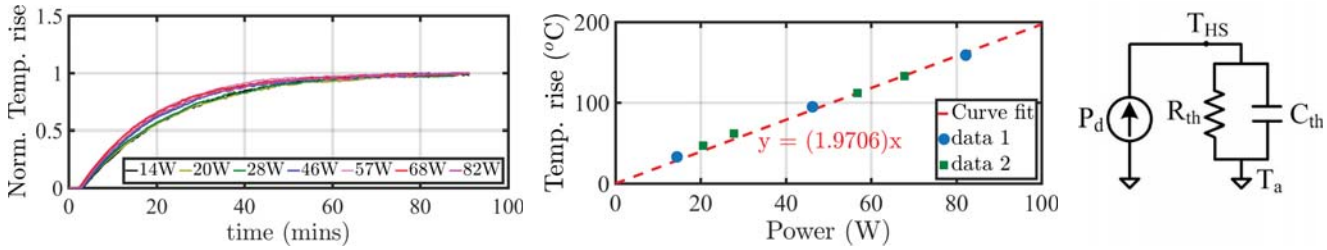
$$\Delta Q = \frac{1}{2} I_o (t_1 + 2t_2) \ \Rightarrow \ C_{dc} = \frac{\Delta Q}{\Delta V} \ = 210\ \mu F \quad (2)$$

B. Heat Spreader Design

The profile of the heat spreader HS is shown in Fig. 3(b). HS is designed such that it is devoid of fins. An external heat source such as heating resistors, as indicated in Fig. 2(a), are employed to raise the HS temperature as well as that of device case to desired value. Two heating resistors, each of value 10Ω connected in series, are powered by a bench top power supply with a variable current limit. The maximum temperature that the HS can attain is 160°C from ambient for a current range of 0-2A. The temperature is measured using thermal imager and no heat sensor is mounted.

The thermal impedance of HS is found experimentally by passing appropriate currents through the heating resistors for different levels of power dissipation. Fig. 4(a) shows the measured normalized temperature rise of HS. From this curve the thermal time constant of system τ = 22min is obtained. Fig. 4(b) illustrates the curve fit of temperature rise as a function of power dissipated taking three data points indicated in blue as data1. Four additional experiments are conducted whose temperature rise is indicated in green as data2. It can be seen that experimental data in data2 lies closely to the value predicted by the curvefit equation. From slope of this curve, the thermal resistance of HS R_{th} = 1.97 °C/W is obtained. The thermal capacity of this design is found to be $C_{th} = \tau / R_{th}$ = 660 J/°C. Adequate thermal capacity is maintained so that the HS temperature does not vary during DP and SC tests.

The thermal model of HS based on the electrical equivalent circuit is as shown in Fig. 4(c). Using this, a first order transfer function model of the HS is obtained which is given as



(a) (b) (c)

Fig. 4: HS characterization showing (a) normalized temperature rise wrt time, (b) temperature rise as a function of power dissipated in HS and (c) thermal equivalent circuit model

$$G_p = \frac{\Delta T}{P_d} = \frac{R_{th}}{(1 + sR_{th}C_{th})} \tag{3}$$

where P_d is the power dissipated in the heating resistors and $\Delta T = T_{HS} - T_a$ is the temperature rise of HS from ambient. (3) serves as the plant transfer function that facilitates the design of a closed loop temperature control for the system. The time domain equation of temperature rise of the system is given by [16]

$$\Delta T = P_d R_{th}(1 - e^{-t/\tau}) \approx \frac{P_d t}{C_{th}} \tag{4}$$

Since DP and SC durations are extremely small, in the order of few 100μs, (4) is simplified and approximated. It is clear that temperature of HS is almost constant owing to its large thermal capacity. This ensures that the effect of HS can be ignored in transient thermal model analysis to estimate device junction temperature for SC test conditions.

C. PCB Design

The energy involved in the device characterization using DP and SC tests is typically minimal. Hence PCB trace thickness and width are significantly reduced as compared to a general inverter board design, which minimizes setup parasitic inductance. A device failure in the circuit can occur due to puncturing of junction caused by an over voltage application, or by fusing of junction due to over temperature caused by excess power dissipation. In either case, at the outset the device fails as a short, and this results in the dc-bus shoot through fault. The resulting over current causes a catastrophic device destruction as shown in Fig. 2(b), following which the device fails as open. When such a large fault current is interrupted by the opening up of the device, an arc is formed across the device and the PCB layers that tends to sustain the fault current. This subsequently results in disastrous board failure due to opening up of the PCB traces as shown in Fig. 2(c) rendering it inoperable. It is desirable not to damage the test fixture even during device characterization at elevated temperatures in the event of a device failure. Hence the PCB must be designed to handle the large fault current i_f caused by a dc-bus shoot through for the fault duration t_f. During this event, the current is limited only by the ESR of the electrolytic capacitors R_{ESR} and trace resistance R_{trace}. The effective resistance that restricts the high current is $R_{eff} = R_{ESR} + R_{trace}$. The corresponding Joule Integral of the dc-bus capacitor JI_{cap} for a duration t_f is given by,

$$E_{cap} = \frac{1}{2}C_{dc}V^2 = \int_0^{t_f} {i_f}^2 R_{eff} dt$$

$$\Rightarrow \int_0^{t_f} {i_f}^2 dt = JI_{cap} = \frac{E_{cap}}{R_{eff}} = 1504\ A^2s \tag{5}$$

The PCB traces must be designed such that the Joule Integral of traces JI_{pcb} is greater than the calculated JI_{cap} value, to prevent the catastrophic PCB failure. Assuming a 50% margin, the PCB trace width t_w for a layer thickness t_t of 35μm, and ratings indicated in Table. I is given by following [17],

$$JI_{pcb} = 1.5 \times 1504 = 2256\ A^2s$$

$$\Rightarrow\ t_w = \frac{1}{t_t}\sqrt{\frac{\rho JI_{pcb}}{\Delta T K_d K_c}} = 3\ mm. \tag{6}$$

where ρ, K_c and K_d are resistivity, specific heat and density of copper respectively and ΔT is the melting temperature-rise for copper. This indicates that a minimum of 3 mm trace width is required in the single layer PCB for sustaining a device failure.

D. Implications of inverter PCB design

The maximum value of trace width that is practically feasible on single PCB layer for TO-247 discrete device leads is 3 mm due to physical space constraint on the board. In practical inverters, a higher value of dc capacitance than (2) may be used. For higher reliability, film capacitors with inherently lower ESR values may be used in the dc-bus instead of electrolytic capacitors. In these scenarios, the resultant JI_{cap} value would be larger than (5) and can invariably lead to a PCB board failure as shown in Fig. 2(c). To prevent such a board failure, a greater copper layer thickness or a multi-layer PCB connection must be employed for device leads to ensure larger JI_{pcb} and design robustness.

IV. Experimental Results

Fig. 2(a) shows the experimental setup consisting of GPDCS circuit, heat spreader, device voltage measurements with twisted-wire pair and current measurement with Rogowski PEM Ultra Mini current probe. GPDCS being a versatile setup serves a variety of functions such as,

1) Double-pulse switching characterization of TO-247 package semiconductor devices of identical ratings at any desired case temperature.
2) Short-circuit device characterization at any desired case temperature.
3) Switching characteristics study for changes in gate-circuit components such as gate-resistors, ferrite beads, and gate-capacitors.
4) Device paralleling study and effect on switching performance.
5) Performance evaluation of thermal interface materials.

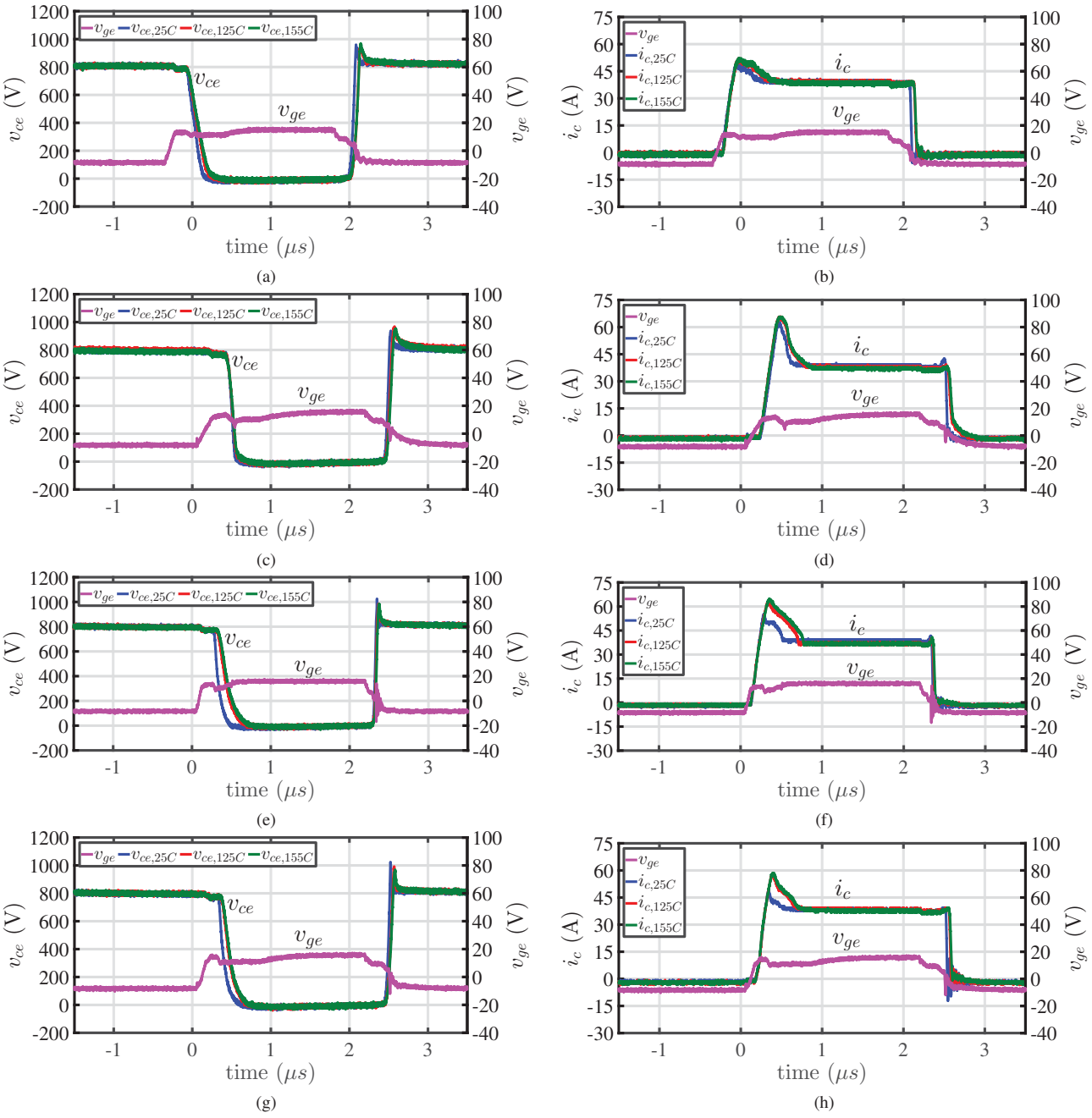


Fig. 5: Turn-on characteristics of Si IGBTs from different manufacturers and their deviations at elevated temperatures upto 155°C at the case showing (a),(b) v_{ce}, i_c of Si-T1 (c),(d) v_{ce}, i_c of Si-T2 (e),(f) v_{ce}, i_c of Si-T3 (g),(h) v_{ce}, i_c of Si-T4.

A. Double Pulse test on Si devices

Si IGBTs of identical rating of 1200V, 40A namely Si-T1, Si-T2, Si-T3 and Si-T4 are studied. These devices are of distinct device technologies such as *Field Stop Trench, 3rd Gen Trench Stop* and from different manufacturers like *Infineon, Toshiba, Rohm, Fairchild, STMicroelectronics, IXYS, Cree, ON Semiconductor*.

In typical inverter applications, the top and bottom switches of inverter leg are packaged with the same device. Hence, comparison of the device performance with its default co-pack diode as FWD is crucial. Fig. 5 shows the turn-on and turn-off characteristics of Si device voltage and current at 25°C, 125°C and 155°C during t_2 of the DP test. It can be seen that, all devices exhibit current overshoot during turn-on, due to reverse recovery charge Q_{rr} of FWD. But, Si-T1 exhibits lowest current overshoot and has minimal deviation in behavior with temperature variation as compared to other devices.

The corresponding measured values of Q_{rr} and its deviation for the four Si devices are tabulated in Table.II. It can be observed that, percentage increase in Q_{rr} charge is minimum in Si-T4 and is comparable with Si-T1. It can be observed that the total Q_{rr} change is 0.6-2.6 times from 25°C and 125°C.

TABLE II: Comparison of reverse recovery performance in Si IGBTs from different device manufacturers

Si IGBT	Q_{rr} (μC)			Change in Q_{rr} (%)		Energy loss E_{rr} (mJ)			Turn-on energy loss E_{on} (mJ)			$\%E_{rr}$ in E_{on}		
	$T_{c,a}$	$T_{c,125}$	$T_{c,155}$	$T_{c,125}$-$T_{c,a}$	$T_{c,155}$-$T_{c,125}$	$T_{c,a}$	$T_{c,125}$	$T_{c,155}$	$T_{c,a}$	$T_{c,125}$	$T_{c,155}$	$T_{c,a}$	$T_{c,125}$	$T_{c,155}$
1	1.9	3.4	4.5	73.4	32.3	0.7	1.2	1.4	6.7	8.3	8.8	1	1.4	1.6
2	3.3	7.4	8.8	123	18.4	0.9	2.8	3.4	5.7	10.3	11.5	1.6	2.8	3
3	1.1	3.9	4.8	263	23	0.4	1.6	2	5.1	12.2	9	0.9	1.3	2.2
4	4.1	6.6	7.2	62.6	8.8	1.5	2.2	2.4	7	8.2	8.6	2.1	2.7	2.8

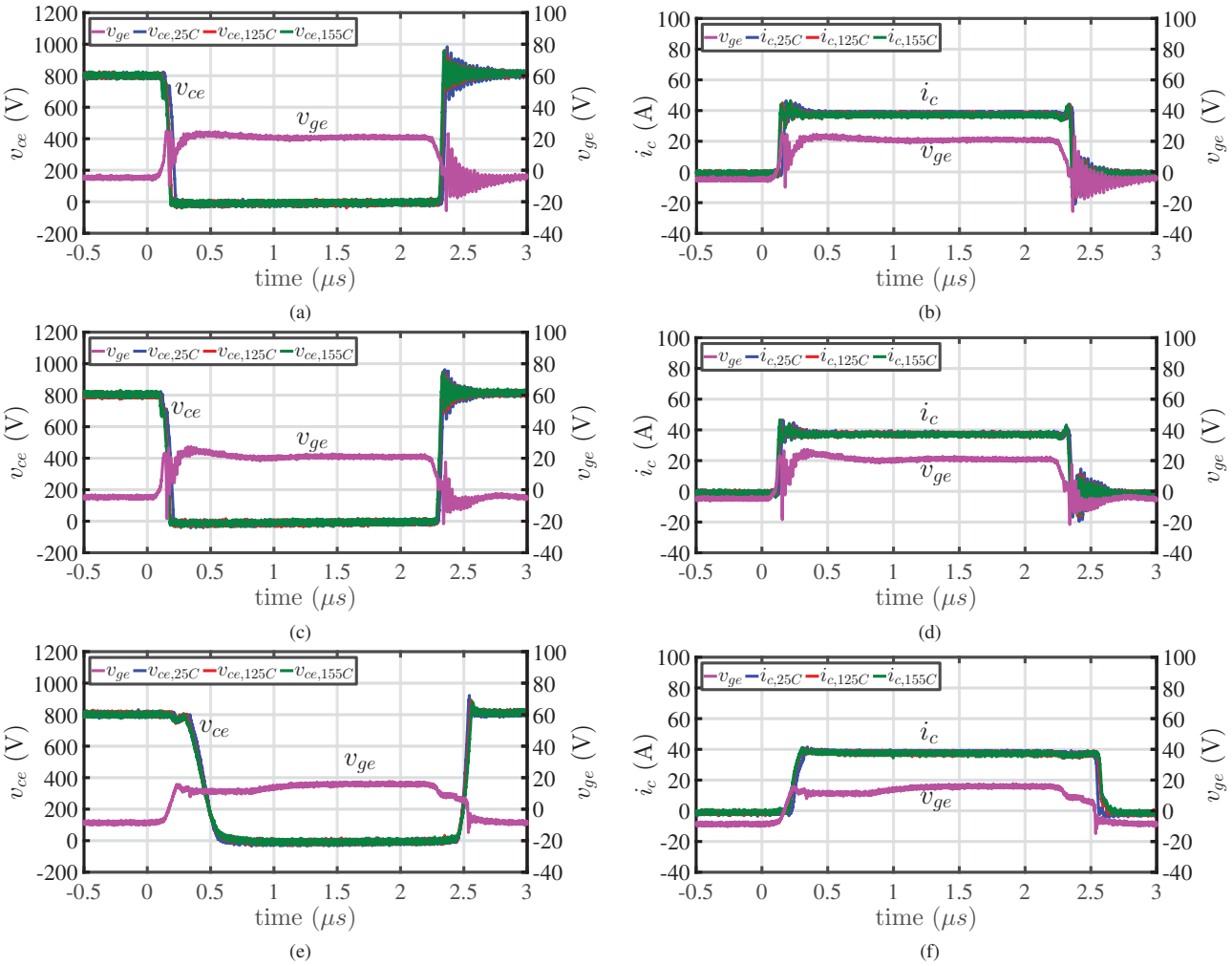


Fig. 6: Double Pulse switching characteristics of SiC MOSFETs with diodes from different manufactures and their deviations at elevated temperatures upto 155°C at the case showing (a),(b) v_{ce}, i_c of SiC-T1 and SiC-D1 (c),(d) v_{ce}, i_c of SiC-T2 and SiC-D1 (e),(f) v_{ce}, i_c of Si-T1 and SiC-D1.

However, the corresponding increase from 125°C to 155°C is in the range of 0.08-0.32.

The energy loss due to reverse recovery E_{rr}, total device turn-on energy loss E_{on} and E_{rr} as a percentage of E_{on} are also compared in Table.II. Minimum increase in reverse recovery energy loss is observed in Si-T4. However, in terms of total energy loss value, Si-T1 and Si-T3 are comparable. Additionally it can be noticed that, minimal ringing oscillations in device voltage and current validates the tight layout achieved in the PCB design.

B. Double Pulse test on SiC devices

Fig. 6(a),(b) and (c),(d) show the switching characteristics of two identically rated 1200V, 50A SiC MOSFETs from different manufacturers, SiC-T1 and SiC-T2, with a discrete SiC diode SiC-D1 functioning as FWD. It can be seen that SiC MOSFETs switch much faster and exhibit greater levels of ringing oscillations as compared to Si devices. It can be noticed that SiC-T2 performes relatively better in terms of both ringing oscillations magnitude in device voltage and the ringing duration.

C. DP test on combination of Si-SiC devices

Fig. 6(e),(f) is the experimental result of DP test conducted with Si-T1 as DUT and SiC-D1 as FWD. The reverse recovery Q_{rr} observed in Fig. 5(b) is almost absent with a discrete SiC diode which results in lower energy loss. Thus, such a combination of devices yield better power converter efficiency

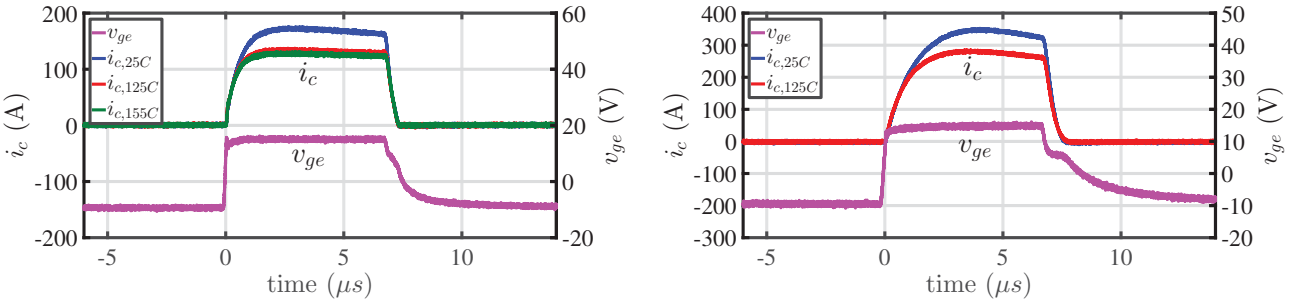


Fig. 7: Type-I short-circuit characteristics and its deviation at elevated temperatures showing (a) Si-T1 (b) Si-T2 devices.

in high frequency hard switched DC-DC applications.

D. Type-I short circuit test on Si devices

In terms of short circut performance, while Si-T1 and Si-T2 are rated for 10μs short circuit withstand capability, Si-T3 and Si-T4 are rated for only 5μs. Hence, Type-I SC experiment is conducted only on Si-T1 and Si-T2 at elevated temperatures as shown in Fig. 7. It can be observed that the short circuit current value decreases at elevated temperatures. This is due to the reduction of transconductance g_m of the device at higher temperatures [18]. It can be seen in Fig. 7(a) that Si-T1 sustains SC for 8μs even when the case temperature is at 155°C while Si-T2 is unable to withstand SC current and results in a catastrophic thermal failure such as the case shown in Fig. 2(b). SOA characteristics of the device can be obtained by plotting i_c with respect to v_{ce}. Such a fault study at elevated temperature is helpful in comparing the robustness of semiconductor devices at extreme operating conditions.

V. Conclusion

This paper presents the design of a PCB based general purpose discrete device characterization setup, using which TO-247 package switches can be studied with double pulse and short-circuit tests at desired operating case temperature. The thermal design of the HS and its characterization method to facilitate elevated temperature tests are explained. The setup can be used to test devices upto an elevated temperature of 160°C. A failure mode of the power PCB of general purpose device characterization setup during elevated temperature tests is presented. The necessary PCB design change to be incorporated to prevent board failures during such tests are outlined. Similar rated Si and SiC device characteristics of different device technologies from various manufacturers are compared experimentally at elevated temperatures, from which reverse recovery charge and the corresponding losses incurred in device are obtained. These tests also bring out the significant variations in ruggedness of the different devices from different manufacturers. Also, same board can be used for different devices. Tests conducted on different combination of power devices verify the performance of the setup and also aid in making appropriate choice for a given power conversion application.

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