Stability Analysis of Phase Locked Loop Controllers for Grid Tied Inverters in Weak Microgrids

Nakul Narayanan K, Shan S, L Umanand
Department of Electronic Systems Engineering
Indian Institute of Science, Bangalore - 560012, India
Email: nakul@iisc.ac.in, shans@iisc.ac.in, lums@iisc.ac.in

***Abstract*—This paper analyses, the effect of the phase locked loop (PLL) controller in the stability of the voltage source converter(VSC) in a microgrid or when connected to a weak AC grid. While designing the controller for PLL, it may not be possible to consider the effect of the load and line impedance as they are not readily known. In a microgrid or in a weak grid, the dynamics of the PLL are affected due to the high impedance nature of the network. A small signal model is built to show how the PLL controller affects the stability of the VSC. A comparison is made between proportional (P) and proportional-integral (PI) controller, using detailed time domain simulation in PSCAD/EMTDC to demonstrate this problem.**

***Index Terms*—PLL, weak grid, microgrid, stability**

I. Introduction

With the increase in power demand all over the world, distributed generations (DG) plays a key role in the electrical power distribution system. These DGs are either connected to the grid at remote locations or they form a local is-landed microgrid. These DGs are generally connected to the electrical networks using VSC. In order to have fast and independent, active and reactive power control, the control of VSC is normally done based on vector control [1], [2]. In vector control, the current injected into the point of common coupling (PCC) is controlled to achieve fast dynamic performance and decoupled control. The injected current is split into two decoupled components which in-turn control active and reactive power independently. In order to decompose the current, the phase information of the grid voltage is needed. Synchronous reference frame (SRF) based PLL is commonly used to get the phase of the PCC voltage [3].

The strength of the AC network where these VSC are connected is represented by short circuit ratio (SCR) as given below,

$$SCR = \frac{V_t^2}{|Z_g|P_{inv}} \tag{1}$$

where V_t is the point of common coupling voltage, Z_g is the network impedance and P_{inv} is the power injected to the PCC by the VSC [4]. For a SCR below 3, the grid is considered to be weak. While designing the PLL in vector control, the strength of the grid (effect of grid impedance) is generally not considered. This is because the grid impedance may not be readily available or it is difficult to measure the grid impedance. In [5]–[9], the effect of the weak grid on the stability of vector control is discussed in detail. The VSC DC transmission limits imposed by the grid impedance and PLL is analysed using time domain simulation in [5]. Further studies has been done in [7], [8] to quantify the effect of SCR and PLL gain on the stability of VSC based high voltage DC transmissions. A PLL model is developed in [9], to consider the non-linear behaviour and the instability of PLL considering the interaction of the VSC current with the grid. The VSC is modelled as a controlled voltage source with an inner current control. However, with the addition of extra control loops like outer power loop, AC voltage control loop, etc. the overall model gets modified.

Several methods have been reported in the literature in order to avoid the stability issue caused due to PLL in VSC when connected to a weak grid. In [10], a feed-forward control method is introduced to suppress the stability issue caused due to PLL. In [11], an ac voltage controller is designed to counter the dynamics occurring due to PLL. A gain scheduling control system design was reported in [12] to enhance the performance of the VSC connected to the weak AC grid. Reshaping the impedance of the VSC has been proposed in [13], [14] to overcome the stability issue of PLL in a weak grid. However, all these methods requires either the information of the grid impedance which may not be readily available or uses complex control structure.

In this paper, a simplified small signal model is built to analyse the effect of the PLL controller on the stability of the overall VSC control system. The model investigates how the PLL is affected by the SCR and the current injection from VSC. The model can be easily extended further to analyse the stability due to the addition of extra control loops. A comparison is made between the proportional and proportional-integral controller to demonstrate the stability of the system including the grid impedance. The analysis is validated through detailed time-domain simulations.

This paper is organized as follows. In section II, a PLL model is developed to show how the PLL dynamics get affected in a weak grid. The selection of the controller structure for PLL is discussed in section III. Section IV discusses the small signal and large signal stability model of the PLL. In section IV, a detailed time domain simulation is carried out in PSCAD/EMTDC for validation. Finally, conclusions are discussed in section V.

978-1-5386-9316-2/18/$31.00 ©2018 IEEE

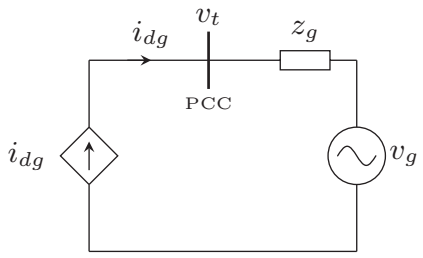

Fig. 1. Equivalent circuit

II. Analysis of VSC connected to Weak Grid

The grid is modelled as a voltage source behind a series impedance z_g as shown in Fig. 1. The VSC is connected at the PCC. Let the grid voltage be,

$$\begin{bmatrix} v_{g,a}(t) \\ v_{g,b}(t) \\ v_{g,c}(t) \end{bmatrix} = \begin{bmatrix} \hat{V_g}\cos(\omega_g t) \\ \hat{V_g}\cos(\omega_g t - \frac{2\pi}{3}) \\ \hat{V_g}\cos(\omega_g t - \frac{4\pi}{3}) \end{bmatrix} \tag{2}$$

where $\hat{V_g}$ is the peak phase voltage and ω_g is the grid frequency. The three phase grid voltage is represented using a complex space vector in stationary reference as,

$$\vec{V_g}(t) = \frac{2}{3}[v_{g,a}(t)e^{j0} + v_{g,b}(t)e^{j\frac{2\pi}{3}} + v_{g,c}(t)e^{j\frac{4\pi}{3}}] = \hat{V_g}e^{j\omega_g t} \tag{3}$$

For an inductive grid impedance, the PCC voltage $\vec{V_t}(t)$ in the stationary reference frame can be written as,

$$\vec{V_t}(t) = \vec{V_g}(t) + L_g\frac{d\vec{I_{dg}}(t)}{dt} \tag{4}$$

where L_g is the equivalent grid impedance inductor. The equation (4) in the stationary reference frame is transformed into a rotating reference frame (d-q) by multiplying with $e^{-j\phi_t}$, where ϕ_t is the PLL angle as shown in Fig. 2. The angle ϕ_t is derived from PLL as shown in Fig. 3. The grid voltage $\vec{V_g}(t)$ is represented in the rotating frame as ,

$$\vec{V_g}(t)e^{-j\phi_t} = \hat{V_g}[\cos(\omega_g t - \phi_t) + j\sin(\omega_g t - \phi_t)] \tag{5}$$

Similarly, the PCC voltage is represented as, $\vec{V_t}(t)e^{-j\phi_t} = V_{t,d} + jV_{t,q}$ and the current $\vec{I_{dg}}$ is represented as $\vec{I_{dg}}(t)e^{-j\phi_t} = I_{dg,d} + jI_{dg,q}$. The d axis and q axis component of the PCC voltage given in (4) can be written as,

$$V_{t,d} = L_g\frac{\mathrm{d}I_{dg,d}}{\mathrm{d}t} - L_g I_{dg,q}\omega_t + \hat{V_g}\cos(\omega_g t - \phi_t) \tag{6}$$

$$V_{t,q} = L_g\frac{\mathrm{d}I_{dg,q}}{dt} + L_g I_{dg,d}\omega_t + \hat{V_g}\sin(\omega_g t - \phi_t) \tag{7}$$

Considering unity power factor operation ($I_{dg,q} = 0$), the equation (7) can be simplified as

$$V_{t,q} = L_g I_{dg,d}\omega_t + \hat{V_g}\sin(\omega_g t - \phi_t) \tag{8}$$

From equation (8) , the effect of converter current on the PLL can be calculated. The loads connected to the PCC can also affect the PLL dynamics on top of the effect due to the grid impedance.

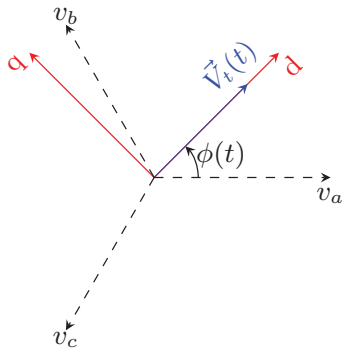

Fig. 2. Voltage space vector

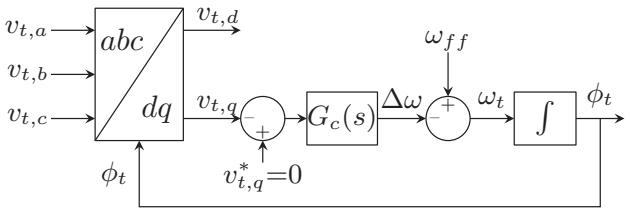

Fig. 3. Second order SRF PLL

III. Stability Limit

The large signal and small signal stability of PLL in a weak grid can be analysed as follows:

A. Large Signal Stability Limit

The large signal stability limit of the PLL can be analysed from the equation (8). The input to the PLL controller $G_c(s)$ is $V_{t,q}$, which is given by (8). For the stable operation of PLL, the error input to the controller $G_c(s)$ should go to zero. So the maximum current that can be injected from the VSC is,

$$|I_{dg,d}| \leq \frac{\hat{V_g}}{L_g\omega_t} \tag{9}$$

B. Small Signal Stability

The small signal model can be obtained by linearising the equation (8) around the nominal operating point. Let $\Delta V_{t,q}$, $\Delta I_{dg,d}$ and $\Delta\omega_t$ be the small signal perturbation around nominal operating point of voltage, current and frequency respectively. The equation (8) with the perturbation can be written as,

$$V_{t,q}+\Delta V_{t,q} = L_g(I_{dg,d}+\Delta I_{dg,d})(\omega_t+\Delta\omega_t)+\hat{V_g}\sin(\delta_o+\Delta\phi_t) \tag{10}$$

where, $(\omega_g t - \phi_t) = \delta_o$. On further simplification, the small signal is obtained as,

$$\Delta V_{t,q} = \omega_t L_g\Delta I_{dg,d} + L_g I_{dg,d}\Delta\omega_t + \hat{V_g}\cos(\delta_o)\Delta\phi_t \tag{11}$$

On taking the Laplace transform of the equation (11) and after simplification the small signal model of PLL is shown in Fig. 4.

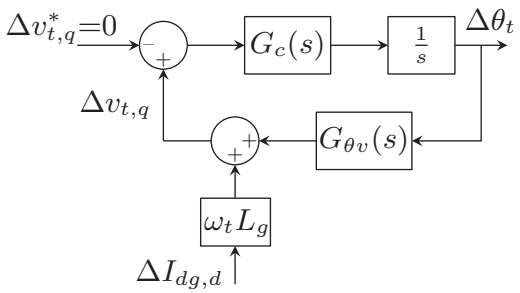

Fig. 4. Small signal model

where $G_{\theta v}(s) = \dfrac{\Delta V_{t,q}(s)}{\Delta\phi(s)} = (sL_gI_{dg,d} + \hat{V}_g\cos(\delta_o))$

The effect of current injected to the grid on the stability of PLL and the vector control can be analysed from this model.

IV. PLL CONTROLLER SELECTION

For the grid connected converter, PLL should be able to track the PCC voltage space vector without any error. Since the voltage space vector is aligned along the d-axis, the q-axis component should go to zero. From the small signal model, let the error between the reference q- axis voltage and the actual q-axis voltage be e, i.e

$$e = \Delta v^*_{t,q} - \Delta v_{t,q} \tag{12}$$

This error should go to zero for the proper operation of PLL, i.e $\lim_{t\to\infty} e(t) = 0$.

Using final value theorem, this can be expressed as,

$$\lim_{t\to\infty} e(t) = \lim_{s\to 0} s\frac{\Delta v^*_{t,q}(s)}{1 + \dfrac{1}{s}G_c(s)G_{\theta v}(s)} \tag{13}$$

So, the controller $G_c(S)$ should be selected in such a way that the equation (13) tends to zero under the steady state. The error analysis is performed for a proportional-integral and proportional controller.

A. Proportional Integral Controller

The controller used in conventional SRF PLL structure is a PI controller. In PI controller, $G_c(s)$ has one zero on the left half plane and one pole at origin. On substituting $G_c(s)$ in equation (13),

$$\lim_{t\to\infty} e(t) = \frac{\lim\limits_{s\to 0} s\Delta v^*_{t,q}(s)}{1 + \lim\limits_{s\to 0}\dfrac{1}{s}G_c(s)G_{\theta v}(s)} = 0 \tag{14}$$

B. Proportional Controller

In proportional controller $G_c(s)$ is selected to be a constant gain. Let $G_c(s) = k_p$. On substituting $G_c(s) = k_p$ in equation (13),

$$\lim_{t\to\infty} e(t) = \frac{\Delta v^*_{t,q}(s)}{1 + \lim\limits_{s\to 0}\dfrac{1}{s}k_pG_{\theta v}(s)} = 0 \tag{15}$$

From the above analysis, it is clear that both the P and PI controller will give zero steady-state error, which will help to track the PCC voltage space vector. This is due to the inherent integrator present in the PLL control structure. The extra integrator in the case of PI-controller is redundant.

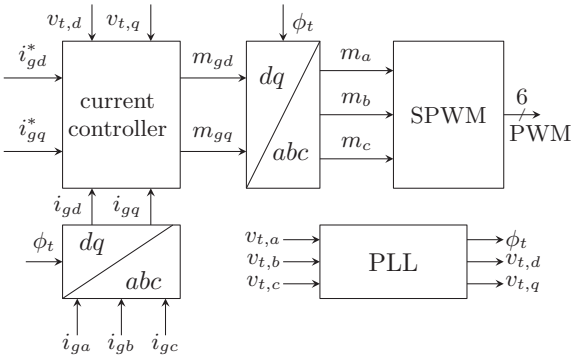

Fig. 5. VSC controller

V. RESULTS AND DISCUSSIONS

To verify the performance of PLL, a detailed time domain model given in Fig. 6 is developed in PSCAD/EMTDC. The VSC is operated with I_d and I_q current loop as shown in Fig. 5. The grid is modelled as a voltage source behind an impedance and the average model is used to model voltage source converter. The rating of the VSC and the grid parameters are listed in Table I.

TABLE I
VSI PARAMETERS

Parameter	**Value**
Base Voltage ,V	400 V
Base Power, P	25 kVA
Base Frequency ,F	50 Hz
Filter impedance, L_f	10 mH
Grid impedance, L_g	10 mH

The following two cases were simulated with different $G_c(s)$ to analyse their dynamic performance.

1) Proportional Integral controller: $G_c(s)$ is chosen to be a PI controller. The PI controller is designed [3] for a 50 HZ bandwidth, without considering the line impedance. For a step change in current I_d from 0.5 p.u. to 1 p.u., the response of I_d, $V_{t,q}$ and $V_{t,d}$ is shown in Fig. 7.

2) Proportional controller: $G_c(s)$ is chosen to be a proportional controller. The proportional controller is designed for a 50 HZ bandwidth, without considering the line impedance. For a step change in current I_d from 0.5 p.u. to 1 p.u., the response of $I_{t,d}$, $V_{t,q}$ and $V_{t,d}$ is shown in Fig. 9.

For the same bandwidth, P and PI control has almost similar dynamic performance. With PI controller an additional state is added which increases the order of the overall system. This increased order can result in damped oscillatory behaviour in some scenarios.

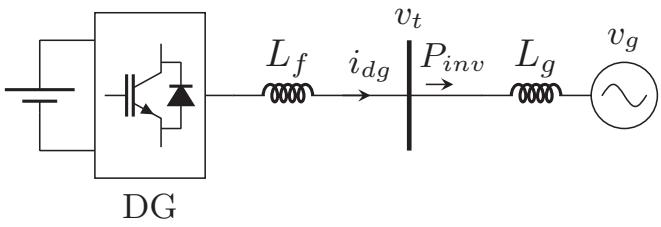

Fig. 6. Simulated system

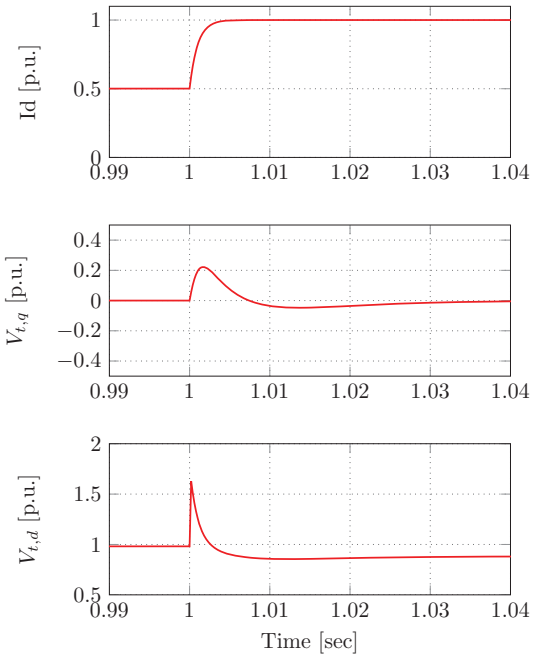

Fig. 7. Step response with PI controller

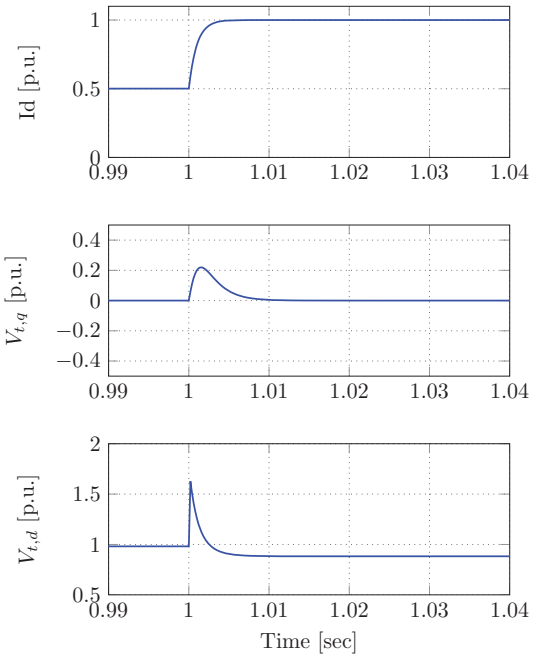

Fig. 9. Step response with P controller

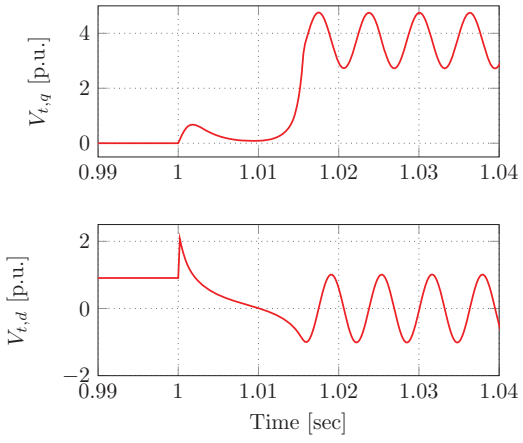

Fig. 8. Step response with SCR=1.13 and PLL bandwidth =50 Hz

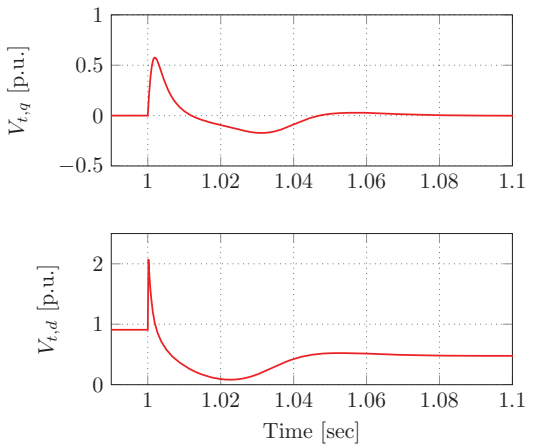

Fig. 10. Step response with SCR=1.13 and PLL bandwidth =40 Hz

In order to analyse the effect of grid impedance on the PLL control structure, the system SCR is reduced to 1.13 and the same step change in current I_d is performed from 0.5 p.u. to 1 p.u. Fig. 8 show the response of PLL voltages for a PLL bandwidth of 50 Hz. The system is unstable for this PLL bandwidth of 50 Hz. In order to make the system stable, the bandwidth of PLL is reduced to 40 Hz and the step response is shown in Fig. 10.

VI. Conclusion

In this paper, the effect of the PLL controller on the stability of a weak grid connected VSC is analysed. A comparison is made between a proportional and proportional-integral controller for PLL in the context of the stability and dynamic performance when connecting to the weak grid. A small signal model is built to show the interaction between injected current and PLL. The impact of PLL controller bandwidth and grid impedance on the system, stability was analysed in detail using time domain simulations.

Acknowledgement

This research is based upon work supported by the Department of Science and Technology (DST), India, for the project entitled UK India Clean Energy Research Institute (UKICERI) (Sanction No. DST/RCUK/JVCCE/2015/02).

References

[1] C. Schauder and H. Mehta, "Vector analysis and control of advanced static var compensators," *IEE Proceedings C - Generation, Transmission and Distribution*, vol. 140, no. 4, pp. 299–306, July 1993.

[2] J. L. Thomas, S. Poullain, and A. Benchaib, "Analysis of a robust dc-bus voltage control system for a vsc transmission scheme," in *Seventh International Conference on AC-DC Power Transmission*, Nov 2001, pp. 119–124.

[3] S.-K. Chung, "A phase tracking system for three phase utility interface inverters," *IEEE Transactions on Power Electronics*, vol. 15, no. 3, pp. 431–438, May 2000.

[4] "Ieee guide for planning dc links terminating at ac locations having low short-circuit capacities," *IEEE Std 1204-1997*, pp. 1–216, Jan 1997.

[5] J. Z. Zhou and A. M. Gole, "Vsc transmission limitations imposed by ac system strength and ac impedance characteristics," in *10th IET International Conference on AC and DC Power Transmission (ACDC 2012)*, Dec 2012, pp. 1–6.

[6] L. Zhang, L. Harnefors, and H. Nee, "Interconnection of two very weak ac systems by vsc-hvdc links using power-synchronization control," *IEEE Transactions on Power Systems*, vol. 26, no. 1, pp. 344–355, Feb 2011.

[7] J. Z. Zhou, H. Ding, S. Fan, Y. Zhang, and A. M. Gole, "Impact of short-circuit ratio and phase-locked-loop parameters on the small-signal behavior of a vsc-hvdc converter," *IEEE Transactions on Power Delivery*, vol. 29, no. 5, pp. 2287–2296, Oct 2014.

[8] L. Harnefors, M. Bongiorno, and S. Lundberg, "Input-admittance calculation and shaping for controlled voltage-source converters," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 3323–3334, Dec 2007.

[9] D. Dong, B. Wen, D. Boroyevich, P. Mattavelli, and Y. Xue, "Analysis of phase-locked loop low-frequency stability in three-phase grid-connected power converters considering impedance interactions," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 310–321, Jan 2015.

[10] X. Zhang, X. Danni, F. Zhichao, G. Wang, and D. Xu, "An improved feedforward control method considering pll dynamics to improve weak grid stability of grid-connected inverters," *IEEE Transactions on Industry Applications*, pp. 1–1, 2018.

[11] M. Davari and Y. A. I. Mohamed, "Robust vector control of a very weak-grid-connected voltage-source converter considering the phase-locked loop dynamics," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 977–994, Feb 2017.

[12] A. Egea-Alvarez, S. Fekriasl, F. Hassan, and O. Gomis-Bellmunt, "Advanced vector control for voltage source converters connected to weak grids," *IEEE Transactions on Power Systems*, vol. 30, no. 6, pp. 3072–3081, Nov 2015.

[13] D. Yang, X. Ruan, and H. Wu, "Impedance shaping of the grid-connected inverter with lcl filter to improve its adaptability to the weak grid condition," *IEEE Transactions on Power Electronics*, vol. 29, no. 11, pp. 5795–5805, Nov 2014.

[14] M. Cespedes and J. Sun, "Adaptive control of grid-connected inverters based on online grid impedance measurements," *IEEE Transactions on Sustainable Energy*, vol. 5, no. 2, pp. 516–523, April 2014.