Design of Controller for Selected Harmonic Power Elimination from DC Bus in Single Phase Inverter

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***Abstract*—Single phase power converters operating in stand-alone mode, has to frequently supply the non-linear loads. Under such case, the power reflected onto the DC bus, contains harmonics other than the usual double-frequency component. This increases the stress on the DC bus capacitor and eventually brings down the life of the converter. This paper proposes a novel control strategy which makes use of the active power decoupling (APD) capacitor in order to neutralise the harmonic power components in addition to the double-frequency power component at the DC bus. In this, a mechanism is developed to directly control the harmonic power flow and its effectiveness is demonstrated with pertinent simulation results.**

***Index Terms*—harmonic power, single phase**

I. Introduction

Single phase converters are inherently subjected to double-frequency power pulsation. Recently, various active power decoupling (APD) topologies are proposed, so as to reroute this pulsating power away from the DC bus capacitor. This eventually reduces the DC bus capacitor requirement leading to the use of film capacitors instead of electrolytic capacitors. The omission of electrolytic capacitor improves the life expectancy of the converter.

The focus of control for APD literature has been to compensate for the double-frequency power alone. This works fine in standard grid connected case, as the injected current is sinusoidal. However, if the same converter is used for stand-alone operation, more often than not, the DC bus capacitor will end up supplying substantial amount of harmonics other than the double-frequency one. This is because of the presence of non-linear local loads. The similar situation can also occur when the converter is controlled to cater to this local load in presence of grid as well.

The solutions to achieve the harmonic power compensation uses the APD topology same as that of double frequency compensation with the modified control strategy. In this regard, mainly two approaches are reported in the literature. In the first approach, the harmonic currents in the DC link gets channelised into the auxilliary APD circuit [1]. On the other hand, the second approach uses differential inverter topologies [2]–[5]. Here the common mode voltage across the capacitors are controlled to circulate the harmonic power between the load and the capacitors, thus preventing it from reaching the DC bus. Various controller implementations have been reported such as waveform control, a set of PR controllers and repetitive controllers to name a few. However, when looked closely one realises the fact that both the approaches essentially use DC decoupling topologies with the large dc offset across the capacitor, and thereby suffer from low utilisation factor for the storage capacitor. Moreover, the differential inverter topologies have higher DC bus voltage requirement [6].

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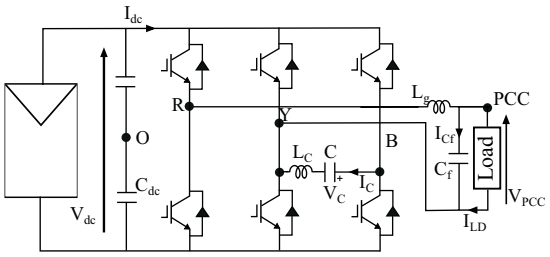


Fig. 1: Circuit diagram

Among various decoupling topologies, the AC decoupling topology of [7] (Fig. 1) stands out due to its adaptability to high power systems. However, adopting the same control strategy as in DC decoupling topologies for the AC decoupling topologies does not work. This is primarily because of the fact that these topologies operate on power compensation strategy rather than on current compensation. Thus, generating reference voltage for the capacitor in presence of harmonics is not straight forward and poses a challenge.

This paper aims to build a control framework to overcome the above mentioned issue. The generation of reference corresponding to mitigation of selected harmonic powers from the DC bus is presented. Moreover, a modulation strategy to overcome the increased DC bus voltage requirement, under such non-linear load, is also proposed. The content of the paper is presented as follows. The operating principle of the controller is presented in section II; section III contains the simulation results and finally, the paper is concluded in section IV.

II. Operating Principle

The schematic of the power converter is presented in Fig. 1. The three legs (R, Y, B) of the converter are shared by the APD capacitor (C) and the load. The DC bus capacitance, C_{dc}, sources/sinks the switching current harmonics. A high frequency filter inductor, L_C, is connected in series with the capacitor. The converter interfaces point of common coupling (PCC) through filter inductance L_g and filter capacitance C_f, and O is the virtual midpoint of DC bus capacitance. DC bus voltage is maintained at V_{dc}, and I_{Cf} and I_{LD} are the currents through the filter capacitor and the load respectively.

The design of system involves evaluating the various system parameters. For the system under consideration, the filter elements L_g and C_f are designed to have 0.1 p.u. system impedance, whereas, the APD elements C and L_C are designed following the procedure as mentioned in [7]. The designed system parameters are presented in Table I for quick reference.

In stand-alone mode, the converter control aims at regulating the PCC voltage, whereas, I_{LD} gets decided by the load. These loads being highly non-linear in nature, demands for harmonic power other than double-frequency power. For a typical rectifier load with capacitive filter, the power profile contains 2^{nd}, 4^{th}, 6^{th} harmonics and so on.

In order to achieve the power decoupling, the capacitive as well as load branch power expressions are formulated below,

Power flowing into the load branch,

$$p_{LD} = v_{RY} * (i_{LD} + i_{Cf}) \tag{1}$$

Power flowing into the capacitive branch,

$$p_C = v_{BY} * i_C \tag{2}$$

Now, the load branch power p_{LD}, in steady state, can be expressed as,

$$p_{LD} = P_{LD0} + P_{LD2\omega}\sin(2\omega t + \phi_2) + P_{LD4\omega}\sin(4\omega t + \phi_4) + P_{LD6\omega}\sin(6\omega t + \phi_6)...$$

Similarly, the capacitive branch power p_C, in steady state, can be expressed as,

$$p_C = P_{C2\omega}\sin(2\omega t + \psi_2) + P_{C4\omega}\sin(4\omega t + \psi_4) + P_{C6\omega}\sin(6\omega t + \psi_6)...$$

For the ideal harmonic compensation, the DC bus power,

$$p_{dc} = p_{LD} + p_C = P_{LD0}$$

Now, the instantaneous capacitive branch power corresponding to various harmonics can be expressed as,

$$\begin{aligned} p_{Ck} &= \sum_{i=\frac{k}{2}} X_{Cbi} I_{Ci}^2 \sin(k\omega t + 2\theta_i) \\ &+ \sum_{\substack{i+j=\frac{k}{2} \\ i\neq j}} (X_{Cbi} + X_{Cbj}) I_{Ci} I_{Cj} \sin(k\omega t + \theta_i + \theta_j) \\ &+ \sum_{\substack{i-j=\frac{k}{2} \\ i\neq j}} (X_{Cbi} - X_{Cbj}) I_{Ci} I_{Cj} \sin(k\omega t + \theta_i - \theta_j); \\ &\qquad\qquad \text{for } i,\ j = 1,\ 3,\ 5, ... \\ &= P_{Ckm}\sin(k\omega t + \mu_k) \qquad \text{where } k = 2,\ 4,\ 6, ... \end{aligned} \tag{3}$$

where, X_{Cbi}, I_{Ci} and θ_i's are the ith harmonic impedance, current magnitude and it's phase in the capacitive branch. As can be observed from the above expression, the relations among the control variables are i) highly nonlinear, and ii) strongly coupled unlike the DC decoupling strategies.

The control objective of compensating the harmonic power in the DC bus involves finding the relevant current harmonic reference in the capacitor branch. Here, to simplify the analysis, the three most dominant lower order harmonics are chosen to be compensated. To achieve this, fundamental, 3^{rd} and 5^{th} harmonic currents are injected in the capacitive branch.

Two schemes are implemented in the process. In scheme-1, 2^{nd}, 4^{th} and 6^{th} harmonic power in the DC bus, are chosen to be zero. Although, the desired elimination can be attained, following the above approach may lead to high current flowing through the capacitor branch. This is because, there is no constraint on the magnitude of reference current obtained from the solution. This increase in the capacitor branch current asks for increase in the i) converter rating ii) capacitor current rating iii) current rating of the filter inductor L_C etc.

To overcome such an undesired phenomenon, a constrained optimisation technique is proposed in scheme-2. The proposed technique aims to minimise the RMS current in the capacitive branch, while still compensating the desired power harmonics. Here 2^{nd}, 4^{th} harmonic power in the DC bus, are chosen to

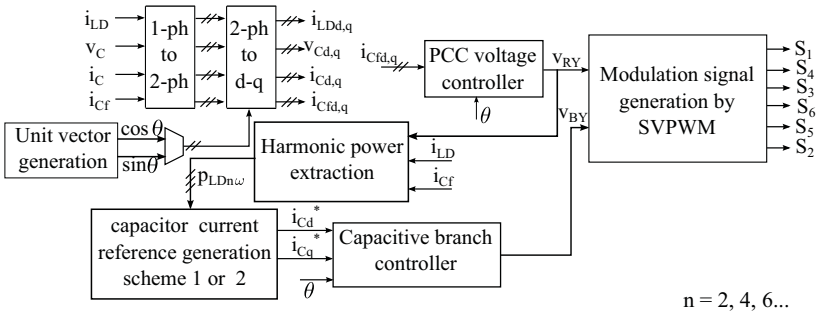


Fig. 2: Controller block diagram

be zero, whereas, 6^{th} harmonic power and the rms current in the capacitive branch is minimised in least square error basis. In both the schemes, fundamental, 3^{rd} and 5^{th} harmonics in the capacitive branch are controlled to achieve the objective.

The controller block diagram is presented in Fig. 2. First, various harmonic components are extracted from p_{LD} in *Harmonic power extraction* block. Notch filters, tuned at harmonic power frequencies, are used to accomplish this. Thereafter, the power equations are solved iteratively using Newton-Raphson method, to get the capacitor branch current reference. *Capacitive branch controller* (Fig. 2), nothing but a combination of proportional-integral (PI) and proportional-resonant (PR) controllers, is used to follow the reference. The controller generates the capacitor branch voltage v_{BY}. This, along with the load branch voltage v_{RY} (output of *PCC voltage controller* block (Fig. 2)), is fed to the Space Vector Pulse Width Modulation (SVPWM) block to generate the switching signals.

III. Results

TABLE I: System Parameters

AC Voltage, V_g	230V (50 Hz)
AC Current, I_{LD}	4A (50 Hz)
DC bus Voltage, V_{dc}	700V
Filter Inductor, L_g	0.1p.u.
Storage Capacitor, C	1.05p.u.
Filter Inductor, L_C	0.05p.u.
Filter Capacitor, C_f	0.1p.u.

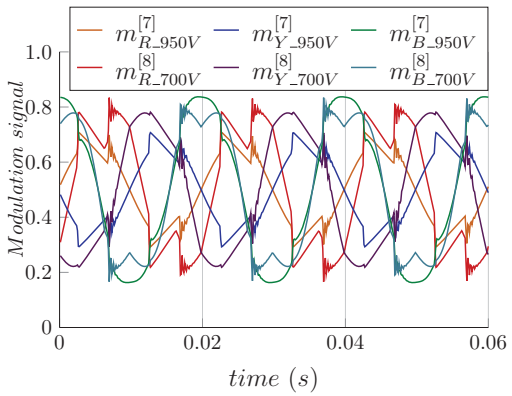
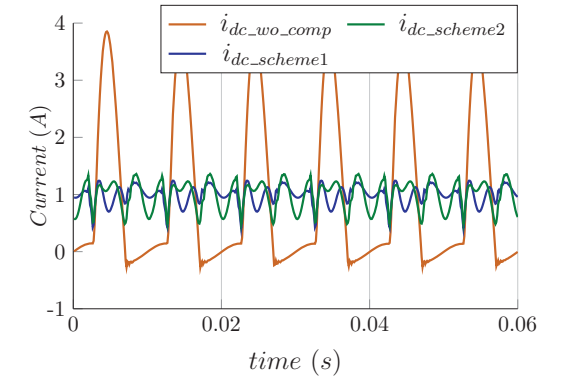
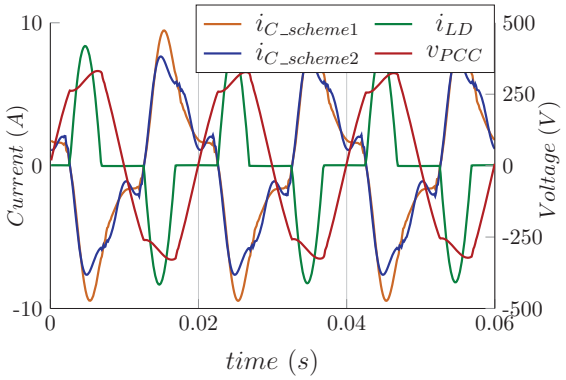


Fig. 3: Modulation signals following PWM strategy in [7] for 950 V DC bus voltage and SVPWM in [8] for 700 V DC bus voltage



(a)



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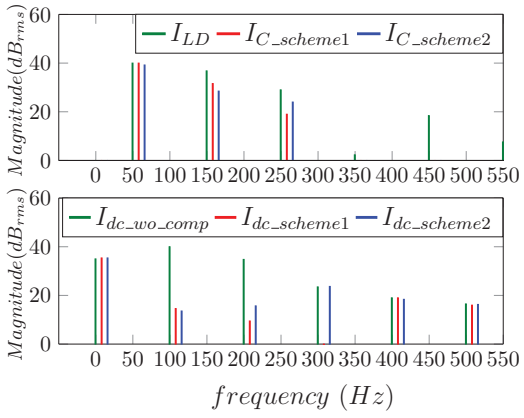
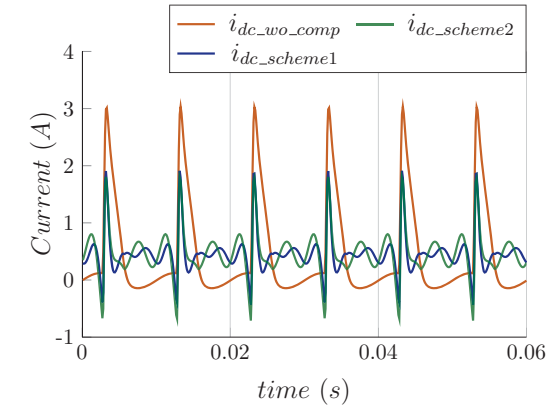


(c)

Fig. 4: (a) DC bus current waveform at steady state (b) Capacitor current, load current and PCC voltage waveform at steady state (c) FFT spectra for load current, capacitor branch current and DC bus current for rectifier load under scheme-1 and scheme-2 in stand-alone scenario

The effectiveness of the proposed control was verified by simulating a rectifier type load of same apparent power as presented in Table I, with crest factor 2.1, in Matlab/Simulink. Figure 4a shows the DC bus current profile without compensation ($I_{dc\_wo\_comp}$) and in presence of scheme-1 ($I_{dc\_scheme1}$) and scheme-2 ($I_{dc\_scheme2}$). The Ripple Factor (RF) reduces to 0.22 and 0.34 under scheme-1 and scheme-2, compared to 2.03 in uncompensated case. The capacitor branch current in scheme-2 ($I_{C\_scheme2}$) reduces over scheme-1 ($I_{C\_scheme1}$), since scheme-2 holds an additional constraint on capacitor current (Fig. 4b). From the FFT spectra in Fig. 4c, the reduction in both 100 Hz and 200 Hz component in $I_{dc\_scheme1}$ and $I_{dc\_scheme2}$ is upto 26 dB (i.e. 95%). However, the 300 Hz component gets reduced only in scheme-1, as it has been



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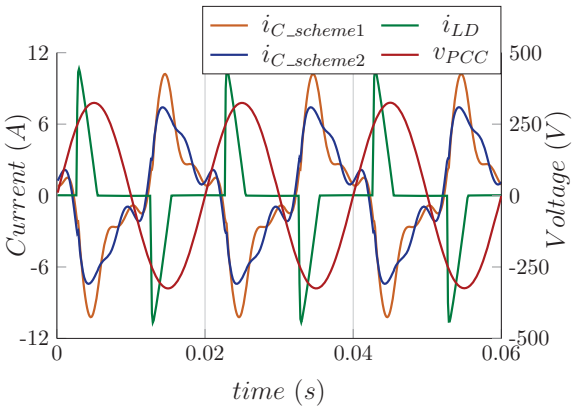

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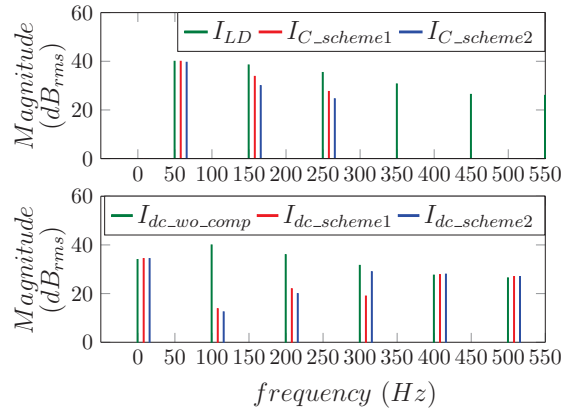

(c)

Fig. 5: (a) DC bus current waveform at steady state (b) Capacitor current, load current and PCC voltage waveform at steady state (c) FFT spectra for load current, capacitor branch current and DC bus current for rectifier load under scheme-1 and scheme-2 in ideal grid scenario

sacrificed over capacitor branch current reduction in scheme-2. The rms current in the capacitor reduces by 11% in scheme-2 compared to scheme-1.

Also, analysing the system as an unbalanced three phase system and adopting SVPWM as in [8], leads to 36% reduction in the DC bus voltage requirement compared to isolated control as in [7], and this can be seen in Fig. 3.

At this point, it should be noted that theoretically the proposed control strategy is not limited by the mode of operation (grid connected or stand alone). In order to validate the same, the system is simulated for the grid connected case as well. Here, unlike the standard grid connected operation, the converter is controlled to pump in sinusoidal current to the grid, while supplying the local non-linear load as well. For this purpose, the control structure needs to be modified slightly, as grid current rather than the PCC voltage is to be controlled in this case. Therefore, *PCC voltage controller* in Fig. 2 should be replaced with *Grid current controller*, rest of the control remaining same. The corresponding simulation results are presented in Fig. 5 for the same apparent power as in table I. The reduction in DC bus harmonic power, as well as, the capacitive branch rms current in scheme-2 over scheme-1 is observed, thus confirming the effective controller operation.

It is worth recalling that the usual approach of compensating only 100 Hz component, leaves behind considerable amount of 200 Hz (up to 50%) and 300 Hz (up to 16%) components in DC bus currents, for the non-linear load considered. These harmonic powers eventually bring down the life of the converter, as mentioned earlier.

IV. Conclusion

In this paper, a control strategy is proposed to compensate the selected harmonics including but not limited to double-frequency power in the DC bus. Two schemes are presented in this regard. Where scheme-1 offers upto 95% reduction of the selected harmonics, scheme-2 offers various optimisation possibilities including 10% reduction in current harmonics. With the compensation in place, the Ripple Factor in the DC bus current reduces upto 10 times. Also, by adopting SVPWM, the DC bus voltage requirement has been reduced by 35%. The simulation results are presented to substantiate the proposed control schemes.

References

[1] I. Serban and C. Marinescu, "Active power decoupling circuit for a single-phase battery energy storage system dedicated to autonomous micro-grids," in *2010 IEEE International Symposium on Industrial Electronics*, DOI 10.1109/ISIE.2010.5637040, pp. 2717–2722, Jul. 2010.

[2] N. Lu, S. Yang, and Y. Tang, "Ripple current reduction for fuel-cell-powered single-phase uninterruptible power supplies," *IEEE Transactions on Industrial Electronics*, vol. 64, DOI 10.1109/TIE.2017.2677329, no. 8, pp. 6607–6617, Aug. 2017.

[3] G. R. Zhu, S. C. Tan, Y. Chen, and C. K. Tse, "Mitigation of low-frequency current ripple in fuel-cell inverter systems through waveform control," *IEEE Transactions on Power Electronics*, vol. 28, DOI 10.1109/TPEL.2012.2205407, no. 2, pp. 779–792, Feb. 2013.

[4] H. Wang, G. Zhu, X. Fu, S. Ma, and H. Wang, "Waveform control method for mitigating harmonics of inverter systems with nonlinear load," in *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, DOI 10.1109/IECON.2015.7392527, pp. 002 806–002 811, Nov. 2015.

[5] W. Yao, Y. Xu, Y. Tang, P. C. Loh, X. Zhang, and F. Blaabjerg, "Generalized power decoupling control for single-phase differential inverters with nonlinear loads," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, DOI 10.1109/JESTPE.2018.2844098, 2018.

[6] H. Zhang, X. Li, B. Ge, and R. S. Balog, "Capacitance, dc voltage utilizaton, and current stress: Comparison of double-line frequency ripple power decoupling for single-phase systems," *IEEE Industrial Electronics Magazine*, vol. 11, DOI 10.1109/MIE.2016.2627013, no. 3, pp. 37–49, Sep. 2017.

[7] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, "Active power decoupling for high-power single-phase pwm rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1308–1319, Mar. 2013.

[8] R. Chen, Y. Liu, and F. Z. Peng, "Dc capacitor-less inverter for single-phase power conversion with minimum voltage and current stress," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5499–5507, Oct. 2015.