A new Approach for CMOS Op-Amp Synthesis

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Abstract

A new approach for CMOS op-amp circuit synthesis has proposed here. The approach is based on the observation that the first order behavior of a MOS transistor in the saturation region is such that the cost and the constraint functions for this optimization problem can be modeled as convex functions. Second order effects are then handled by formulating the problem as one of solving a sequence of convex programs. Numerical experiments show that the solutions to the sequence of convex programs converges to the same design point for widely varying initial guesses. This strongly suggests that the approach is capable of determining the globally optimal solution to the problem. Performance of the synthesized op-amps has been verified against detailed SPICE simulation for a 1.6μ CMOS process.

1 Introduction

In a mixed-signal integrated system, though the analog circuit occupies a small physical area compare to the digital counterpart, the analog circuit becomes the bottleneck in design time reduction. The main reason of this is that analog performances are very sensitive to the design variables. In other words the analog design problem is a complex trade off problem which is knowledge intensive. However, the research community has been aggressively working for computer aided analog design.

Existing approaches of automatic analog circuit sizing are broadly classified into three main categories, namely, *knowledge-based*, *simulation-based optimization* and *analytical equations based optimization*. Since analog design requires detailed circuit knowledge, a major approach of implementing an analog synthesis tool has been the knowledge-based approach. Some of the existing tools which follow this approach are BLADES [1], OASYS [2], IDAC [3]. However, the application of this approach has been limited due to requirement of having to codify extensive circuit knowledge and design heuristics.

On the other hand, DELIGHT.SPICE [4], ASTRX/OBLX [5] and FRIDGE [6] use simulation-based optimization approach. The main advantage of this approach is that a wide range of circuits can be synthesized. However the basic limitation comes from the requirement of costly circuit simulation in each iteration of the optimization algorithm.

To reduce the CPU-time of optimization-based techniques, the third approach that is followed in OPASYN [7] and OPTIMAN [8] is analytical equation based optimization where the circuit performances are evaluated using analytical equations. In equation based optimization use of simulated annealing [8] or gradient based cost optimization is not a good choice. This is because the analog circuit synthesis problem is a constrained optimization problem with complex trade-offs among the constraints, which is difficult to convert into one of minimizing a single cost function.

It therefore appears that an analytical equation based constrained optimization method is the most promising approach for automatic circuit sizing. However, the existing technique that uses this approach [9] suffers from the drawback that it needs expert designer knowledge to sequentially introduce the constraints. If this is not done, the method may fail to provide even a feasible design point. Further, any optimal point that is provided is only a local optimum design point.

In this paper, an efficient and robust synthesis method for CMOS analog circuits has been proposed. The proposed method has the capability of providing the globally optimal design point. This method is similar to that in a recent reference [10] which appears to have been done independently and in parallel with this work [11]. However, compared to [10], the proposed method addresses second order effects and finding d.c. operating point in a better way.

Organization of the remaining part of this paper is as follows. Various acronyms which are used through out the paper are provided in the following section. In the subsequent section the Shichman-Hodges (S-H) MOS model is described. In section 4, with the first order S-H model the op-amp synthesis problem is

formulated as a convex programming problem. On the other hand, section 5 describes how the higher order effects can be captured through an iterative approach. Experimental results are provided in section 6. Section 7 summarizes the work that is described in this paper.

2 Acronyms

Throughout this document the following symbols are used to denote various parameters of a transistor. W, L, L_e and ρ $(=\frac{W}{L_e})$ respectively denote channel width, length and effective length and aspect ratio of a transistor. I_D denotes magnitude of the drain current (d.c.). V_D, V_G, V_S and V_B are drain, gate, source and substrate voltages (d.c.), respectively. V_{DS}, V_{GS} and V_{SB} are magnitude of drain-source, gate-source and source-substrate voltages, respectively. Magnitude of threshold voltage, drain saturation voltage and effective gate to source voltage are denoted by V_T, V_{DSAT}, V_{EGS} $(=|V_{GS} - V_T|)$ respectively. λ denotes channel length modulation and $k^{'}$ $(= \frac{\mu C_{ox}}{2})$ denotes transconductance factor. Λ denotes a factor $(1 + \lambda V_{DS})$. Finally, g_m and g_d are transconductance and drain conductance.

Note that, for ease of discussion, we consider only the magnitude of some of the parameters.

3 Shichman-Hodges MOS model

In Shichman-Hodges MOS model [13], a transistor is in saturation region when,

$$V_{GS} > V_T \text{ and } V_{DS} \geq V_{DSAT}(= V_{EGS}) \tag{1}$$

and in this region of operation the drain current is,

$$I_D = k^{'} \rho (V_{EGS})^2 \Lambda. \tag{2}$$

The body effected threshold voltage is,

$$V_T = V_{To} + \gamma(\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|})$$

where, γ is body factor and ϕ_F is equilibrium electrostatic potential. The channel length modulation λ is equal to λ_c / L_e, where, λ_c is a constant.

From equation (2) we get transconductance, drain conductance and effective gate to source voltage of the transistor in terms of its bias current respectively,

$$\left.\begin{array}{rcl} g_m & = & 2\left[k^{'} I_D \rho \Lambda\right]^{\frac{1}{2}} \\ g_d & = & \frac{\lambda_c I_D}{\Lambda L_e} \\ \text{and, } V_{EGS} & = & \left[\frac{I_D}{k^{'}\rho\Lambda}\right]^{\frac{1}{2}} \end{array}\right\} \tag{3}$$

One of the primary objective in analog synthesis is to bias all transistors in appropriate operating point (mostly in saturation region of operation) which helps to get high performance. This objective can be achieved by introducing a set of design space constraints. Therefore, in our synthesis formulation we use these saturation region characteristic equations. Note that in S-H model, assuming constant Λ, the device model parameters g_m, g_d and V_{EGS} are product of power (PoP) functions of ρ, L_e and I_D. A PoP function is product of a positive coefficient and various variables which are raised to some power (any real number). This is the key information on which our synthesis formulation is based.

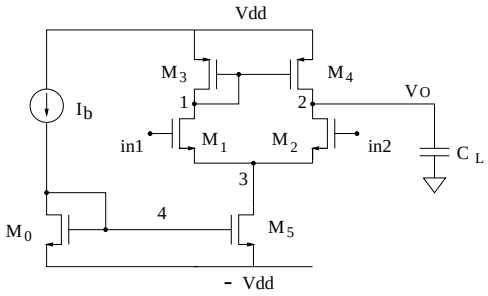

Figure 1: Simple op-amp, a running example

4 The Basic Approach

The proposed synthesis approach has been explained with the running example circuit shown in Figure 1. The design optimization problem is,
minimize a weighted sum of gate area and power while,

$$\begin{array}{rcl} \text{low frequency gain, } A(0) & \geq & A_{SPEC} \\ \text{unity gain frequency, } UGF & \geq & UGF_{SPEC} \\ \text{slew rate, } SR & \geq & SR_{SPEC} \\ \text{common mode range, } CMR & \geq & CMR_{SPEC} \\ W_L \leq W_i & \leq & W_U \\ L_L \leq L_{ei} & \leq & L_U \end{array}$$

W_L and W_U and, L_L and L_U are specified lower and upper bounds on W_i and, L_{ei}. In this design problem L_e and $\rho (= W/L_e)$ of the transistors, and the bias current I_b are the design variables. The various intermediate steps of the design formulation are as follows.

4.1 D.C. Analysis

It is observed that in a CMOS analog circuit, the d.c. current through all the transistors can be essentially determined by that through only a few transistors which we refer to as current source transistors. Then from the drain currents and sizes of the transistors their gate to source voltages can be obtained. Further, various node voltages can be defined by the gate to source voltages of the transistors.

Transistors	V_{DS}	V_{SB}
M_1, M_2	$V_1 - V_3$	$V_{dd} - V_3$
M_3, M_4	$V_{dd} - V_1$	0.0
M_5	$V_3 - (-V_{dd})$	0.0
M_0	$V_4 - (-V_{dd})$	0.0

Table 1: V_{DS} and V_{SB} of various transistors

In the example op-amp, the drain current of the current source transistor M_5 is,

$$I_{D5} = k_5^{'}\rho_5\Lambda_5\left[\frac{I_b}{k_0^{'}\rho_0\Lambda_0}\right]. \quad (4)$$

Since M_1, M_2 and M_3, M_4 are two matched pairs,

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{I_{D5}}{2} \quad (5)$$

From equation (3) for all transistors we get,

$$V_{GSi} = V_{Ti} + \left[\frac{I_{Di}}{k_i^{'}\rho_i\Lambda_i}\right]^{\frac{1}{2}} \quad (6)$$

Consider the transistor M_3. Its gate and drain voltages are the same and $V_{DS3} = V_{GS3} = V_{dd} - V_1$.

$$\text{Therefore, } V_1 = V_{dd} - V_{GS3}. \quad (7)$$

Note that, V_1 and V_2 are the same. Now considering the transistors M_1 and M_5 respectively,

$$V_3 = V_{in1} - V_{GS1}. \quad (8)$$
$$\text{and, } V_4 = -V_{dd} + V_{GS5}. \quad (9)$$

These node voltages are now used to express the V_{DSi}'s and V_{SBi}'s of the various transistors as given in the Table 1.

The above analysis shows that, the equations (4) - (9) and Table 1 represent a complete set of nonlinear equations whose solution provides accurate node voltages. An effective way of solving this set of nonlinear equations is through a fixed point scheme. The overall method of finding node voltages is shown in Figure 2.

In the first step, the device model parameters Λ_i's and V_{Ti}'s are updated based on the V_{DSi} and V_{SBi} values in the previous iteration. Next, the drain current of all transistors in the circuit are found.

In the next step V_{GSi}'s are determined from I_{Di}'s, ρ_i's, Λ_i's and V_{Ti}'s of the transistors. In the subsequent step, from the V_{GSi}'s, various node voltages are determined. For the running example circuit the

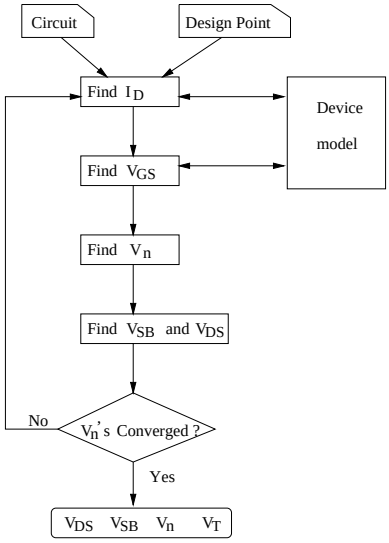

Figure 2: Finding d.c. operating point

equations (4) - (9) are used to find various node voltages. In the final step V_{DSi}'s and V_{SBi}'s are evaluated using their equations which are given in Table 1. In the subsequent iteration the values of the V_{DSi}'s and V_{SBi}'s are then used to get a more accurate estimate of the d.c. operating point. The terminating condition is, all node voltages in two consecutive iterations are very close.

4.2 Design space constraints

Here we find the design space constraints by which all the transistors are kept away from subthreshold and linear regions. The constraints,

$$\frac{\epsilon_{SUB}}{V_{EGSi}} \leq 1 \quad (10)$$

keep all the transistors away from the subthreshold region with a margin of ϵ_{SUB}. On the other hand to keep a transistor away from the linear region we require,

$$\left.\begin{array}{r} V_D \geq V_G - V_{TSAT} \text{ for n-type} \\ \text{or, } V_D \leq V_G + V_{TSAT} \text{ for p-type} \end{array}\right\} \quad (11)$$
$$\text{where, } V_{TSAT} = V_{GS} - V_{DSAT}.$$

In the example circuit, as the gate and drain voltages of the transistors M_3 and M_4 are the same, they are always in saturation. Now, to keep M_1 (and M_2) in saturation, we require $V_1 \geq V_{in1} - V_{TSAT1}$. In quiescent condition $V_{in1} = 0$. Further, from equation (7), $V_1 = V_{dd} - V_{GS3}$. Therefore, the design inequality is,

$$\text{or, } \frac{1}{(V_{dd} - V_{T3} + V_{TSAT1})}.V_{EGS3} \leq 1 \quad (12)$$

To keep transistor M_5 away from linear region, we require $V_3 \geq V_4 - V_{TSAT5}$. Using the expressions of V_3 and V_4 in equations (8) and (9) we get,

$$\frac{(V_{EGS5} + V_{EGS1})}{V_{dd} + V_{in1} - V_{T1} - V_{T5} + V_{TSAT5}} \leq 1. \quad (13)$$

The explicit inequalities (10), (12) and (13) keep all the transistors in the example circuit in saturation.

Finally, to keep the transistor sizes within the specified limit the following inequalities should be satisfied:

$$\frac{\rho_i L_{ei}}{W_U}, \frac{W_L}{\rho_i L_{ei}}, \frac{L_{ei}}{L_U}, \frac{L_L}{L_{ei}} \leq 1 \quad (14)$$

4.3 Performance constraints and objective function

The low frequency gain of the op-amp is $\frac{g_{m1}}{g_{d1}+g_{d3}}$. Therefore, to meet the gain specification

$$A_{SPEC} \cdot \frac{g_{d1}}{g_{m1}} + A_{SPEC} \cdot \frac{g_{d3}}{g_{m1}} \leq 1 \quad (15)$$

The unity gain frequency and slew rate of the op-amp are g_{m1}/C_L and I_{D5}/C_L, respectively. Therefore to meet their specification,

$$\frac{C_L.UGF_{SPEC}}{g_{m1}} \leq 1 \quad (16)$$

$$\frac{C_L.SR_{SPEC}}{I_{D5}} \leq 1 \quad (17)$$

The negative and positive common mode ranges of the op-amp are respectively, $CMR^- = -V_{dd} + V_{GS0} + V_{GS1} - V_{TSAT5}$ and $CMR^+ = V_{dd} - V_{GS3} + V_{TSAT1}$. Therefore, to get the specified CMR we need,

$$\frac{(V_{EGS0} + V_{EGS1})}{(V_{dd} - V_{T0} - V_{T1} + V_{TSAT5} - CMR_{SPEC})} \leq 1 \quad (18)$$

$$\text{and, } \frac{V_{EGS3}}{(V_{dd} - V_{T3} + V_{T1} - CMR_{SPEC})} \leq 1 \quad (19)$$

The objective function is,

$$f_0 = w_1 \sum_i \rho_i L_{ei}^2 + w_2 (I_b + I_{D5}). \quad (20)$$

where w_1 and w_2 are two specified weights.

With constant Λ, it is found that I_D, V_{EGS}, g_m, g_d and I_D are PoP functions of the design variables (ρ, L_e and the bias current I_b). Further, with constant V_T, V_{TSAT} and Λ, the constraint functions (ref. equations (10) and (12) – (19)) and the objective function (ref. equation (20)) are *posynomial functions* [14] of the design variables.

To summarize the formulation which is given in this section, an op-amp design problem is a constrained optimization problem. With the logarithmic transformation on the design variables design problem becomes a convex programming problem.

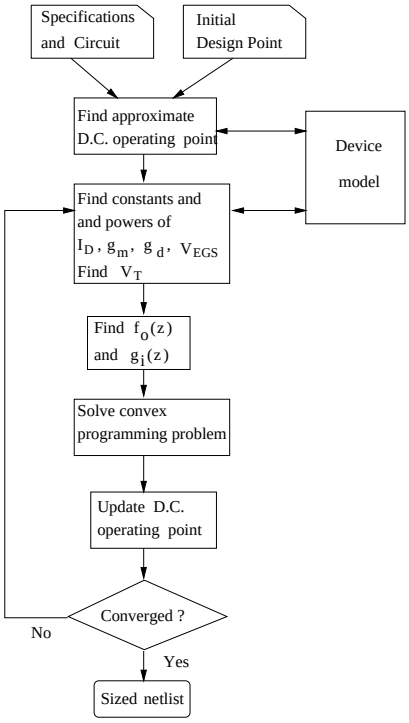

Figure 3: Op-amp synthesis method

5 Formulation of Op-Amp Design as a Sequence of Convex Programming Problems

In the last section assuming constant V_T, V_{TSAT} and Λ, the op-amp synthesis problem is formulated as a convex programming problem. Here, to account for the effect of variations in V_T, V_{TSAT} and Λ, the overall method is shown in Figure 3. The various steps of the method are as follows. In the first step the designer specifications and the circuit to be sized are accepted. Then using two iterations of the d.c. analysis technique described in section 4.1, an approximate d.c. operating point at the initial design point is found.

In the next step the constants and powers of the PoP representation of the various I_{Di}'s g_{mi}'s, g_{di}'s and V_{EGSi}'s are determined. The values of V_{DSi}'s which are used to determine the constants of the PoP terms come from the previous iteration. Similarly, to evaluate the threshold voltage of the transistors the values of V_{SBi}'s come from the previous iteration.

In the third step, from the constants and powers of g_{mi}'s, g_{di}'s, V_{EGSi}'s and I_{Di}'s and, the values of V_{Ti}'s the objective function and the constraint functions in the log transformed design space are derived. The convex programming problem is then solved in the fourth step.

In the subsequent step, the d.c. operating point is

Perf.(unit)	Spec.	S-H Deg-I	Spice Deg-I	S-H Deg-II	Spice Deg-II
A(0) (dB)	70	70	59	70	67
UGF (MHz)	10	10	9.6	10	9
PM (deg.)	60	65	71	66	61
BW (kHz)	–	3.3	10.6	3.2	4.3
CMRR (dB)	60	79	71	81	82
CMR (V)	± 2.5	-2.8,5.0	-3.8,4.7	-2.5,4.8	-3.4,4.8
OS (V)	± 3	-4.7,4.7	-4.8,4.8	-4.4,4.5	-4.4,4.7
SR (V/μsec)	20	20	19.3	20	18.4
PD (mW)	–	0.27	0.39	0.51	0.54
Area ($\mu \times \mu$)	–	87.6	–	137.99	–

Table 2: Specifications, S-H model based predicted performances and Spice measured performances at the two final design points

It.#	CPU time (sec)	MaxErr in L_i (μ)	MaxErr in W_i (μ)	MaxErr in V_n (V)
1	9.5100	–	–	–
2	7.8800	0.2339	1.6499	0.2005
3	7.1000	0.0166	0.2664	0.0305
4	5.2300	0.0008	0.0048	0.0048
5	5.1600	0.0001	0.0006	0.0008
Tot.	34.8900			

Table 3: Optimization statistics in design-I

updated for the new solution design point.

In the final step, the convergence of the sequence of solution design points is checked. If the design points and the node voltages of the last two iterations are very close then the op-amp netlist with sized transistors is provided. Otherwise, it goes back to the second step.

6 Experimental Results

The CMOS op-amp synthesis technique that has been described so far, has been implemented in MATLAB [15] for a large class of 2-stage CMOS op-amps. MATLAB was selected in the interest of quick prototyping.

A number of two stage op-amps were synthesized for a 1.6μ technology. While synthesis results of a simple two stage op-amp is provided in this section, more synthesis results are available in [11]. The first stage of the considered example op-amp is exactly the same circuit that is shown in Figure 1. The second stage of the op-amp is simple transconductance amplifier which consists of a p-type transistor (M_6) and a n-type transistor (M_7). The circuit uses $R-C$ compensation circuit that consists of R_c and C_c. The performance specification is given in the second column of the Table 2.

Variables	Design-I	Design-11
W_0/L_0 (μ/μ)	2.4000/2.0441	2.4000/3.4674
W_1/L_1 (μ/μ)	2.4000/3.5361	2.4000/2.6598
W_2/L_2 (μ/μ)	2.4000/3.5361	2.4000/2.6598
W_3/L_3 (μ/μ)	3.8246/1.9246	2.5782/2.6109
W_4/L_4 (μ/μ)	3.8246/1.9246	2.5782/2.6109
W_5/L_5 (μ/μ)	2.4000/2.0889	2.4000/4.0244
W_6/L_6 (μ/μ)	21.5914/1.6000	27.9688/2.6000
W_7/L_7 (μ/μ)	7.1581/1.6000	8.1017/2.6000
Cc (pF)	0.1830	0.2943
Ib (μA)	3.3468	6.7618

Table 4: The two optimal design points

The circuit was synthesized by starting from four widely varying initial design points. The optimization statistics in one of the four cases is shown in Table 3. In the table, the first and second columns indicate the iteration number and the CPU time (IBM RS/6000, running AIX) required for solving each of the the convex programming subproblems. The last three columns of the table provide the maximum difference in transistors lengths and widths and, node voltages, at the two solution design points in two consecutive subproblems. With the other three initial guesses the convergence behavior was quite similar to this. Further, the four solution design points which were obtained by starting from the four initial design points are essentially the same. This indicates that the technique has found the globally optimal solution. The final design point is given in the second column of Table 4.

An expert designer would pick non-minimum channel length for the input stage transistors to get high gain. On the other hand, for the second stage transistors, in order to achieve high slew rate he/she would choose minimum channel length with large channel width. The optimal design point given in Table 4 is qualitatively similar to such a choice.

The various performances at the optimal design point as predicted by the synthesizer using Shichman-Hodges model and the corresponding Spice measurements (using the level 2 MOS model) are given in the third and fourth columns of Table 2. Note that while the Shichman-Hodges model based predictions satisfy the specifications, some of the performances like, low frequency gain, band width and power dissipation as actually measured in Spice (using level 2 model) do

not. The inaccuracies are due to the inadequacy in the the S-H MOS model in the short channel regime. However, for long channels the model is quite accurate. To demonstrate this, in the second design optimization we restrict the channel length of the transistors to be more than 2.6 μ.

The solution design point and the predicted performance of the op-amp at the solution design point are given in Tables 2 and 4 Note that, at the second solution design point, the predicted performances using S-H MOS model is close to those of Spice simulation. However, the total gate area and the power dissipation at the second solution point are respectively, 57% and 38% more than those at the first solution design point.

7 Summary

An efficient method of circuit synthesis of CMOS op-amps is proposed here. In this method the op-amp synthesis problem is formulated as a sequential convex programming problem. The main advantage of such a formulation is that a convex programming problem is very straight forward to solve it in a robust and computationally efficient manner. Further, the sequence of solutions generated, is a sequence of global optima of convex programming subproblems. Intuition therefore suggests that the point to which this sequence converges is the globally optimal solution of the original problem.

Using the Shichman-Hodges MOS model the method has been implemented in MATLAB as a quick prototype. The experimental results highlight the robustness and computational efficiency of the technique. The fact that the same optimal design point was obtained with widely varying initial guesses strongly suggests that the technique is capable of finding the globally optimal solution. Further, the optimal design point is qualitatively similar to one that would be picked by an expert designer.

However, since the Shichman-Hodges model is not accurate in the short channel regime. Therefore, a different MOS model is required to target a technology for short channel. For this we may refer to [11].

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