A Course on Introduction to Electronic Packaging

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Abstract

The translation of performance achievable on silicon to the system level requires the intervention of a high performance packaging technology. In high performance systems, the package is more than a mere provider of interconnections, mechanical support and protection. The package can and will actively influence the performance of the circuit and the system. With the lead times for introducing new products continuously getting reduced, it is necessary to manage the interface between the functional design and the package design at the board level. To manage this interface effectively, the electronics hardware designer needs to have a good appreciation of different aspects of packaging. This paper presents the case for a core course to the students of electrical and electronic engineering programme. Detailed syllabus, lecture plans and laboratory exercises related to the proposed course are presented. It is also suggested that a course of this nature should be created for web based instruction.

Introduction

Computer, telecommunication, automotive and consumer electronic products are undergoing dramatic changes. The new generation electronic products are characterized by very low-cost, large volumes, portability, very high performance and diverse functionalities. While semiconductor technology has been the main driving force in bringing about these changes, the performance gains achievable at silicon level, cannot be realized without corresponding developments in electronic packaging technology. Single chip packaging has evolved, during the last three decades, from DIP/wirebond, QFP and SMT to BGA. The packaging of passive components also kept pace with these evolutions. Multichip packaging is normally done through ceramic, thin film and printed wiring board technologies. The cost per I/O connection being the best with printed wiring board technology, it is the best candidate for the next generation electronic products. Packaging Research Centre of Georgia Tech, USA, proposes a technical vision for the printed wiring board technology, known as Single Level Integrated Module (SLIM) technology, that can offer a very high silicon efficiency at the board level while drastically reducing the cost of interconnections.

Electronic packaging may be defined as the engineering and art of providing singal and power connections to the active compoents of an electronic circuit, and protecting that circuit adequately from the environment. The electronic packaging my be viewed at three levels: *chip, board* and *system*. The materials, components, manufacturing technologies, and design considerations are very different at different levels of packaging. There has been a proliferation of packaging technologies and packages in the last few years. Each one of them provide a different cost-performance optimization. Consequently packaging design is fast emerging as an important and distinct activity in electronics. At present the performance of an electronic product is as good as its packaging design and the packaging technology used. Electronic packaging is a highly multidisciplinary activity that integrates materials, electrical, thermal, reliability, and manufacturing aspects

There is certainly a case for evolving both undergraduate and graduate programmes in electronic packaging. Packaging design is concerned with the electrical and thermal design of an electronic product in the context of a manufacturing technology chosen. It would greatly help the development of a new state-of-the-art electronic product, if the electronic (functional) designer has an appreciation of the packaging aspects, and is able to integrate the packaging considerations into his functional design and to effectively interface with the *packaging designer*.

This paper presents a course on electronic packaging for students of electrical and electronic engineering, that can be offered either at senior undergraduate or graduate level. The design of the proposed course is based on twenty five years of experience with the graduate programme on Electronics Design and Technology offered at CEDT (Centre for Electronics Design and Technology) of Indian Institute of Science, Bangalore, India. This graduate programme offers separate courses on Interconnection Technology and Design, and Mechanical Packaging of Electronic Systems. These courses were mainly aimed at board and system level packaging aspects. These two courses were further supported by a course on Electromagnetic Compatibility and a course on Reliability. The proposed course "Introduction to Electronic Packaging" has focus on the board level packaging. This course, while sensitizing the students to the packaging aspects of electronic products, and providing limited packaging design capabilities is also expected to enthuse some of the students to plan for a career in electronic packaging.

Structure of the Course

The development of an electronic product in the present context is a highly multidisciplinary activity. There are industrial design, packaging, reliability, manufacturing and marketing dimensions to a product besides the functional (hardware and software) dimension. With the time to introduce new products continuously reducing in the global scenario, it is necessary that all the dimensions of the products can be effectively and efficiently addressed. With the packaging technology playing a central role in the present day products, it is necessary for an electronic engineer to have adequate knowledge of the packaging design and technology.

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An undergraduate programme in electronics may not have scope for introducing more than one course in packaging into its core. In such situation, what should be focus and scope of that course on electronics packaging? Electronic packaging issues, as mentioned earlier, need to be addressed at three levels of hierarchy, namely Chip, Board and System. An electronics hardware engineer is often concerned with the design and development of electronic products. He is concerned with functional design using readily available ICs and/or ASICs and FPGAs in some standard packages, and is done predominantly at the board level. On some occasions he is also concerned with the integration of the boards into a product. An electronics hardware designer will be able to relate more to the board and system level packaging than to the chip level packaging. Therefore, the first on electronic packaging should have the board as its focus, with some familiarization with the packaging issues at the system level.

The printed wiring board has thoroughly changed its character over the years. Table 1 summarizes the features of printed wiring boards in relation to the developments at silicon level. It is no more a passive, but an active element greatly contributing to the signal integrity. The attention that needs to be paid to the signal integrity issues, especially in mixed mode designs is significantly more than that to the connectivity issues.

Quantum jumps have occurred in the assembly of the printed wiring boards. The through hole mounting of yesterday is no more a candidate in the context of today's miniaturization. The surface mount devices have come handy for size reduction. The BGAs, Micro-BGAs need to be attached in the flip chip mode. All this brings a host of assembly and testing problems. The small size IC packages by virtue of higher technology throw a lot of heat onto the PC board. The boards need newer methods of cooling, better thermal conductivity, matching thermal expansions, higher glass transition temperatures, better co-planarity, lighter weight, better machining ability and so forth. All these considerations are getting shifted to the designer's domain. In addition to all the above consideration the designer has to be concerned with the translation of his design into a manufacturable item in the context of an identified fabrication facility. This kind of a situation calls for a thorough insight into the principles of board manufacturing and assembly methodologies. In other words, Design for Manufacturability is no more a wish but a need.

Year	Max System Clock	PC Board complexity	PC Board Min trace width	IC Design Geometry
1965	1 MHz	1-2 layers	100 mil[2.54 mm]	10 microns
1980	10 MHz	2-4 layers	20 mil[0.50 mm]	3 microns
1995	100 MHz	4-10 layers	6 mil[0.15mm]	0.5 micron
2001	1000 MHz	4-24 layers	2 mil [0.05 mm]	0.1 micron

Table 1: Evolution of the Printed Wiring Board

Keeping the needs of an electronic engineer, as identified above, limitation on the core credits available, and the need to enthuse some of the students to explore the areas of electronic packaging further, the goals of the proposed course are chosen to enable the students of electrical and electronics engineering programme

- to effectively interface with packaging designers, and
- to design and document printed wiring boards of medium complexity that are manufacturable.

As formal engineering programmes are offered in different contexts in different parts of the world, it is necessary to develop the proposed course in a manner that would meet a wide range of requirements. For example the credit load of this course may be chosen as 2:0, 2:1 or 3:0 in the context of 12 week term or 16 week semester. Besides, different instructors may wish to emphasize different aspects of packaging design or technology. In order to meet these varying requirements, and still meet the above stated objectives, it is proposed to

- have a modular structure for the course material, and
- generate about sixty hours of learning material, and 35 laboratory exercises

Packaging design, besides knowledge of manufacturing processes, electrical engineering aspects of signal and power interconnections, and principles of heat transfer, requires familiarity with a large quantity of data related to materials, packages, testing and manufacturing. The students need to internalize a significant of such quantitative data. They need to be familiar with standards, document practices of manufacturing units, and with environmental issues. It is advantageous if the students have a chance to see the video clips on certain manufacturing processes, and pictures of many mechanical details, properly and improperly assembled boards and components. It is also desirable if the student can get a chance to simulate correct and faulty conditions, and directly see the consequences. The nature of the subject of packaging design and technology, makes it an ideal candidate for web based instruction. Institutions that do not have the required laboratory facilities to give direct experience to students will also be able to offer a course on packaging.

The features of the proposed course on electronic packaging may be summarized as:

- Modularity
- 60 hours of instructional material
- 35 laboratory exercises with some on a virtual laboratory based on public domain CAE tools.
- Web based instructional material supported by hard copy lecture notes

The learners of this course are the senior undergraduate and graduate students of electrical and electronic engineering. They are all expected to have gone through courses like network theory, transmission lines, and analog and digital electronics. They are also expected to be familiar with circuit and dynamic system simulation using CAE tools.

The topics and their weigtages are listed in the following. Most of the topics are divided into two levels. While the first level is considered essential, the instructor is free to choose from the elective topics to make up for the balance of the course. The choice of topics is based on the background of the target audience, namely, electrical and electronic engineering students, and not on the criticality of issues.

	Topic	Level 1 Hours	Level 2 Hours
1.	Overview of Electronic Packaging	4	-
2.	Board Manufacturing	4	8
3.	Board Assembly	2	4
4.	Electrical Issues	6	8
5.	Thermal Issues	6	6
6.	Reliability	2	-
7.	Quality Issues	-	2
8.	Standards, Documentation and Environmental Issues	2	-
9.	Board Design	4	-
10.	Emerging Packaging Technologies	-	2
	Total	30	30

The syllabus for these topics, organized as Modules, is presented in the following.

MODULE 1 : Overview of Electronics Packaging - 4

Nature of present and future of electronic products. Review of different approaches to meet future challenges. What is electronic packaging. Levels of packaging. Overview of technologies at different levels of packaging. Description of passive as well as active device packaging styles. Package wiring and terminals. Some examples of state of the art electronic products highlighting the usefulness of packaging concepts in system development.

MODULE 2 : Board Manufacture : 4 Hours

Description of types of PWBs, subtractive, semi-additive and additive technological routes, photo tooling, imaging by screening and photolithography, drilling and plating through hole variations, solder masking, legend printing, and surface finishing of boards, multi layer, flexible and 3D board concepts.

MODULE 3 : Board Assembly - 2 Hours

Electronic solders, flux and its role, hand Soldering of through hole components, component pick and place, hand as well machine assembly methods, soldering of surface mount components. IR reflow and wave soldering principles.

MODULE 4 Electrical Issues - 6 hours

Identification of issues that need to be addressed in the electrical design of packages. Characterization of receivers and drivers. Signal distribution in slow speed packages. Modeling of the behavior of interconnection elements at high frequency. Reflections. Design of terminations. Power distribution, ΔI noise, power supply impedance at high frequency, and ΔI noise containment. Crosstalk.

MODULE 5- Thermal Issues - 6 hours

Heat generation in electronic packages and thermal management strategies. Fundamentals of heat transfer processes. Modeling of thermal behavior different packaging instances at board level. Cooling methods. Design of heat sinks and simple forced cooling systems

MODULE 6 - Board Reliability - 2 hours

What is reliability of electronic packages and how do we measure it. Factors that influence the reliability of the board: contact resistance, environmental interactions, thermal mismatch and thermal fatigue, mechanical and tribological considerations, and heat transfer degradation.

MODULE 7 - Standards and Documentation - 2 hours

Standardizing bodies, laminate classification and IPC/MIL/NEMA standards, acceptability of the printed wiring boards, thumb rules for component assembly, documentation of design requirements for manufacturability, digital description for board manufacture. Environmental issues.

MODULE 8 : Board Design - 4 hours

Schematic circuits, planning the design, design rules, creating libraries, foot print design component placement strategies, establishing interconnectivity, net designation, layering, drill file and Gerber plots, design documentation. Design for Manufacturability issues.

MODULE 9: Board Manufacturing : 8 (Level 2)

High Performance Laminates: High performance requirements, glass transition, and thermal expansion needs, signal delays related to laminate properties, concepts of impedance matching, thermal management at board level with metal cored laminates, incorporation of thermal vias.

Advanced MLBs and BUM Technologies : Methods of multilayer construction, sequential build up concept, advantages of buried and blind vias, overview of emerging BUM [Build-up multilayer] technologies, signal integrity as well as thermal issues in multilayer construction.

Board Quality: Understanding board quality, process errors which influence board quality, quality audit, quantification of errors and fixing acceptance standards, plated through hole quality, cross sectioning.

Electronics Finishing: Finishing needs of board, tin and tin/lead finishes, hot air leveling, nickel-gold plating, organic surface preservatives.

Microvias: Different technology options

MODULE 10: Board Assembly : 4 hours (Level 2)

Flip chip attach. Influence of I/Os on packaging style, PGAs and BGAs, issues of thermal mismatch, fatigue of the ball joints, co-planarity of the substrate, assembly challenges, and underfills.

MODULE 11: HF Electrical Package Design: 8 hours (Level 2)

Analysis and design of high frequency interconnects. Design of bus structures and mother boards.

MODULE 12: Cooling of Electronic Systems : 6 hours (Level 2)

Modeling of the thermal behavior of boards and systems. Case studies in cooling system design.

Laboratory Exercises

Most of the packaging issues can only be appreciated if the student has a chance to work in the laboratory. Unfortunately all Departments may not want to create elaborate laboratory facilities for just one course. The resources available to students, therefore, will significantly vary. In the context of web based instruction, some of the experiments may have to be conducted in virtual environment. A total number of 35 exercises are proposed in the following. The instructor can choose a subset of these according to the resources available and his personal preferences.

1. PCB design with simple CAD tool	8
2. Simulation of electrical behavior of interconnections	4
3. Measurements of electrical behavior of the interconnections on the board	3
4. Simulation of thermal behavior of boards	3
5. Board level thermal measurements	3
6. Substrate testing	2
7. Board manufacturing	
Photo tooling and imaging	1
Etching and PTH plating	1
Quality and inspection	1
8. Board assembly and rework	3
9. Miniproject (design, build and test)	6

Conclusions

There is strong case for offering a course on electronic packaging to students of electrical and electronic engineering either at undergraduate or graduate level. The aims of such a course is to sensitise the electronic engineer to various issues of electronic packaging and to enable him to design printed wiring boards of medium complexity. By creating this course in the context of web based instruction, it can be made accessible to a much wider audience.

References

[1] Rao R. Tummala et.al.: Microelectronics Packaging Handbook, Techology Drivers Part I, 2nd Edition, Chapman&Hall, 1997.