A STATCOM for Composite Power Line Conditioning

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Abstract - **Although desirability of active filters is universally accepted, equipment cost can still be an impediment for usage. This aspect can be somewhat redeemed by incorporating multiple mitigatory functions on the same hardware platform. In this paper, inclusion of two compensatory functions on a single STATCOM is discussed. All analytical designs are supported by experimental results.**

I. INTRODUCTION

With the ongoing deregulation taking place worldwide in the power industry, Power Quality (PQ) issues are being given increasing importance. Adherence to PQ norms is poised to serve as the figure-of-merit influencing procurement choice of consumers. Consequently, it influences the business of competing distribution utilities. Today, it presents a major area of technology development for providing effective PQ solutions at the optimum cost.

The subject of PQ compensation has been receiving considerable attention from researchers in the recent past. It is accepted that power electronic converters, chiefly voltage source inverters (VSI), are to be suitably connected to the utility grid to obtain PQ compensatory functions. Based on their connection, these compensators can be classified into the shunt, series or the unified types. Of these, the shunt configuration, which is popularly known as the STATCOM, is being given more preference due to its simpler connection requirements. Various authors [1], [2] have reported control strategies for using the shunt compensator as *active filters,* for compensating harmonic currents, injected into the utility by non-linear loads. Others [3] have reported its usage for indirectly compensating the voltage at the load bus, by injecting a regulated reactive current. The emphasis, therefore, has been on using it for one *or* the other function.

In spite of all its desirable effects, the high equipment cost of a power electronic converter will be a major impediment against their widespread use. The burden of costs, however, can be somewhat mitigated by incorporating more than one function in a single compensator. In this paper, such a composite shunt compensator is described. It is used to compensate for the reactive power *and* harmonic currents generated by a load center, comprising both linear and non-linear loads. The control strategy is explained and an analytical design method is reported. Experimental results obtained with an IGBT based STATCOM are presented.

Some possible drawbacks of the adopted strategy are pointed out and relevant conclusions drawn.

II. THE STATCOM

The STATCOM is primarily a variable current source, connected in shunt with the Point of Common Coupling (PCC), as shown in Fig. 1. It is realized by connecting a VSI to the PCC through series inductors. For situations which do not demand any steady active power input, only a capacitor is connected across the inverter dc bus.

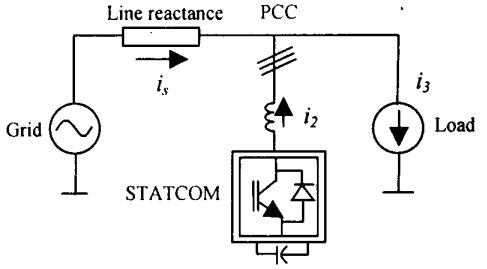

Fig.1 : STATCOM in the system

To inject the desired current, the STATCOM *must* have a closed-loop current control scheme, which forms the innermost loop within the controller hierarchy. Use of fast switching devices, like the IGBT, has made possible the realization of a high controller bandwidth. Hence, apart from control of currents at fundamental frequency, controlled injection of harmonic currents can also be achieved.

The series inductors separate the two voltage sources and also filter the switching ripple in the inverter current. To replenish the internal losses in the inverter, a small amount of active power is drawn from the PCC. The capacitor voltage is maintained by closed-loop control, which regulates the active current drawn from the mains.

III. EXPERIMENTAL HARDWARE

For experimental verification, an 8 KVA, IGBT-based inverter is fabricated. The series inductors (9 mH, 0.3 Ω) and dc bus capacitors (1750 μF) are designed to limit the ripple on the ac side current and dc voltage, respectively. Inverter protection functions like overvoltage, overcurrent and shoot-through are incorporated.

The load comprises a 5-hp induction motor and a 1 kW, 6-pulse thyristor rectifier. The induction motor is run on

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no-load and draws predominantly reactive current. The thyristor rectifier feeds an R-L load and injects harmonic currents into the supply lines. Fig. 2 shows the experimental set-up.

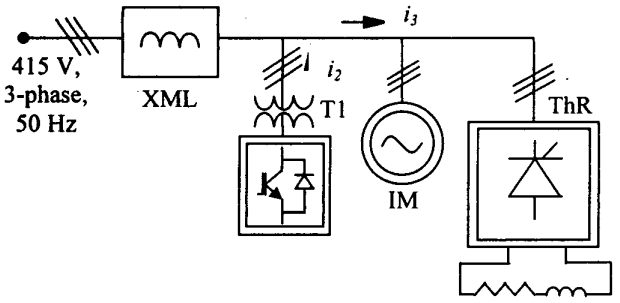

Fig. 2 : Experimental set-up
IM : Induction motor, 3-phase
ThR : Thyristor rectifier
T1 : Matching transformer (2:1)
XML : Transmission Line module

The controller is implemented on a fixed-point, DSP-processor (TMS320F240) with an internal clock rate of 36 MHz. Apart from the usual facilities, this processor has a built-in peripheral module, consisting of a 16-channel,10-bit ADC and a dedicated PWM engine.

IV. CURRENT CONTROL

The current controller used is of the type described in [4]. The currents are converted from the three-phase co-ordinates to the synchronously rotating reference axes using the following equations.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} 1.5 & 0 & 0 \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (2)$$

The control law along either of the rotating axes (d or q) takes the following form: -

$$u = V \pm \omega L \cdot i' + H(\delta i) \quad (3)$$

where,

V : PCC voltage component along that axis
L : inductance of inverter series reactor
i' : current component along complementary axis
$H(\delta I)$: control function involving current error along that axis.

Theoretically, ω should strictly match the line frequency, thus implying online measurement of system frequency. However, for a power system, the frequency variation is restricted to a small range. Therefore, a constant ω corresponding to the most probable frequency can be used without significant deterioration of transient performance.

With the above feedforward terms in place, the controllers can be independently designed. The plant for each of the axes consists of a first-order lag corresponding to the series inductance (L) and its internal resistance (R), shown in Fig. 3.

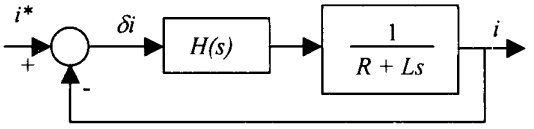

Fig. 3 : Current controller structure

The controller is chosen to be of the PI-type, with the PI parameters designed to cancel the plant pole and also to obtain a satisfactory speed of response. Thus,

$$H(s) = K\frac{1+sT_c}{s} = \frac{K+sKT_c}{s} \quad (4)$$

Consequently,

$$K_P = KT_c \quad \text{and} \quad K_I = K \quad (5)$$

Here, K_p = 21.2, K_I = 600. In the present paper, the entire control is realized with the help of a digital processor. Therefore, all the controller parameters obtained from continuous-time analysis (s-domain) are converted to their discrete-time equivalents (z-domain) using the Bilinear rule (without pre-warping). A sampling interval of 125 μs was used.

Fig. 4 shows the waveforms obtained in experiment for a step change in the q-axis reference current. Both simulation and experimental results are shown for comparison. The simulation model includes sampling delay and controller saturation effects, but does not include switching.

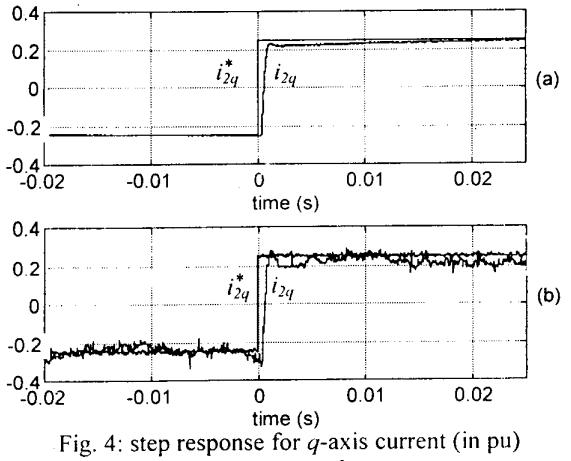

Fig. 4: step response for q-axis current (in pu)
(a) simulated waveform
(b) experimental result

V. HARMONIC COMPENSATION

Various solution approaches for harmonic current compensation have been proposed in literature [5], [6]. These methods are different in terms of the signals measured and compensation strategies that are adopted. In the present paper, the active cancellation approach is used. This requires extraction of the harmonic component of load current and injection of a current at the opposite phase. These issues are individually discussed here.

A. Current harmonic extraction

1) Extraction algorithm: Although various approaches for harmonic extraction have been proposed, it is now accepted that the Synchronous Reference Frame (SRF) method is more suitable for realization. It involves transformation of the three-phase line currents to their *d-q* equivalents using (1) and (2). The features of this transformation are listed below: -

- fundamental components of current are transformed to dc quantities
- harmonic components of frequency ω_h are transformed into ac quantities of frequency $\omega+\omega_h$ or $\omega-\omega_h$, depending on the relative sense of rotation of the harmonic vectors and the rotating reference-frame.

A modified high-pass filter algorithm then extracts the harmonic components.

2) The PLL: To get a good harmonic measurement, the unit vectors must have very high fidelity. This implies that they have a fixed phase relationship with the PCC voltage and should be free of any other harmonic component. The PLL used for this purpose has to be very stable with low phase error. In the present paper, a software-PLL is used. The PLL algorithm is run on a separate platform and the unit vectors are read in by the main processor at every sampling interval. The interval between two successive zero-crossings of the PCC voltage is sensed and the frequency computed. Accuracy of the phase relationship depends on the reliability of the zero-crossing detector. A Kalman-filter algorithm is used to minimise the effects of multiple zero-crossing and distortion in the PCC voltage. The unit vectors are aligned to be in phase with the PCC voltage vector. Hence, control of active and reactive current can be done independently of each other.

B. Harmonic current injection

1) Controller delay: For operation within saturation limits of the controller, the operation of the current loop can be represented by a first-order lag

$$\frac{i(s)}{i^*(s)} = \frac{1}{1+\frac{s}{\omega_b}} \qquad (6)$$

As a result, the current response is *phase*-shifted with respect to the reference current. Also, this phase shift is a non-linear function of frequency. In a digital implementation using carrier-based PWM methods, the sampling time and carrier wave period introduces a *time*-shift in the output response. The corresponding transfer characteristic can be expressed as

$$H_d(s) = e^{-sT_d} \qquad (7)$$

The corresponding phase-shift is a linear function of frequency.

The total effect of these phase shifts is to hamper exact cancellation of the harmonic current, even if the harmonic extraction were very accurate.

2) Delay compensation: It is possible to compensate the delay in (6) by using a phase-lead network. However, such solutions are effective only for a very narrow frequency range and a wide-spectrum harmonic compensator becomes difficult to achieve. Exact compensation of the delay in (7) is not possible in real-time, since the required compensator becomes non-causal. Although phase-lead compensators can also be used as before, the same limitations exist.

Since harmonic standards, like the IEEE-519, 1992, specify current harmonics as a steady-state problem, the harmonic currents can be predicted from its time-history as

$$i_3(kT_s + T_P) = i_3(kT_s) \qquad (8)$$

where,

T_s : sampling interval of the processor

T_P : periodicity of the harmonic current.

This allows the use of advanced DSP techniques like FFT for delay compensation. The phase-shift for every frequency can be computed from offline analysis and individually compensated for. The inverse transformation is then performed to generate the current references in time domain. However, in all such cases, there is a tradeoff between the size of the buffer memory and accuracy of harmonic extraction. It is also computation intensive.

A simpler method, being proposed here, is to store the actual data points for one cycle of the harmonic waveform and then introduce the required phase advance, i.e.

$$i_2^*(kT_s + T_P) = i_3(kT_s + a) \qquad (9)$$

where,

a : time advance to be given.

Two data storage spaces S1 and S2 are defined in the processor memory. In a particular cycle, the load current samples are stored in S1 (10) and the reference for the current controller is fetched from S2 (11). In the subsequent cycle, S2 is used as the storage space and reference is fetched from S1. This sequence repeats itself. By adjusting the data pointer for the "fetch" space, the required phase advance (a) can be provided.

$$i_3^S(k) = i_3(k) \qquad (10)$$

$$i_2^*(k) = i_3^f(k+a) \qquad (11)$$

where, the superscript (f) indicates data from the fetch table.

The source current (i_s) contains the magnetising current of transformer T1. As the available PCC voltage contains distortion components at 5th and 7th harmonics, the magnetising currents also contain these harmonics. Since the shunt compensator is only meant for compensating the load-induced harmonics, a correct signal to observe is $i1$, where,

$$i1 = i_3 - \frac{i_2}{n} \qquad (12)$$

and n is the transformation ratio of T1. Fig. 5 shows $i1$ waveforms (Phase A) with and without harmonic compensation. Only the thyristor rectifier was energized and the STATCOM was run in the harmonic compensation (HC) mode.

Fig. 6 shows $i1$ waveforms (Phase A and B) when both ThR and IM are energized and the STATCOM run in the HC mode as before. Table I shows the harmonic analysis of $i1$ (Phase-A), with and without compensation.

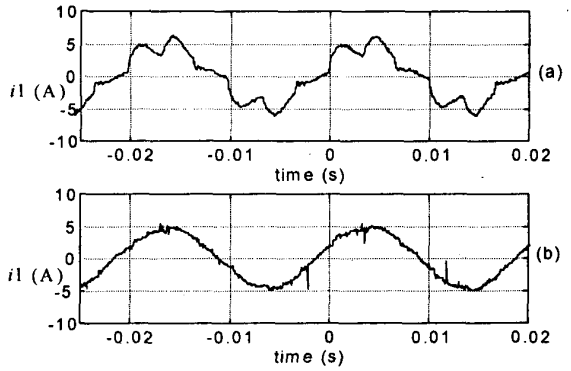

Fig.5 : Current harmonic compensation
(a) without compensator
(b) with compensator

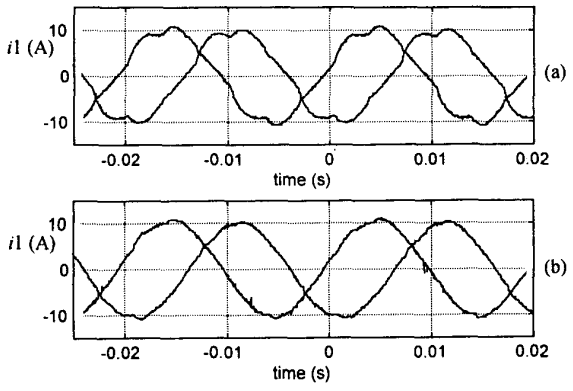

Fig.6 : Current harmonic compensation with induction motor on
(a) without compensator
(b) with compensator

TABLE I
HARMONIC ANALYSIS OF $i1$

harmonic number	harmonic content	
	without compensation	with compensation
1	0 dB	0 dB
3	-38.75 dB	-38.44 dB
5	-21.56 dB	-36.56 dB
7	-32.5 dB	-39.06 dB
9	-54.7 dB	-46.56 dB
11	-35 dB	-42.5 dB
13	-48.44 dB	-47.5 dB
15	-54.7 dB	-48.75 dB
17	-41.56 dB	-45.62 dB
19	-59.38 dB	-54.06 dB

VI. POWER FACTOR COMPENSATION

For power factor compensation, the reactive component of the load current is measured and fed as a reference to the current controller. As mentioned before, aligning the unit vectors with the PCC voltage helps to decouple the measurement and control of real and reactive currents. Hence, all active currents are reflected in the d-axis current and all reactive currents are reflected in the q-axis current as dc components.

Fig. 7 shows the low-pass filter (LPF) used in the harmonic extraction scheme. The output of the q-axis LPF generates the reactive component of the load current. It is seen that the load power factor can be easily computed from the harmonic extraction routine. The extracted reactive component is then added on to any other q-axis current reference to generate the overall q-axis current reference.

Fig. 8 shows the source current (Phase A) with and without compensation. Only the induction motor was energized and the STATCOM was operated in the power factor correction (PFC) mode. The entire reactive current was not compensated because of limiter action, which is described in the next section. A residual harmonic component can still be observed in the line current. This is due to the harmonic content in the source voltage (chiefly 5th and 7th), which induces currents at those frequencies in the motor and T1.

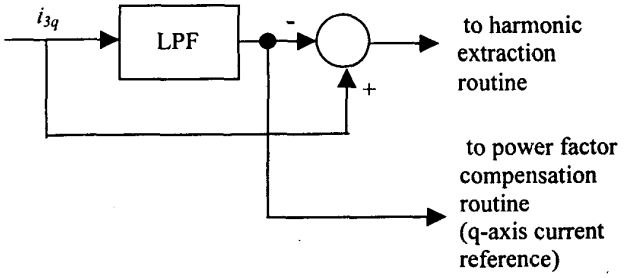

Fig.7: Power Factor Compensation (reference generation)

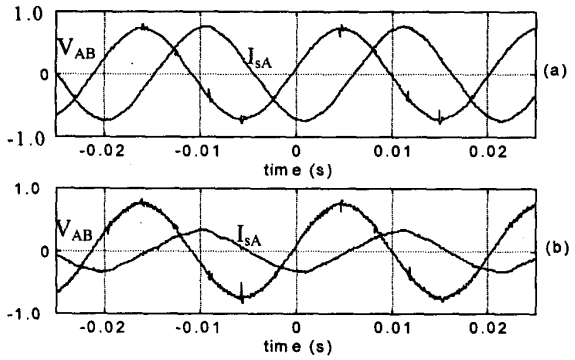

Fig. 8 : Reactive power demand
(a) without compensation
(b) with compensation
Scale (y-axis) : 1div = 800 V / 10 A

VII. COMPOSITE COMPENSATION

A. Control Scheme

The control scheme for composite compensation (CC) is shown in Fig. 6. Both the inverter and load currents are sensed. Since a 3-wire system is being considered here, only two line currents are measured. The PCC voltages are also measured for generating the feedforward term for current control.

To limit the inverter current within the rated value, the reactive current reference is output limited. The outputs of the harmonic current controllers (*d* and *q*) are indirectly restricted by the limits on the reactive current reference and modulation signals (m_d and m_q). The final limits on the modulation voltage, which is also sensed at every computation step. The limit is calculated as signals are dynamically varied according to the dc bus voltage as

$$m_{max} = 0.675\, V_{dc} \qquad (13)$$

The *d-q* axes modulation signals are then transformed to three-phase reference signals using the inverse transformations of (1) and (2). To prevent low-order harmonic interaction between the dc bus and the inverter current, the modulation signals are *divided* by the dc bus voltage. This ensures that the harmonics on the dc bus do not get reflected on the output modulation signals. The final switching signals are generated after comparison with an 8 kHz triangular carrier wave.

B. Experimental Results

The STATCOM was run in the CC mode with both the motor and rectifier energized. Fig. 10(a) shows the *i*1 waveforms for phases A and B. The harmonic distortion can be clearly detected. Fig. 10(b) shows the PCC voltage (V_{AB}) and *i*1 for phase A. It shows that the fundamental component of the line current is predominantly reactive. For improvement of the steady-state power quality, both the current harmonics and power factor need to be compensated.

Fig. 11(a) and 11(b) show the experimental results obtained with the CC scheme in operation. Fig.10(a) shows *i*1 waveforms for phases A and B. Comparison with Fig. 10(a) shows a decrease in the waveshape distortion. The dominant harmonic (5^{th}) is attenuated by a factor of about 5dB. Fig. 11(b) shows PCC voltage (V_{AB}) and *i*1 (phase A) waveforms. Comparison with Fig. 10(b) shows a reduction in the reactive current (peak value) by 2.75A. It can be concluded that, there is a general improvement in PQ.

C. Discussions

The PWM is done here by the sine-triangle modulation method, which has the lowest ac output voltage, for a given dc bus voltage, amongst all PWM modulation schemes. So, although the control effort was individually sufficient for HC or PFC, it was not adequate for CC implementation. As a result, a general improvement in power quality was observed, but total compensation could not be achieved *only* due to

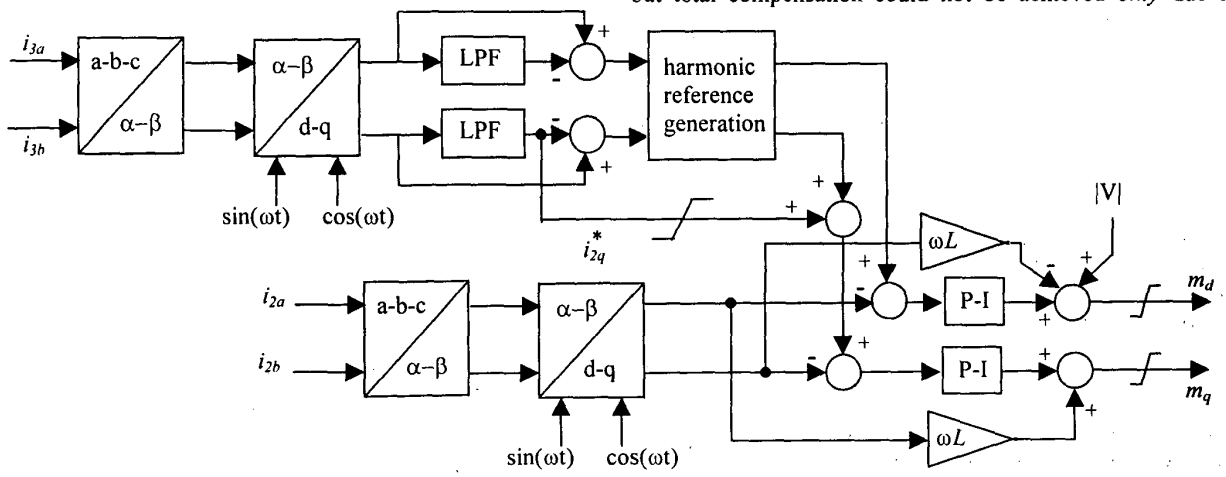

Fig. 9: Control Schematic

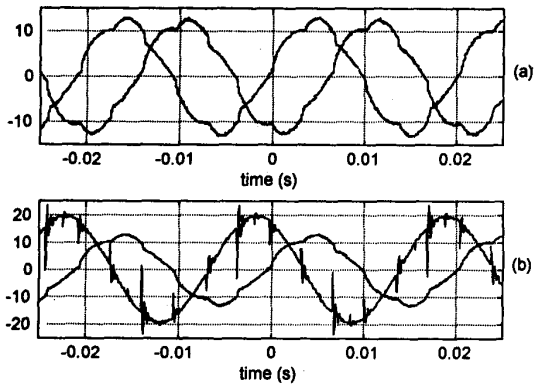

Fig. 10 : Utility pollution
(a) harmonics : $i1$ (Phases A and B)
(b) poor power factor : $i1$ and $0.5V_{AB}$

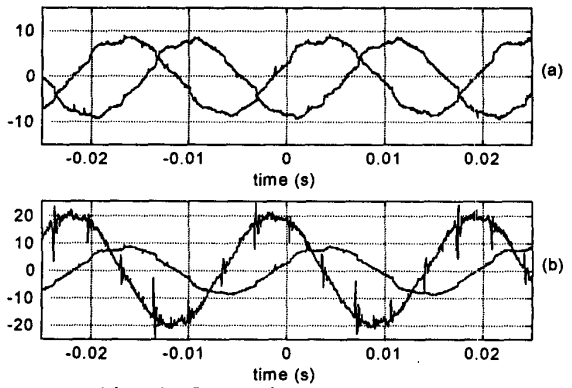

Fig. 11 : Composite compensation
(a) harmonics : $i1$ (Phases A and B)
(b) power factor : $i1$ and $0.5V_{AB}$

rating constraints. For such cases of resource constraint, the weightage given to each function has to be adjusted according to the load requirements or penalty imposed.

However, the central point is that a combination of PQ compensation functions, at different frequencies, is possible with a single hardware platform. Moreover, this can be achieved with unit vectors of a single frequency. Although the CC scheme entails some more complexity in the modulation strategy or additional dc bus voltage, it may still be more economical than multiple, dedicated hardware platforms.

VIII. CONCLUSIONS

Based on the above discussions and experimental results, the following can be concluded.

1. A simple harmonic compensation scheme was proposed. Experimental results show compliance with the existing standards (IEEE-519,1992).

2. Power factor compensation could also be achieved. The corresponding measurement signal can be derived from the harmonic extraction routine.

3. A composite compensation (CC) scheme was proposed, which incorporates the above two functions. Unit vectors used were only of fundamental frequency, resulting in a simpler PLL.

4. Experimental results show that a direct combination of the HC and PFC modes is possible without any extra control requirements. Improvement in the current waveform was noted, though it was not to the extent desired. Reasons for the shortfall were discussed.

IX. ACKNOWLEDGEMENT

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