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Analytical evaluation of DC capacitor RMS current and voltage ripple in neutral-point clamped inverters

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Abstract. The sizing of the DC-link capacitor in a three-level inverter is based on the RMS current flowing through it. This paper analyses the DC-link capacitor RMS current in a neutral-point clamped (NPC) inverter and expresses the same as a function of modulation index, line-side current amplitude and power factor. Analytical closed-form expressions are derived for the capacitor RMS current for single-phase half-bridge, single-phase full-bridge and three-phase three-leg topologies of a three-level inverter. The worst-case capacitor current stress is determined for each topology based on the analytical expressions. Further, analytical expressions are derived for the RMS values of low-frequency and high-frequency capacitor currents. These expressions are then used to estimate voltage ripple across the DC capacitor for sinusoidally modulated three-phase NPC inverter. The analytical expressions for the RMS current and voltage ripple are validated experimentally over a wide range of operating points.

Keywords. Current control; current stress; diode-clamped inverter; full-bridge inverter; half-bridge inverter; multi-level inverter; proportional-resonant controller; sinusoidal modulation; vector control; voltage ripple.

1. Introduction

Extensive research has been carried out on two-level and three-level inverters for DC–AC power conversion [1, 2]. In a two-level inverter, the mid-point of each leg can be connected to either the positive DC terminal or the negative DC terminal. In a three-level neutral-point-clamped (NPC) inverter, the mid-point of each leg could also be connected to the DC-bus mid-point, otherwise known as the DC-bus neutral [3, 4].

The NPC inverter offers several advantages over the traditional two-level inverter. With devices of the same voltage rating, this inverter can handle higher DC-bus voltage. Hence, this finds application in medium-voltage application [5]. At the same DC-bus voltage, each device blocks only half the DC-bus voltage in the off state. Therefore, the voltage stress on each device is reduced. Hence, the switching loss is reduced [2]. The NPC inverter is advantageous at high switching frequencies in low-voltage applications [2].

The NPC inverter has the ability of getting connected to the DC-bus midpoint as stated earlier. This capability leads to better waveform quality than that of a two-level inverter [6]. However, the connection to the mid-point also causes DC voltage imbalance due to injection of the load current into the DC bus during certain intervals. A number of methods have been devised to reduce this problem of voltage imbalance [7, 8].

The capacitor RMS current is important in both two-level and three-level inverters from the perspective of sizing and cost of the DC capacitor. The worst-case capacitor RMS current in either case can be obtained through repeated digital simulations of the converter under various operating conditions. However, it would be elegant to determine the worst-case capacitor RMS current through an analytical expression, relating the capacitor current to the operating conditions such as modulation index, line current amplitude and power factor.

Analytical expressions for the capacitor RMS current in a two-level inverter have been derived in [9, 10]. For a three-level inverter, this expression is more involved as there are three possible connections to the converter mid-point and more devices are involved. More recently, an expression has also been reported for the capacitor RMS current in a sinusoidally modulated three-phase NPC inverter [11, 12].

This paper derives such analytical expressions for single-phase half-bridge figure 1a, single-phase full-bridge figure 1b and three-phase three-leg figure 1c topologies of an NPC inverter. These analytical expressions are validated

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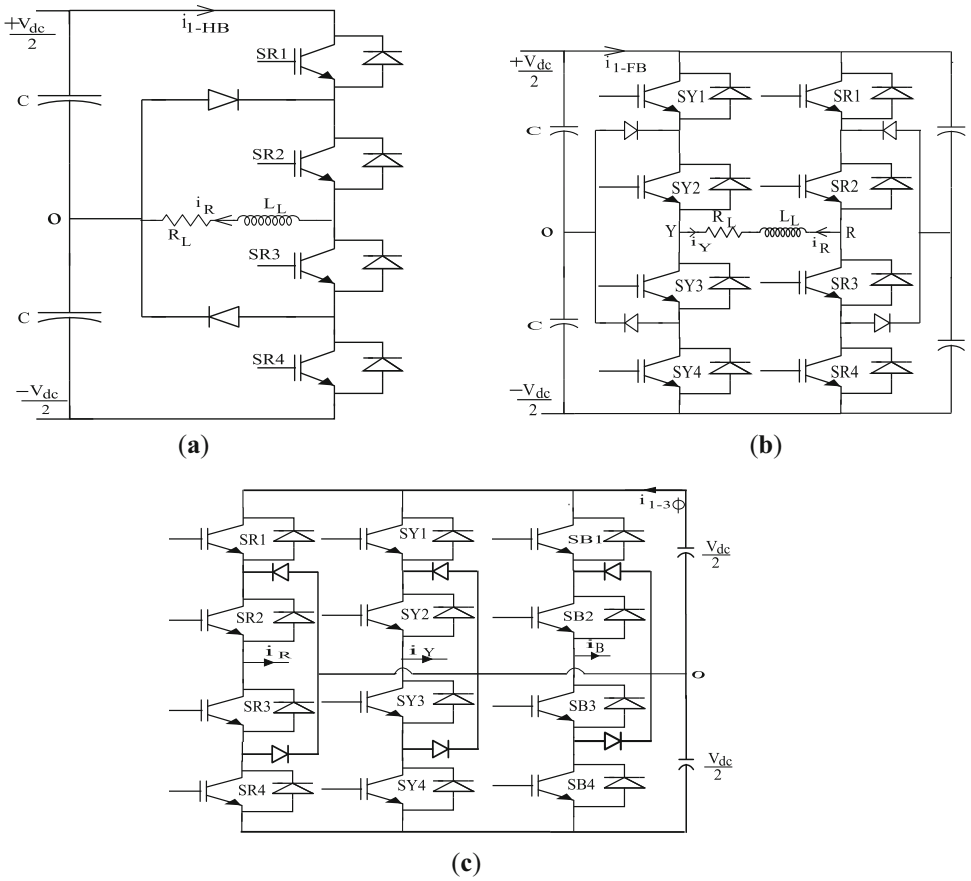


Figure 1. Topologies of neutral-point clamped inverters.

through extensive simulation and experimental studies, both under open-loop and closed-loop conditions.

Another stress on the DC capacitor is the voltage ripple, caused by the ripple current flowing through it [12, 13]. The capacitor voltage ripple is more dependent on the low-frequency current (e.g., third harmonic) than on high-frequency currents (i.e., switching frequency components) of the capacitor current [12, 14]. Closed-form expressions are derived here for the RMS values of low-frequency and high-frequency capacitor currents. An analytical expression is then derived to provide an estimate of the DC voltage ripple in a sinusoidally modulated three-phase NPC inverter. This is then validated experimentally at different modulation indices and power factor angles.

A preliminary version of this work was published [15], which reports only the analytical expression for capacitor RMS current pertaining to the three-leg topology and its experimental validation under open-loop conditions. This extended version reports such analytical expressions corresponding to all three topologies in figure 1, and also validates these expressions under open-loop as well as closed-loop conditions, as mentioned earlier. Further, the paper also includes evaluation of DC capacitor voltage ripple as indicated earlier.

2. Derivation of analytical expression for capacitor RMS current

Analytical closed-form expressions are derived for the capacitor RMS current pertaining to a single-phase half-bridge NPC inverter figure 1a, single-phase full-bridge NPC inverter figure 1b, and three-phase NPC inverter figure 1c in this section. Sine-triangle PWM is considered.

2.1 *Duty ratio*

In each leg of an NPC inverter, switches SR1 and SR3 are complementary, and switches SR2 and SR4 are also complementary [4]. The duty ratio d_{R1} of the top switch SR1 in the half-bridge inverter is given by

$$\begin{aligned} d_{R1} &= M\sin(\omega t), \\ d_{R1} &= 0, \end{aligned} \tag{1}$$

where M is the modulation index, and is also the peak duty ratio of the top switch; $\omega = 2\pi f$ and f is the fundamental frequency. The duty ratio d_{Y1} of the top switch SY1 in the single-phase full-bridge inverter is phase shifted by 180° from d_{R1} in (1), as indicated in figure 2a.

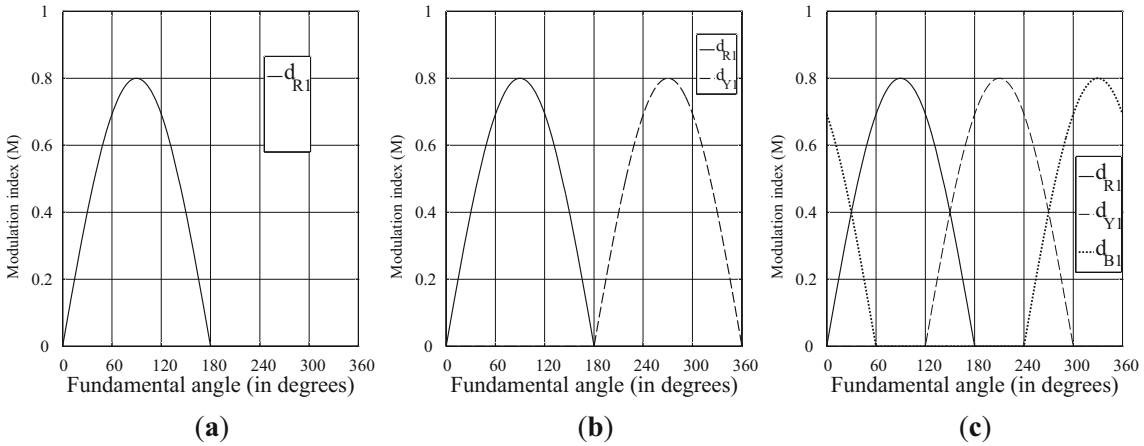


Figure 2. Plot of duty ratios of switches SR1, SY1 and SB1 for (**a**) single-phase, half-bridge, (**b**) single-phase, full-bridge and (**c**) three-phase NPC inverters.

Similarly, d_{Y1} and d_{B1} are the duty ratios of the top switches in the Y-phase and B-phase legs, respectively, in the three-phase inverter. These duty ratios d_{Y1} and d_{B1} are phase shifted by 120° and 240°, respectively, from the d_{R1} in (1). They are illustrated in figure 2, considering $M = 0.8$.

2.2 *Single-phase half-bridge inverter*

In a single-phase half-bridge inverter, the load current flows through the positive DC link only when the switch SR1 is on. Therefore the instantaneous DC-link current (i_{1-HB}) can be written as the product of switching function (S_{R1}) and load current (i_R) as follows:

$$i_{1-HB} = S_{R1} i_R. \tag{2}$$

Ignoring the harmonic components, the load current can be expressed as shown in (3), where ϕ is the fundamental power factor angle:

$$i_R = I_m \sin(\omega t - \phi). \tag{3}$$

Now, based on (1) and (3), the fundamental-cycle-average of the DC-link current (I_{avg-HB}) can be evaluated as follows:

$$I_{avg-HB} = \frac{1}{2\pi}\int_0^{\pi} d_{R1} i_R \, \mathrm{d}\omega t = \frac{MI_m}{4}\cos(\phi). \tag{4}$$

Similarly, the expression for DC-link RMS current (I_{rms-HB}) can be found as follows:

$$I_{rms-HB} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} d_{R1} i_R^2 \, \mathrm{d}\omega t} = \sqrt{\frac{MI_m^2}{2\pi}\left(1 + \frac{\cos(2\phi)}{3}\right)}. \tag{5}$$

The expressions for the DC-link RMS and average currents obtained in (5) and (4), respectively, are used to derive an expression for the DC-link capacitor RMS current (I_{c-HB}) as shown below:

$$I_{c-HB} = \sqrt{I_{rms-HB}^2 - I_{avg-HB}^2} \tag{6}$$

$$I_{c-HB} = \sqrt{MI_m^2\left(\frac{1}{2\pi}\left(1 + \frac{\cos(2\phi)}{3}\right) - \frac{M}{16}\cos^2(\phi)\right)}. \tag{7}$$

The normalized capacitor current is plotted as a function of modulation index at different power factors of 0, 0.2, 0.4, 0.6, 0.8 and 1 in figure 3a. As seen, the capacitor RMS current increases with power factor for a fixed modulation index. Also, for a given power factor, the capacitor RMS current increases with modulation index. Thus the maximum RMS current flows through the capacitor when the power factor is unity and the modulation index is 1. The maximum capacitor RMS current in half-bridge inverter is found to be 0.38 times the peak load current.

2.3 *Single-phase full-bridge inverter*

The instantaneous DC-link current (i_{1-FB}) and the fundamental-cycle-average DC-link current (I_{avg-FB}) of a single-phase full-bridge inverter are expressed as shown here. S_{R1} and S_{Y1} are the switching functions of the switches SR1 and SY1, respectively.

$$i_{1-FB} = S_{R1} i_R + S_{Y1} i_Y, \tag{8}$$

$$I_{avg-FB} = \frac{1}{2\pi}\int_0^{2\pi} (d_{R1} i_R + d_{Y1} i_Y) \, \mathrm{d}\omega t. \tag{9}$$

Since the operation of the full-bridge inverter is symmetrical, it is sufficient to consider the interval $0 \le \omega t \le \pi$ for analysis. Based on symmetry, Eq. (9) can be simplified, and I_{avg-FB} can be evaluated as shown in (10):

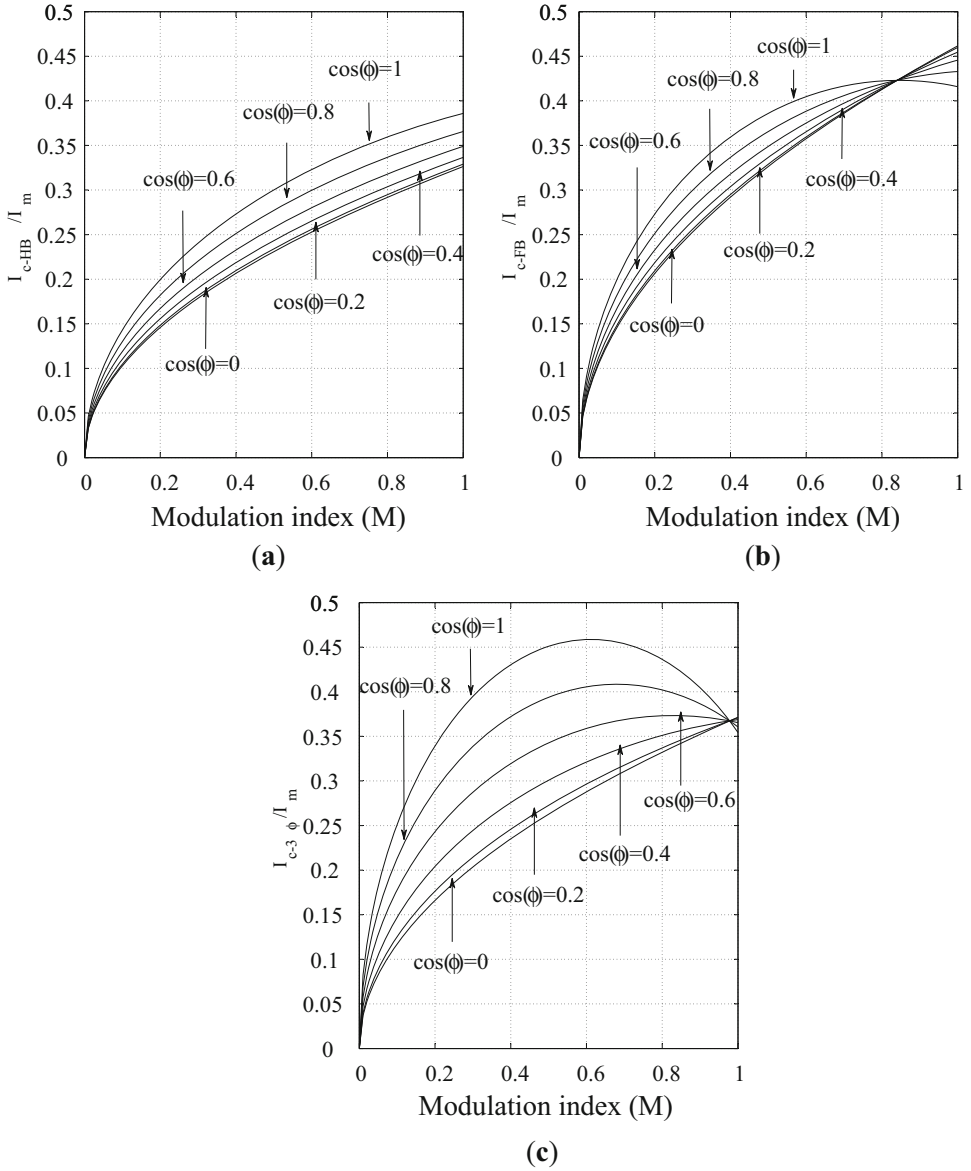


Figure 3. Variation of capacitor RMS current with modulation index and power factor (**a**) single-phase, half-bridge NPC inverter (**b**) single-phase, full-bridge NPC inverter and (**c**) three-phase NPC inverters.

$$I_{avg-FB} = \frac{1}{\pi}\int_0^{\pi} d_{R1} i_R \, \mathrm{d}\omega t = \frac{MI_m}{2}\cos(\phi). \tag{10}$$

Further, an expression for DC-link RMS current (I_{rms-FB}) can be derived as follows:

$$I_{rms-FB} = \sqrt{\frac{1}{\pi}\int_0^{\pi} d_{R1} i_R^2 \, \mathrm{d}\omega t} = \sqrt{\frac{MI_m^2}{\pi}\left(1+\frac{\cos(2\phi)}{3}\right)}. \tag{11}$$

An expression for the DC-link capacitor RMS current (I_{c-FB}) can be obtained using the expressions for the DC-link RMS and average currents obtained in (11) and (10), respectively, as follows:

$$I_{c-FB} = \sqrt{I_{rms-FB}^2 - I_{avg-FB}^2} \tag{12}$$

$$I_{c-FB} = \sqrt{MI_m^2\left(\frac{1}{\pi}\left(1+\frac{\cos(2\phi)}{3}\right) - \frac{M}{4}\cos^2(\phi)\right)} \tag{13}$$

From figure 3b, it can be seen that the capacitor RMS current in a full-bridge inverter increases with power factor up to a modulation index of 0.83, and decreases thereafter with increase in power factor. The maximum capacitor

RMS current is 0.462 times the peak load current. This happens when the power factor is zero, and the modulation index is unity.

2.4 *Three-phase NPC inverter*

Ignoring the switching frequency harmonics, the pole currents i_R, i_Y and i_B for the three-phase topology are defined as follows:

$$\begin{aligned} i_R &= I_m sin(\omega t - \phi), \\ i_Y &= I_m sin(\omega t - \frac{2\pi}{3} - \phi), \\ i_B &= I_m sin(\omega t + \frac{2\pi}{3} - \phi). \end{aligned} \tag{14}$$

2.4a *DC bus current*: The instantaneous DC-link current, which is the sum of all top switch currents, is given as follows:

$$i_{1-3\phi} = i_R S_{R1} + i_Y S_{Y1} + i_B S_{B1}. \tag{15}$$

In this expression, S_{R1}, S_{Y1} and S_{B1} are the switching functions of the switches SR1, SY1 and SB1, respectively, in figure 1c.

2.4b *Average DC bus current*: Since the three-phase duty ratios and three-phase currents are symmetric, an expression for the fundamental-cycle-average DC-link current ($I_{avg-3\phi}$) can be derived as shown by the following equations:

$$I_{avg-3\phi} = \frac{1}{2\pi}\int_0^{2\pi} (i_R S_{R1} + i_Y S_{Y1} + i_B S_{B1})\,\mathrm{d}\omega t, \tag{16}$$

$$I_{avg-3\phi} = \frac{3}{2\pi}\left(\int_0^{\frac{2\pi}{3}} d_{R1} i_R\,\mathrm{d}\omega t + \int_0^{\frac{\pi}{3}} d_{B1} i_B\,\mathrm{d}\omega t\right), \tag{17}$$

$$I_{avg-3\phi} = \frac{3MI_m}{4}\cos(\phi). \tag{18}$$

2.4c *RMS DC-link current*: The RMS DC-link current ($I_{rms-3\phi}$) for a three-phase inverter can be expressed as follows:

$$I_{rms-3\phi} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} (i_R S_{R1} + i_Y S_{Y1} + i_B S_{B1})^2\,\mathrm{d}\omega t}. \tag{19}$$

By virtue of three-phase symmetry, Eq. (19) reduces to the following equation:

$$I^2_{rms-3\phi} = \frac{3}{2\pi}\int_0^{2\pi} (S^2_{R1} i^2_R + 2S_{R1}S_{B1} i_R i_B)\,\mathrm{d}\omega t. \tag{20}$$

Square of a switching function is the same as the switching function. Further, the switching function S_{R1} is always zero between π and 2π (see figure 2). Similarly, S_{B1} is always zero between $\pi/3$ and $4\pi/3$. Hence

$$I^2_{rms-3\phi} = \frac{3}{2\pi}\left(\int_0^{\pi} S_{R1} i^2_R\,\mathrm{d}\omega t + \int_0^{\frac{\pi}{3}} 2S_{R1}S_{B1} i_R i_B\,\mathrm{d}\omega t\right). \tag{21}$$

From table 1, the product of the switching function $S_{R1}S_{B1}$ reduces to either S_{R1} or S_{B1} in different intervals as follows:

$$\begin{aligned} S_{R1}S_{B1} &= S_{R1}, \\ S_{R1}S_{B1} &= S_{B1}, \end{aligned} \tag{22}$$

Then, based on (21) and (22),

$$\begin{aligned} I^2_{rms-3\phi} = \frac{3}{2\pi}\Bigg(&\int_0^{\pi} S_{R1} i^2_R\,\mathrm{d}\omega t + \int_0^{\frac{\pi}{6}} 2S_{R1} i_R i_B\,\mathrm{d}\omega t \\ &+ \int_{\frac{\pi}{6}}^{\frac{\pi}{3}} 2S_{B1} i_R i_B\,\mathrm{d}\omega t\Bigg). \end{aligned} \tag{23}$$

Now, the DC-link RMS current can be rewritten in terms of the three-phase duty ratios as follows:

$$\begin{aligned} I^2_{rms-3\phi} = \frac{3}{2\pi}\Bigg(&\int_0^{\pi} d_{R1} i^2_R\,\mathrm{d}\omega t + \int_0^{\frac{\pi}{6}} 2d_{R1} i_R i_B\,\mathrm{d}\omega t \\ &+ \int_{\frac{\pi}{6}}^{\frac{\pi}{3}} 2d_{B1} i_R i_B\,\mathrm{d}\omega t\Bigg). \end{aligned} \tag{24}$$

By evaluating the integrals in (24), an expression for the DC-link RMS current is obtained as follows:

$$I_{rms-3\phi} = \sqrt{\frac{3I^2_m M(\sqrt{3} + \cos(2\phi)\frac{2}{\sqrt{3}})}{4\pi}} \tag{25}$$

2.4d *DC-link capacitor RMS current*: Using the expressions for the DC-link RMS and average currents obtained in (25) and (18), respectively, an expression for the DC-link capacitor RMS current ($I_{c-3\phi}$) can be derived as follows:

$$I_{c-3\phi} = \sqrt{\frac{3I^2_m M}{4\pi}\left(\sqrt{3} + \left(\frac{2}{\sqrt{3}}\right)\cos(2\phi)\right) - \frac{9}{16}(I_m M)^2\cos^2(\phi)}. \tag{26}$$

In the case of three-phase three-level inverter, as can be seen from figure 3c, the capacitor RMS current increases with power factor in the modulation index range $M < 0.95$; the capacitor RMS current decreases with increase in power factor in the range $0.95 < M < 1$. The maximum capacitor RMS current is 0.459 times the maximum load current; this

Table 1. Switching functions of the switches in the three legs.

Angular duration	S_{R1}	S_{Y1}	S_{B1}	$S_{R1}S_{Y1}$	$S_{Y1}S_{B1}$	$S_{B1}S_{R1}$
$0 \le \omega t < \frac{\pi}{6}$	0, 1	0	0, 1	0	0	S_{R1}
$\frac{\pi}{6} \le \omega t < \frac{\pi}{3}$	0, 1	0	0, 1	0	0	S_{B1}
$\frac{\pi}{3} \le \omega t < \frac{\pi}{2}$	0, 1	0	0	0	0	0
$\frac{\pi}{2} \le \omega t < \frac{2\pi}{3}$	0, 1	0	0	0	0	0

happens at unity power factor and a modulation index of 0.61. Thus, the capacitor RMS current is close to 46 per cent of the peak load current in case of single-phase full-bridge as well as three-phase NPC inverters. It is noteworthy that the capacitor RMS current rating is comparable for the single-phase and three-phase cases for the same current rating, despite the higher power handling capability of the three-phase inverter.

The analysis here is applied to three-level converters with one, two and three legs. This can certainly be extended to three-level converters with any number of legs (e.g., multiphase motor drives) or multiple converters connected to a common DC bus. Also, the above analysis ignores dead-time effect as this is not expected to be significant at the operating conditions considered here. At high switching frequencies, when the ratio of dead time to switching period is considerable, the dead-time effect could be incorporated into the analysis, extending the approach in [16] for two-level converters.

3. Simulated and experimental results under open-loop conditions

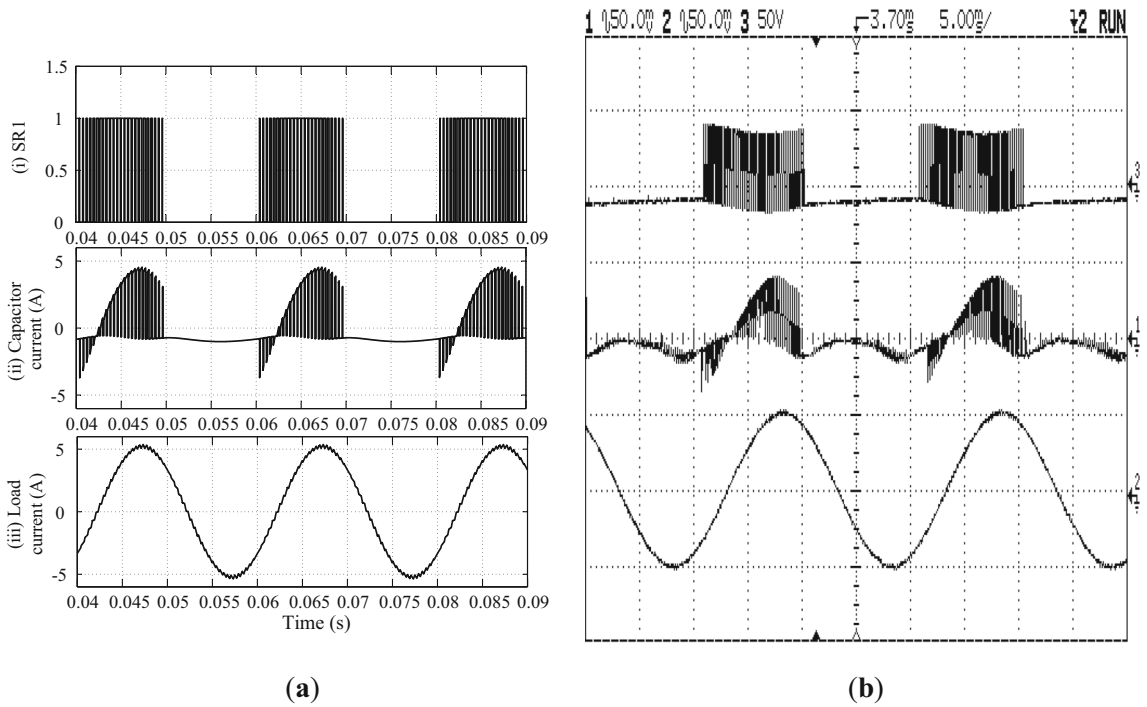
The analytical expressions derived in the previous section are first validated through simulations and measurements under open-loop operation of the NPC inverter.

3.1 *Simulated and experimental waveform*

A single-phase half-bridge NPC inverter, realized using one leg of an NPC inverter, is simulated using MATLAB Simulink. The devices are assumed to be ideal. The inverter is switched using sine-triangle PWM (see section 2.1) at a carrier frequency of 1.5 kHz. The ac load is considered as a sinusoidal current sink. The simulated waveforms of the gating pulses to the top device (i.e., S_{R1}), the DC capacitor current and the load current are shown in figure 4a for a modulation index M of 0.8, peak load current I_m of 5 A, and load power factor of 0.8 (lag).

The experimental waveforms, corresponding to the simulated ones in figure 4, are presented in figure 4b. The experimental NPC inverter is built with SEMIKRON SK150MLI066T (150 A/1200 V) IGBTs. Each leg consists of two 4700 uF, 450 V, 13 A electrolytic capacitors in series. The DC source is an Agilent 6035A (0–500V, 0–5 A, 1000 W) programmable power supply. The capacitor current is measured using a Fluke 1400S current probe. A TMS320F2407-DSP-processor-based digital controller is used for control implementation and generation of gating pulses.

The simulated and experimental sets of waveforms, corresponding to a single-phase full-bridge inverter, are shown in figure 5a and b, respectively, for M = 0.8, $\cos(\phi) = 0.8$ (lag) and $I_m = 5$ A. This full-bridge inverter is realized using two NPC inverter legs, described earlier.



(a) (b)

Figure 4. (**a**) Simulated waveforms of gating pulses to top device SR1, DC capacitor current and load current in a single-phase, half-bridge NPC inverter at $M = 0.8$ and $\cos\phi = 0.8$ (lag). (**b**) Experimental gating pulses to top device SR1 (trace 3), DC capacitor current (trace 1) load current (trace 2) in a single-phase, half-bridge NPC inverter at $M = 0.8$ and $\cos\phi = 0.8$ (lag), [scale: trace 3, 10 V/division; Trace 2, 5 A/division; Trace 1, 5 A/division].

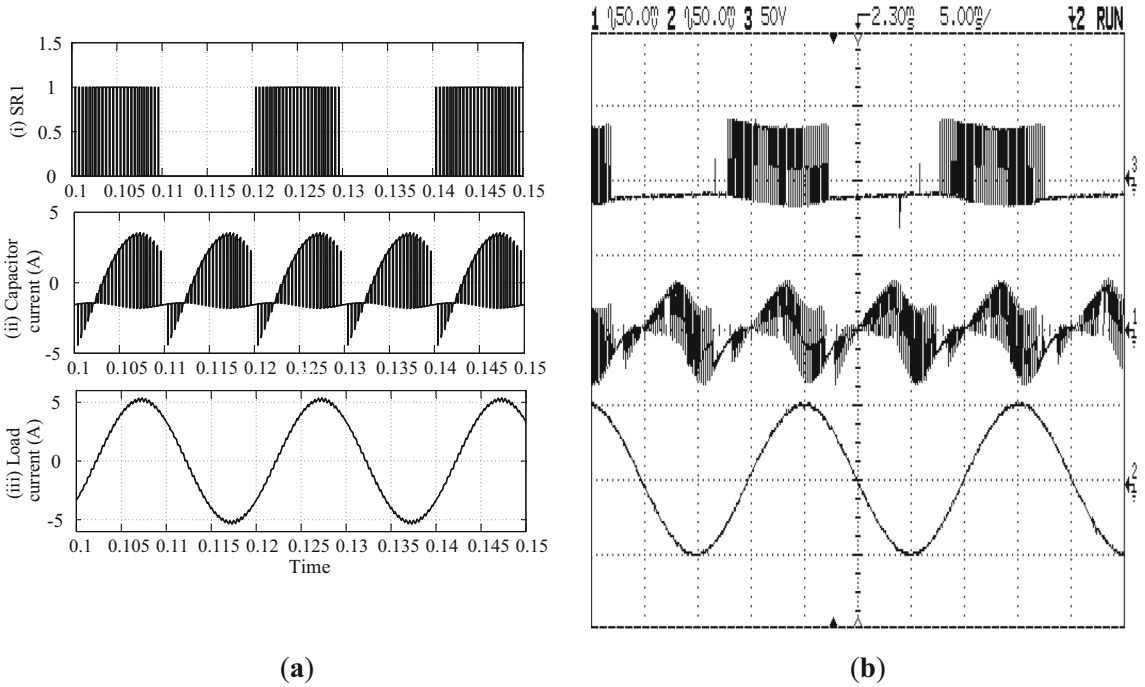


Figure 5. (**a**) Simulated waveforms of gating pulses to top device SR1, DC capacitor current and load Current in a single-phase, full-bridge NPC inverter at $M = 0.8$ and cos $\phi = 0.8$ (lag). (**b**) Experimental gating pulses to top device SR1 (trace 3), DC capacitor current (trace 1) and load current (trace 2) in a single-phase, full-bridge NPC inverter at $M = 0.8$ and cos $\phi = 0.8$ (lag), [scale: trace 3, 10 V/division; trace 2, 5 A/division; Trace 1, 5 A/division].

Similarly, the simulated waveforms pertaining to the three-phase NPC inverter at $M = 0.61$ and $cos(\phi) = 0.4$ (lag) are presented in figure 6a. Similar results at $M = 0.61$, but a different power factor of 0.8 (lag), are shown in figure 6b. Figure 7a and b presents the experimental results corresponding to figure 6a and b, respectively.

As one can see, the simulated and experimental waveforms agree reasonably well though certain differences are evident. While the simulations consider the DC voltage to be constant, there is a ripple in the DC voltage in the actual case. Apart from such inevitable differences between the simulation model and the actual system, the bandwidth of the current probe is also limited to accurately capture the DC capacitor current pulses with fast rising/falling edges and rather short widths. Hence the simulated and measured DC capacitor current waveforms appear different. However, the distortions caused by the measurement system are mostly limited to the high frequency components (such as related to the edges of the pulses). The low frequency components, which are dominant, are measured with reasonable precision. This is borne out by the fact that the capacitor RMS currents based on analysis, simulation and measurements are in good agreements as shown in the following sections.

3.2 *Validation of analytical expressions for capacitor current*

For the single-phase half-bridge, single-phase full-bridge and three-phase full-bridge topologies, capacitor RMS current is evaluated through simulation at different operating conditions as indicated in table 2. The various operating conditions include different modulation indices, different power factors and different values of peak load current as seen from the table. The capacitor RMS current is also measured at each of these operating conditions. The simulated and experimental values are compared with analytically obtained ones (based on the expressions in section 2) in table 2. As seen, the values predicted by the analytical expressions are in good agreement with the simulated and measured values.

4. Simulation and experimental results under closed-loop conditions

Closed-loop control is implemented for the three topologies. The capacitor RMS current is measured at different operating conditions under closed-loop control. The simulated and measured values of capacitor RMS current under closed-loop control are compared with the analytically predicted values in this section.

4.1 *Closed-loop current control*

A proportional resonant (PR)-controller-based current control [17] is implemented on a single-phase half-bridge

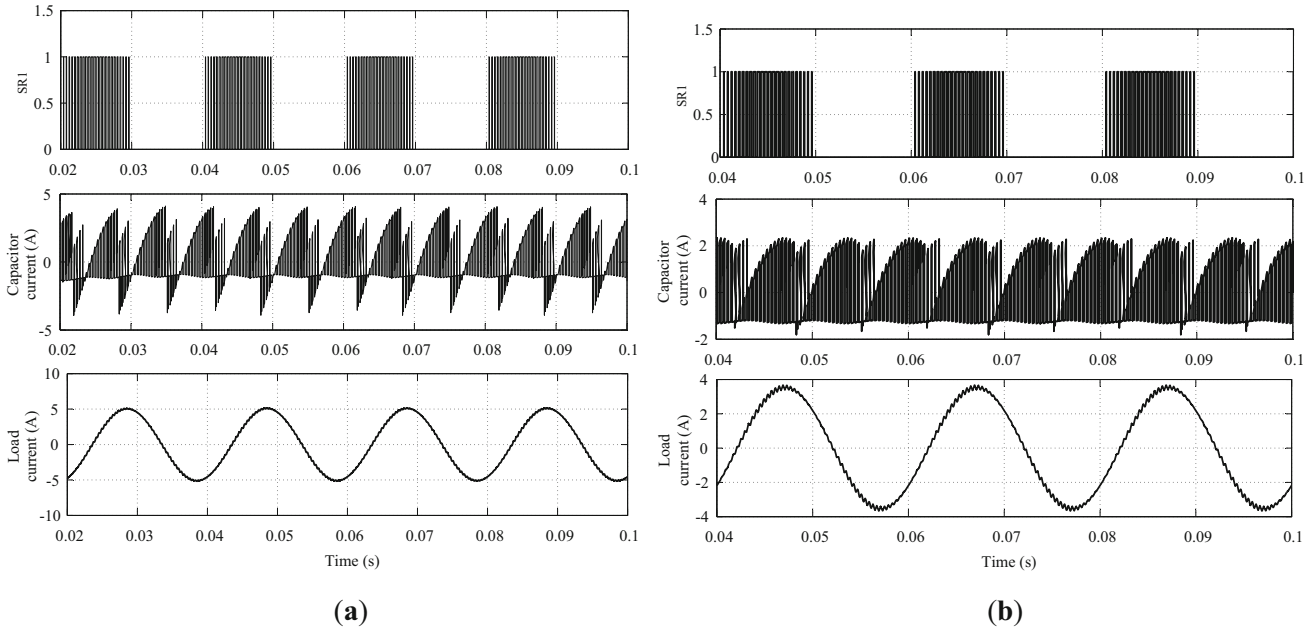


Figure 6. Simulated waveforms of gating pulses to top device SR1, DC capacitor current and load current in a three-phase, NPC inverter at (**a**) $M = 0.61$, cos $\phi = 0.4$ (lag) and (**b**) $M = 0.61$, cos $\phi = 0.8$ (lag).

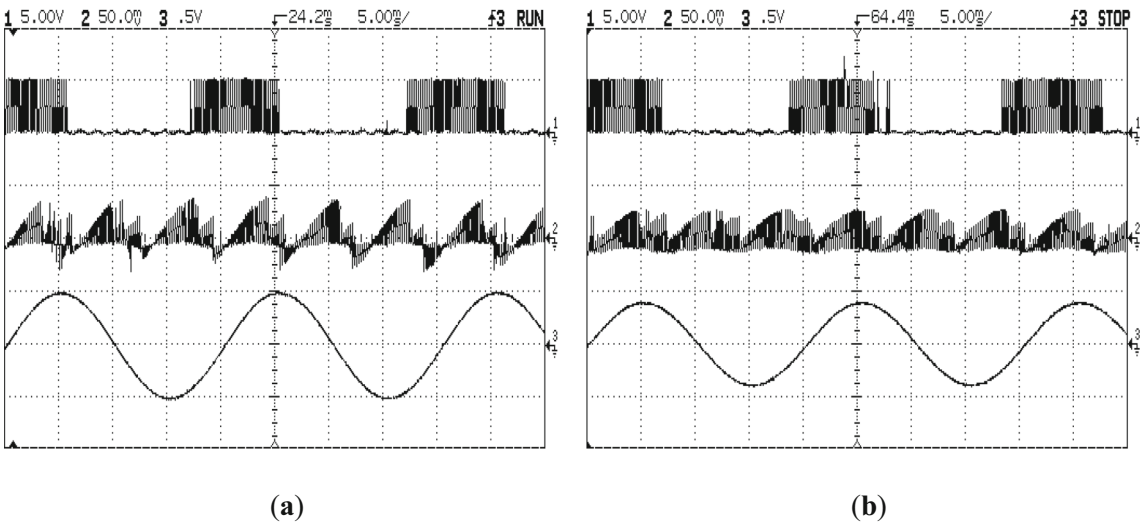


Figure 7. Experimental gating pulses to top device SR1 (trace 1), DC capacitor current (trace 2) and load current in a three-phase NPC inverter (trace 3) at (**a**) $M = 0.61$, cos $\phi = 0.4$ (lag) and (**b**) $M = 0.61$, cos $\phi = 0.8$ (lag), [scale: trace 1, 10 V/division; trace 2, 5 A/division; Trace 3, 5 A/division].

inverter. The PR controller has a transfer function as shown in (27), where ω_o is the resonant frequency:

$$G_s = K_p + \frac{2K_i s}{s^2 + \omega_o^2} \tag{27}$$

The controller parameters K_p and K_i are selected as discussed in [17], considering $\omega_o = 314$ rad/s and carrier frequency $f_c = 10$ kHz. The measured dynamic response of the current controller to a step change in current reference is shown by the oscillogram in figure 8. As seen from the experimental result, the dynamic response of the controller is satisfactory.

The PR current controller for the single-phase, full-bridge inverter is also designed along similar lines. Figure 9 shows the dynamic response of the experimental system to a step change in the current reference. As seen. the dynamic response is satisfactory.

Table 2. Analytical, simulated and experimental values of capacitor RMS currents for three topologies with open-loop control.

Topology	M	ϕ (lag)	I_m(A)	Capacitor RMS current (A)		
				Analytical	Simulation	Expt
1-phase	1	28.8°	2.04	0.76	0.88	0.80
half-	1	46.1°	3.5	1.25	1.40	1.25
bridge	0.75	80.6°	2.9	0.84	0.80	0.76
	0.75	27.4°	1.5	0.51	0.54	0.52
	0.5	25.9°	1.0	0.28	0.29	0.27
	0.5	77.0°	2.5	0.59	0.58	0.52
1-phase	1	18.7°	2.33	0.98	0.89	0.91
full-	1	29.5°	3.1	1.32	1.3	1.15
bridge	1	38.2°	3.4	1.49	1.45	1.32
	0.75	40.3°	2.5	1.05	1.03	0.94
	0.75	66.2°	3.7	1.51	1.49	1.34
	0.75	21.4°	1.3	0.54	0.52	0.50
	0.5	21.6°	1.1	0.43	0.43	0.40
	0.5	39.6°	2.3	0.83	0.81	0.77
	0.5	57.6°	3.2	1.11	1.11	0.98
	0.25	56.2°	1.9	0.49	0.47	0.41
	0.25	66.9°	2.3	0.55	0.53	0.46
	0.25	30.2°	1.1	0.30	0.28	0.27
3-phase	0.18	59.0°	2.9	0.63	0.63	0.52
full-	0.35	27.4°	3.0	1.14	1.14	1.00
bridge	0.47	33.8°	3.5	1.39	1.39	1.38
	0.28	37.4°	3.2	1.05	1.10	0.90
	0.228	63.4°	3.4	0.76	0.72	0.67
	0.4	31.7°	3.2	1.23	1.19	1.19
	0.9	82.0°	4	1.41	1.42	1.42
	0.9	33.2°	4	1.56	1.55	1.58
	0.8	82°	4	1.34	1.34	1.33
	0.8	33.2°	4	1.64	1.64	1.64
	0.7	82°	4	1.26	1.26	1.23
	0.7	33.2°	4	1.67	1.66	1.65
	0.6	82°	4	1.17	1.17	1.15
	0.6	33.2°	4	1.66	1.66	1.64
	0.5	82°	4	1.07	1.07	1.05

For the three-phase NPC inverter, closed-loop control is implemented in the synchronously revolving d–q reference frame [18]. The three-phase currents (i_R, i_Y and i_B) are transformed into the synchronous reference frame (SRF) as d-axis and q-axis currents, namely i_d and i_q. Closed-loop control is implemented for both i_d and i_q [18]. The PI controller parameters for the two current controllers are chosen based on [18].

Figure 10a and b shows the dynamic response of the current controller for the three-phase NPC inverter. The d-axis current reference is set to zero. The q-axis current reference is used to obtain the desired peak value of load current. When the q-axis current reference is changed, the actual q-axis current and the actual load current change at a large rate and settle down at a new value.

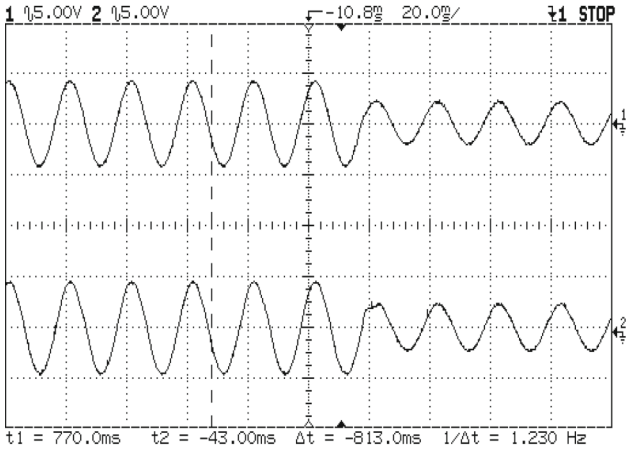


Figure 8. Half bridge inverter current controller response: (i) Reference current and (ii) load current; scale: trace 1: 5 A/division; trace 2: 5 A/division.

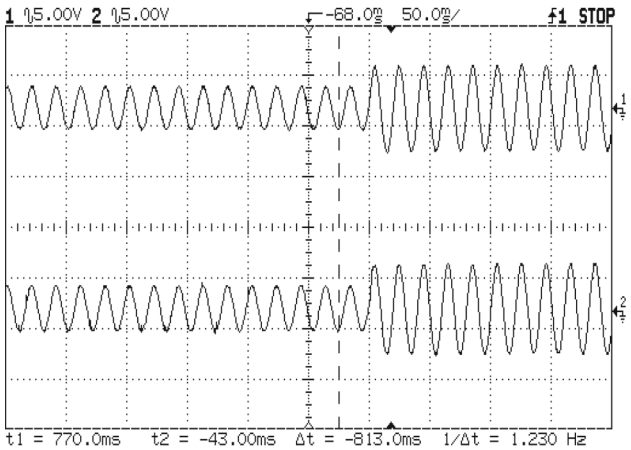


Figure 9. Full bridge inverter current controller response: (i) Reference current and (ii) load current, scale: trace 1: 5 A/division; trace 2: 5 A/division.

4.2 *Validation of analytical expression for capacitor current*

The three topologies are simulated under closed loop conditions using MATLAB Simulink. The simulated values of capacitor RMS current at different operating points are tabulated in table 3.

The capacitor RMS current is also measured in case of all three topologies at different operating conditions. These results are also tabulated in table 3. As seen from table 3, the analytical, simulated and measured values of the DC capacitor current are in close agreement at the various operating points.

Thus, the closed-form analytical expressions for the capacitor RMS current, derived in section 2, are validated both through simulations and actual measurements. The

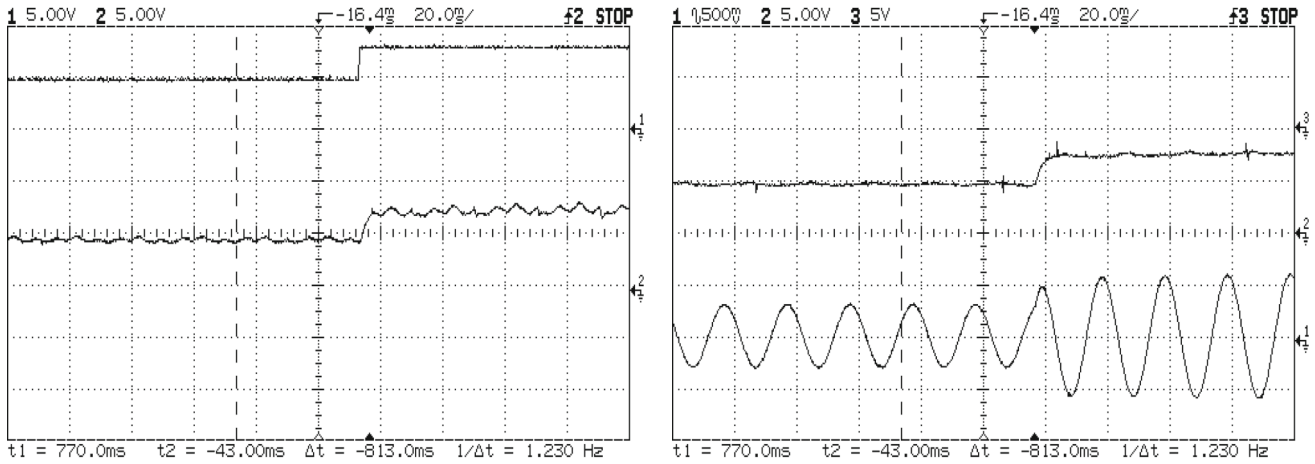


Figure 10. Three-phase inverter-current controller response, scale: trace 1: 5 A/division and Trace 2: 5 A/division. (**a**) Experimental waveforms: (i) q-axis current reference and (ii) q-axis current. (**b**) Experimental waveforms: (i) q-axis current and (ii) load current.

Table 3. Analytical, simulated and experimental values of capacitor RMS currents for three topologies with closed-loop control.

Topology	M	ϕ (lag)	I_m(A)	Capacitor RMS current (A)		
				Analytical	Simulation	Expt
1-phase half-bridge	1	63.4°	2.9	0.98	1.0	0.97
	1	18.3°	1.4	0.52	0.52	0.54
	1	34.2°	2.6	0.96	0.98	0.98
	0.75	12.9°	0.7	0.25	0.25	0.24
	0.75	61.7°	3.0	0.89	0.85	0.81
	0.75	35.0°	1.9	0.63	0.63	0.55
	0.5	27.3°	1.1	0.32	0.32	0.31
	0.5	18.5°	0.7	0.22	0.22	0.21
	0.5	61.7°	2.0	0.49	0.49	0.43
	0.25	28.2°	0.53	0.11	0.11	0.10
	0.25	65.8°	1.1	0.19	0.18	0.18
	0.25	48.1°	0.9	0.17	0.17	0.17
1-phase full-bridge	0.25	78.5°	2.5	0.57	0.57	0.50
	0.25	75.9°	3.4	0.79	0.77	0.70
	0.25	53.3°	2.5	0.64	0.63	0.59
	0.5	10.3°	1.6	0.62	0.59	0.55
	0.5	24.3°	3.7	1.37	1.34	1.25
	0.5	27.1°	3.4	1.29	1.26	1.19
	0.75	29.5°	3.5	1.44	1.45	1.37
	0.75	45.2°	5	2.05	2.1	1.94
	0.75	19.2°	2.44	1.02	1.03	0.97
	1	69.7°	3.5	1.59	1.59	1.57
	1	12.9°	2.1	0.89	0.87	0.96
	1	45.2°	4.9	2.16	2.19	2.20
3-phase full-bridge	0.45	27.3°	2.28	0.93	0.89	0.95
	0.32	44.6°	3.4	1.04	1.11	1.07
	0.486	16.6°	3.0	1.31	1.29	1.20
	0.63	18.7°	3.2	1.42	1.37	1.35
	0.21	48.9°	2.3	0.61	0.63	0.60

capacitor RMS current contains both low-frequency and high-frequency components. The RMS values of the low-frequency and high-frequency components are analyzed in the following section.

5. Analysis of low-frequency and high-frequency capacitor current

To evaluate the low-frequency components in the DC-capacitor current, one can consider the switching-cycle-average $i_{C1,avg}$ defined as follows:

$$i_{C1,avg} = i_{1,avg} - I_{avg-3\phi} \tag{28}$$

where $I_{avg-3\phi}$ is the average DC-link current over a fundamental cycle as derived in (18). Since the capacitor current has a periodicity of 120°, considering the interval $0° < \omega t < 120°$, the switching-cycle-average ($i_{1,avg}$) can be expressed as follows:

$$\begin{aligned} i_{1,avg} &= d_{R1} i_R + d_{B1} i_B, \quad 0° < \omega t < 60°, \\ &= d_{R1} i_R, \quad 60° < \omega t < 120°. \end{aligned} \tag{29}$$

Based on Eqs. (28), (29), (18), (14) and (1), the switching-cycle-average capacitor-current $i_{C1,avg}$ is expressed as shown in (30):

$$\begin{aligned} i_{C1,avg} &= \frac{M}{4} I_m[\cos(\phi) + 2\cos(2\omega t - \frac{4\pi}{3} - \phi)], \qquad 0° < \omega t < 60°, \\ i_{C1,avg} &= -\frac{M}{4} I_m[\cos(\phi) + 2\cos(2\omega t - \phi)], \qquad 60° < \omega t < 120°. \end{aligned} \tag{30}$$

Further, the RMS value of the low-frequency capacitor current components can be evaluated as follows:

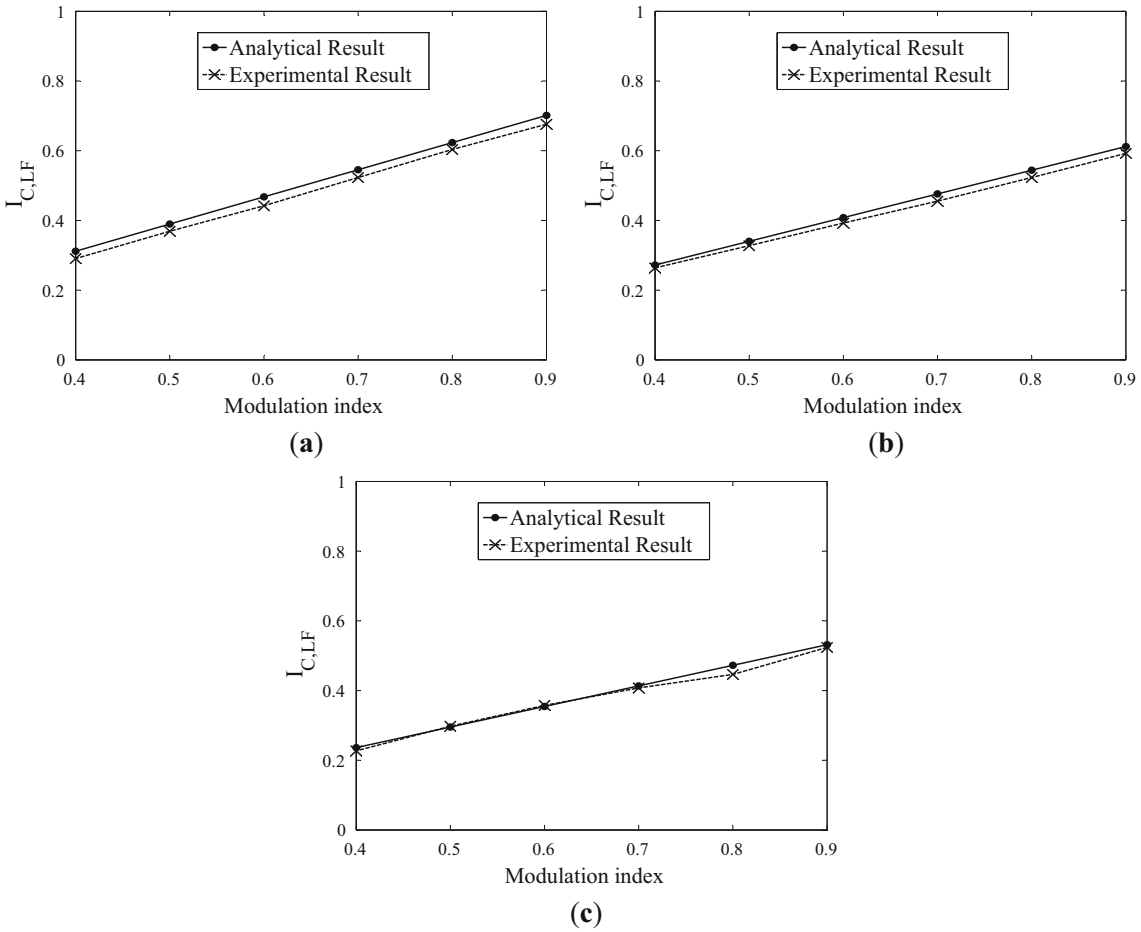


Figure 11. Analytical and experimental values of low-order harmonic RMS current for SPWM scheme at lagging power factors of (**a**) 0.249, (**b**) 0.669 and (**c**) 0.866.

$$I_{C,LF}^2 = \frac{3}{2\pi}\int_0^{2\pi/3} i_{C1,avg}^2\, d\omega t = \frac{9M^2I_m^2}{16\pi^2}\left[\cos^2(\phi)\left(\frac{\pi}{3}-\sqrt{3}\right)+\frac{2\pi}{3}-\frac{\sqrt{3}}{2}\right]. \quad (31)$$

The RMS value of the high-frequency capacitor current is obtained as shown in (32), where $I_{c-3\phi}$ is the total RMS current through the DC-link capacitor, the expression for which is derived earlier in (26):

$$I_{C,HF}^2 = I_{c-3\phi}^2 - I_{C,LF}^2. \quad (32)$$

Substituting the expressions for $I_{c-3\phi}$ and $I_{C,LF}$ from (26) and (31), respectively, the following expression for the high-frequency RMS capacitor current can be derived:

$$I_{C,HF}^2 = \frac{3I_m^2M}{4\pi}\left(\sqrt{3}+\frac{2}{\sqrt{3}}\cos(2\phi)\right)-\frac{9}{16}I_m^2M^2\cos^2(\phi) - \frac{9M^2I_m^2}{16\pi^2}\left[\cos^2(\phi)\left(\frac{\pi}{3}-\sqrt{3}\right)+\frac{2\pi}{3}-\frac{\sqrt{3}}{2}\right]. \quad (33)$$

The voltage ripple contributed by the low-frequency and high-frequency components of the capacitor current is discussed in the next section.

6. Estimation of capacitor voltage ripple

The total RMS value of all the low-frequency components in the DC capacitor current in a sinusoidally modulated three-phase NPC inverter can be expressed as shown in (30). As has been established previously [14], the principal low-frequency component in the DC capacitor current of a sinusoidally modulated NPC inverter is the third harmonic (i.e., $3f$) component. Hence, assuming $I_{C,LF}$ to be the RMS value of the $3f$ component, the voltage ripple V_{rms-LF} caused by the same can be evaluated as shown in (34), where C_{dc} is the DC link capacitance and ESR_3 is the equivalent series resistance seen by the third harmonic:

$$V_{rms-LF} = \sqrt{\left(\frac{I_{C,LF}}{2\pi(3f)C_{dc}}\right)^2 + (I_{C,LF} * ESR_3)^2}. \quad (34)$$

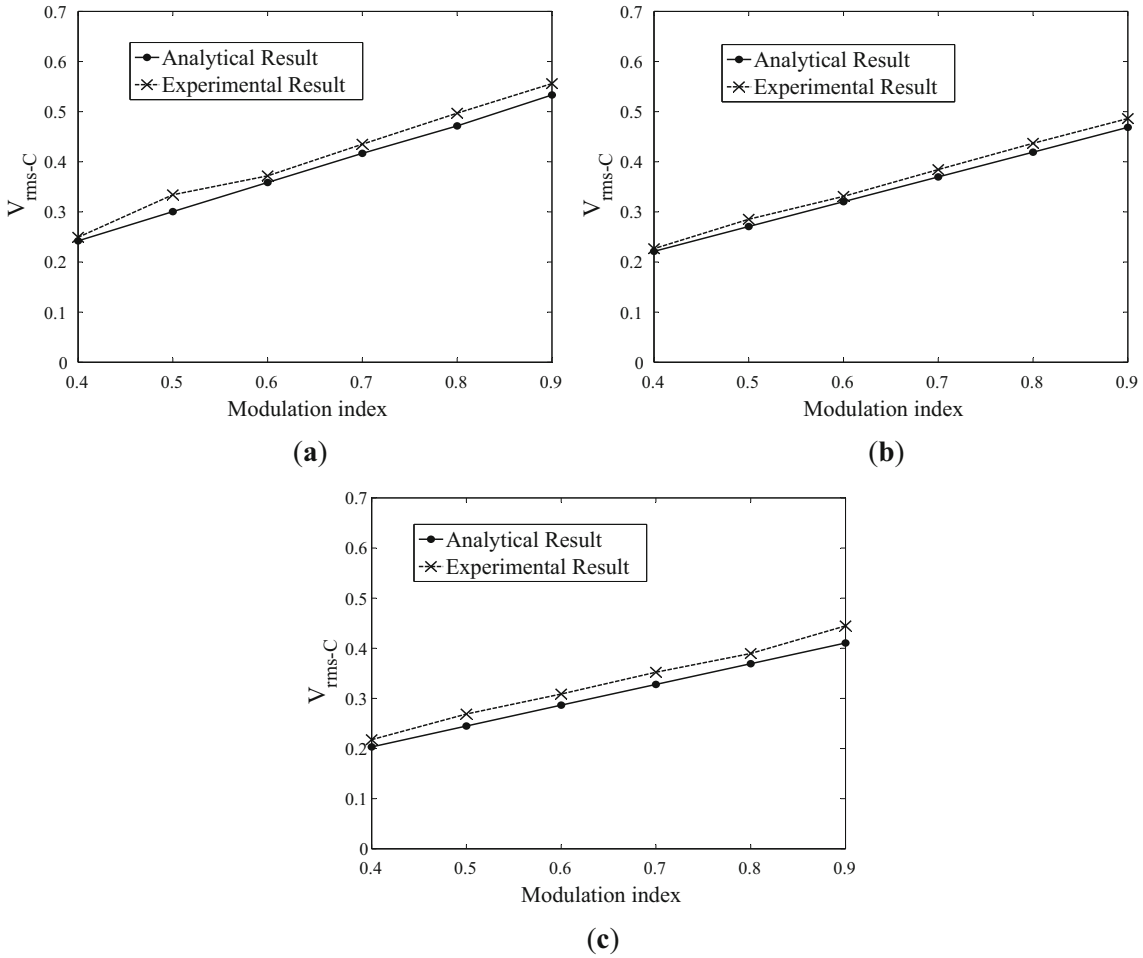


Figure 12. Analytical and experimental values of RMS voltage ripple for SPWM scheme at lagging power factors of (**a**) 0.249, (**b**) 0.669 and (**c**) 0.866.

The high-frequency capacitor current consists of components around integral multiples of switching frequency f_{sw}. The first side-band components (i.e., frequencies around f_{sw}) are more dominant than the other side bands [14]. Also, the capacitive reactances seen by the higher side-bands are much lower than that seen by the first side band. Further, the variation of ESR at high frequencies is not very significant [19]. Hence, the entire high-frequency capacitor current of RMS value $I_{C,HF}$ is assumed to be of switching frequency f_{sw} for the purpose of evaluating the RMS high-frequency voltage ripple as shown by (35), where ESR_{SF} is the ESR value at switching frequency f_{sw}:

$$V_{rms-HF} = \sqrt{\left(\frac{I_{C,HF}}{2\pi(f_{sw})C_{dc}}\right)^2 + (I_{C,HF} \times ESR_{SF})^2}. \quad (35)$$

The total RMS voltage ripple across the DC capacitor is evaluated further as follows:

$$V_{rms-C} = \sqrt{V_{rms-LF}^2 + V_{rms-HF}^2}. \quad (36)$$

7. Validation of analysis of voltage ripple

The experimental set-up consists of a MOSFET-based 3-kVA inverter. The capacitor bank consists of two sets of three parallel capacitors of value 470 μF each. The load consists of a three-phase *R–L* load. The load inductance per phase is fixed at 10 mH. The rheostat is varied to obtain the desired power factor angle. The controller platform is a TMS320LF2407A DSP processor. Sine-triangle PWM is considered as mentioned earlier. The switching frequency is 1.5 kHz. The DC-bus voltage is varied to maintain the load current at a constant amplitude of 3 A. The capacitor current is measured using a Fluke 1400S probe. The FFT of the measured capacitor current is carried out in the MATLAB platform. Considering the frequency components less than half of the switching frequency, the low-frequency capacitor RMS current is calculated. The analytically and experimentally obtained values of the low-frequency capacitor RMS current $I_{C,LF}$ are plotted in figure 11. As seen, the experimental and analytical results tally with each other reasonably well.

The voltage ripple across the capacitor is measured using a fluke multimeter. The analytical and experimental values of voltage ripple for SPWM scheme are shown plotted in figure 12. As seen from the plots, the experimental and analytical values agree reasonably well. Also, it is seen that the voltage ripple increases with both modulation index and power factor angle. Therefore, the voltage ripple is maximum when the power factor is zero, and the modulation index is 1.

8. Conclusions

Analytical expressions for the DC-link capacitor RMS current pertaining to single-phase half-bridge, single-phase full-bridge and three-phase three-level inverter topologies are derived, considering a sinusoidal PWM scheme. The analytical expressions for the three topologies are validated extensively, using simulation studies and experimental measurements, under both open-loop and closed-loop conditions. The analytical expressions yield the worst-case capacitor RMS current and the operating condition at which this occurs for all three topologies.

The capacitor RMS current is found to be the highest at the maximum modulation index and unity power factor for the half-bridge topology, whereas for the full-bridge topology at the maximum modulation index and zero power factor. For the three-phase NPC, on the other hand, the capacitor RMS current is maximum at a modulation index of 0.61 at unity power factor. The worst-case capacitor RMS current is always a percentage of the peak load current. This is 38 per cent of the peak load current for the half-bridge inverter, while it is 46 per cent for the other two topologies.

Analytical expressions are also derived for the RMS values of low-frequency and high-frequency capacitor currents for the sinusoidally modulated three-phase NPC inverter. These expressions are used to evaluate the voltage ripple across the DC capacitor at various operating conditions. Once again, these analytical results are validated through extensive measurements at different operating points.

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