International Collaboration in Packaging Education: Hands-on System-on-Package (SOP) Graduate Level Courses at Indian Institute of Science and Georgia Tech PRC

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Abstract

System-on-Package (SOP) continues to revolutionize the realization of convergent systems in microelectronics packaging. The SOP concept which began at the Packaging Research Center (PRC) at Georgia Tech has benefited its international collaborative partners in education including the Indian Institute of Science (IISc). The academic program for electronics packaging currently in the Centre for Electronics Design and Technology (CEDT) at IISc is aimed at educating a new breed of globally-competitive engineers in the new SOP technology to meet the next generation workforce need of global as well as the Indian electronics industry. This has been possible with the hands-on electronics packaging course being taught at IISc. The first-ever fundamental systems packaging textbook from the PRC, and in which IISc has been a partner has brought awareness among the engineering students as to the need for better packaging in electronic products and systems. This paper will highlight the electronics packaging scenario in India, the first-of-its-kind electronics packaging course curriculum in CEDT at the IISc, explain the benefits of research integration with education and look at how SOP technology and packaging education has helped to enrich the engineering students at the graduate level.

Introduction- System-on-Package (SOP)

System-On-Package is a new and emerging electronics system paradigm with applications not only for electronic systems but also for bio-medical systems [1]. It goes beyond System-on-Chip (SOC) and System-In-Package (SIP) technologies that are widely practiced in the industry. It overcomes the fundamental limits to computing and integration limits to wireless communications and to consumer electronics that SOC and SIP present. It began at the Georgia Institute of Technology's Packaging Research Center in 1993, funded by NSF as one of 20 National Centers, to both explore and develop, as well as to educate a new breed of engineers in this new technology. Today this technology is pervasive as exemplified by many activities around the world and in many areas of research namely, mixed signal design, signal and power integrity, EMI, fabrication, integration and test of mixed digital , RF and optical functions as well as assembly, manufacturing, and reliability. The SOP paradigm is expected to change the current chip-centric system-on-chip (SOC) methodology to cheaper, faster-to-market IC-package-system co-design flow. The SOP concept (Figure 1) also has brought together universities and industries on common platform with the PRC, in research, education and long-term projects.

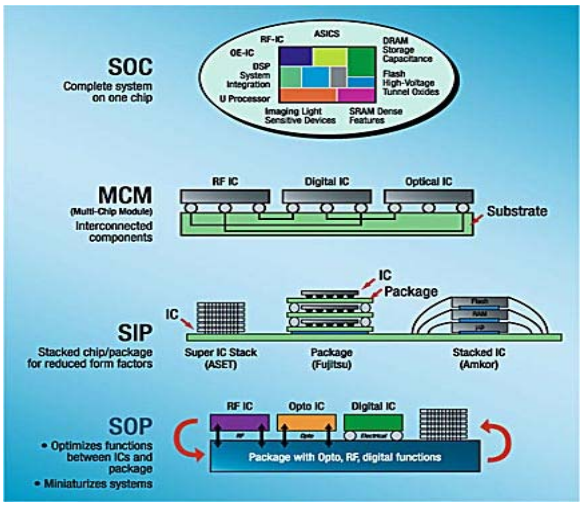

Fig 1: SOP as compared to SOC, SIP and MCM

Electronics Scenario in India

During the year 2003-04, electronics and IT industry in India showed a phenomenal growth of 19 percent [2]. Although software and services industry in India continues to be the leading sector and shows a robust growth, hardware services are now into strategic areas including satellite based communication, infra-red based detection and ranging, GPS based vehicle tracking systems etc.. Microelectronics forms the core of hardware constituent of the IT, internet and communications revolution. The thrust of microelectronics and nano-technology development program initiatives is to build a strong microelectronics industry and R & D base in the country to cater to the needs of the human resource development, research base, entrepreneurship and healthy growth of the industry. This focus has led to major efforts on the part of the universities in the country to tune the academic program suited to meet the requirements of the thrust areas in science and technology. The presence of multinational companies and the establishment of R & D centers by these industries in India is an important step for the development of electronics manufacturing and services in India.

Indian Institute of Science (IISc) and the presence of Packaging Education in India

The Indian Institute of Science was started in 1909 and since then has grown into a premier institution of research and advanced instruction, with more than 1500 active researchers working in almost all frontier areas of science and technology. IISc is an institute of higher learning and is constantly in pursuit of excellence. It is one of the oldest and finest centers of its kind in India and has a very high international standing in the academic world as well.

The Centre for Electronics Design and Technology was established in 1974 at the Indian Institute of Science, Bangalore, with the joint support of the Department of Electronics (DoE), Ministry of Education, University Grants Commission and Swiss Agency for Development and Co-operation under the Technical and Scientific Co-operation Agreement, New Delhi of 1966 between Governments of India and Switzerland. CEDT is now a full Department in the division of Electrical Sciences of the Indian Institute of Science.

CEDT started its postgraduate Diploma program in Electronics Design and Technology in 1975. Initially this program was made available exclusively to engineers sponsored by industries and R&D Institutions. In 1984, the program was opened to non-sponsored students. The postgraduate Diploma Program was replaced by an M. Tech. (Masters in Technology) in Electronic Design and Technology in 1987. Research programs leading to M.Sc (Engg) and Ph.D. were introduced in 1992. External registration for research program was introduced in 1995. M.E (Masters in Electronics) in Microelectronics was introduced in 1997 as a joint program between CEDT and Electrical Communication Engineering department.

Based on the experience gained at this Centre, the Ministry of Information Technology, Government of India, has set up seven more CEDTs elsewhere in the country. In addition, an Electronics Design Laboratory was established in Bangkok on the pattern of CEDT, as an Indo-Thai venture. The Centre is participating in various activities associated with these new Centers.

The M.Tech program in CEDT (Figure 2) is design-oriented with nearly two thirds of the 24 months spent by students on learning by practical work. M.Tech project is an extremely important component of the program. One third of the credits for the M.Tech program are assigned for the project. The annual intake of students in this special program is around 30 students with up to 30% sponsored candidates from industry. Additional candidates from the Quality Improvement Program from Universities in India (QIP) are also admitted. Students complete their project work (whose time period is almost one year from planning to prototype demo) in any of the electronics disciplines from the following:

- Telematics
- Electromechanics
- Instrumentation and
- Power Electronics.

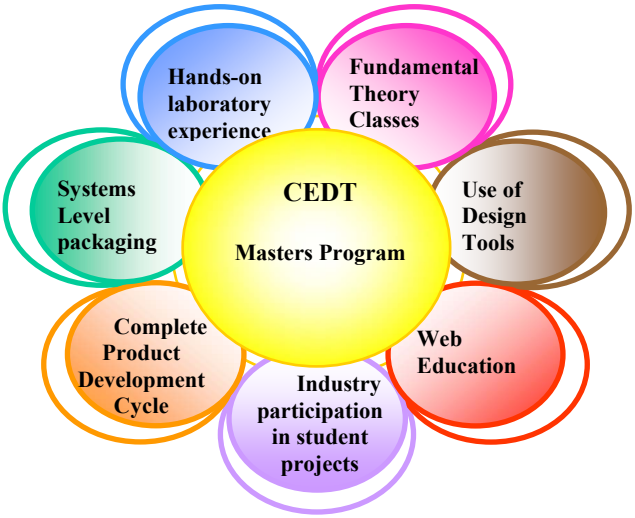

Fig 2: Post-graduate packaging education model in IISc

Industrial Design and Electronics Packaging are core courses in the curriculum of CEDT and are an integral part of every student project work in the Center. Almost all of the student projects are sponsored by multinational companies and other electronics industries in India and this is similar to the internship done by students in US, resulting in a majority of the industries absorbing the students for full-time employment after their completion of the Masters Program.

Fig 3: Clean Room and Lab facilities at IISc for electronics systems packaging education and research

CEDT has well equipped facilities. Following are some of the facilities:

- Electronic Design Automation (EDA) tools on workstations.
- Well equipped power-electronics, instrumentation, Electromechanics, Telematics laboratories
- Product design studio
- Mechanical Workshop
- PWB design and fabrication facilities.(Figure 3)
- CAD facilities for PCB and mechanical drawings

- EMC facilities with an EMI receiver and Faraday cage.
- Embedded systems lab
- TI DSP Centre
- Intel Multimedia and IXA Processor Lab
- Motorola Digital DNA Lab
- Surface Mount Assembly and Training Lab
- High speed computing facility

The M.Tech flagship program in CEDT comprises of the following set of core and elective courses which the students are required to formally complete in addition to project work.

Core Courses

- Analogue and data conversion systems
- Design of digital systems
- Designing with power devices
- Electromagnetic compatibility
- Electronic Systems Packaging
- Mechanical Packaging of electronics equipment
- Industrial design of electronic equipment
- Basics of VLSI
- FPGAs and PLDs

Electives Courses

- Control system design
- Data communication systems
- Design of photovoltaic systems
- Design of power converters and drives
- Embedded Systems
- Incremental motion control
- Industrial instrumentation
- Mechatronics
- Microcomputer applications
- Microprocessor system design
- Software for industrial microcomputer systems
- TCP/IP Networking
- Low power VLSI Design

Apart from the established Masters Program, CEDT also offers short-courses in the fields of electronics packaging, VLSI, Embedded Systems, Microprocessors & microcontrollers and Industrial Design periodically for the Indian industry. These are typically two-week courses run twice a year with full hands-on component.

Curriculum and Lab Facilities for Electronics Systems Packaging Course

The Electronics Systems Packaging Group at CEDT has the unique feature of having modeled a structured academic course in electronics packaging in tune with the current requirements similar to the one at the Packaging Research Center at PRC who are pioneers in this growing field. This has been made possible through a Memorandum of Understanding (MoU) signed between IISc and PRC during 1998-1999 which enabled faculty exchange visits and research interaction. CEDT is probably the only institution in India where considerable hands-on experience is given to post-graduate students in electronics packaging, which includes CAD, manufacturing and assembly, reliability and test.

The students who finish the systems-level electronics packaging course in CEDT gain the following skills:

1. Fundamental and system-level electronics knowledge
2. Hands-on skills for the complete product development in industry from electrical and mechanical design, materials, processes, structures, packages, electrical testing, thermal management, assembly and reliability.
3. Industry perspective.
4. Communication skills through seminars

The following is the syllabus for the course, which has extensive practical content including CAD.

- Electronics systems and needs
- Physical integration of circuits, packages, boards and electronic systems
- System applications like computer, automobile, medical and consumer electronics with case studies
- Packaging levels; electrical design considerations -power distribution, signal integrity and parasitics, EMI/EMC and wireability issues
- Computer aided design (CAD) for Printed Wiring Boards (PWB)
- PWB Technologies; MCMs, flexible and 3-D PWBs
- Recent trends in manufacturing like microvias and sequential build-up circuits
- Substrates and their importance in deciding electrical properties of board-level packages
- Fundamentals of Materials and Processes
- Assembly choices- flip chip, TAB and wirebond; surface mount assembly, hybrid assembly; other chip connection methods
- Joining methods in electronics- solders and their alternates
- Electrical test and reliability
- Thermal management of PWBs and methods
- Mini Project on a functional prototype with focus on board assembly and testing
- Student Seminar on advanced research paper
- Practical lab exercises on PWB CAD and manufacturing

The laboratory facilities available to the students who register for the electronics packaging course are the following:

- Class 1000 clean room for imaging and inspection of finished boards
- Yellow room for photo imaging of circuits onto PCB substrates. Equipments used here are a dry film laminator, UV exposure unit, and suitable developers; manual screen printing machine for solder mask application and legend printing purposes.

- A chemical lab consisting of all the major equipments required for plated-through hole (PTH) processing:
    - PTH line with DI water rinsing and custom made design for power supply
    - conveyorized etching machine
    - conveyorized deburring and brushing machine
    - conveyorized developing machine
    - deionized water supply for all the units
    - analytical equipments for cross-section, chemical analysis and plating thickness measurement
- Stereo zoom microscopes; USB microscope for inspection
- SMD lab with pick & place, reflow and inspection units
- CNC drilling machine

Every year a working prototype product is chosen for case study to highlight the electronics packaging and industrial design aspects of the product and the students are then asked to improvise on that design and come up with better solutions in the form of a seminar presentation. This has proved to be a successful methodology to highlight packaging emphasis as is evident from the feedback obtained from the students. The lab sessions include evolving designs with certain specifications and applications, board fabrication to understand the concept of microvia and multilayer build-up, surface mount assembly and board repair methods.

Some of the salient features and objectives of the hands-on packaging course are the following: (Figure 4)

- Electrical design of circuits, medium complexity to suit single-layer, double-layer and multilayer PWBs
- Understanding the need for electrical issues like cross-talk, impedance, capacitances and their modeling
- Understanding the influence of different types of substrates on the electrical issues
- Package forms- through-hole, Surface Mount Technology and Chip-on-board types and their design rules
- Board level process steps and feature sizes up to 4-5 mil lines and spaces; microvia build-up methods and electrochemical processes
- Understanding material and process characterization
- Measurement of capacitances in test board
- Component assembly and test especially surface mount components
- Reflow soldering procedures
- Overview of thermal cycling and reliability
- Appreciation of environmental effects in electronics packaging industry
- Simple experiments to demonstrate thermal cooling procedures on test boards

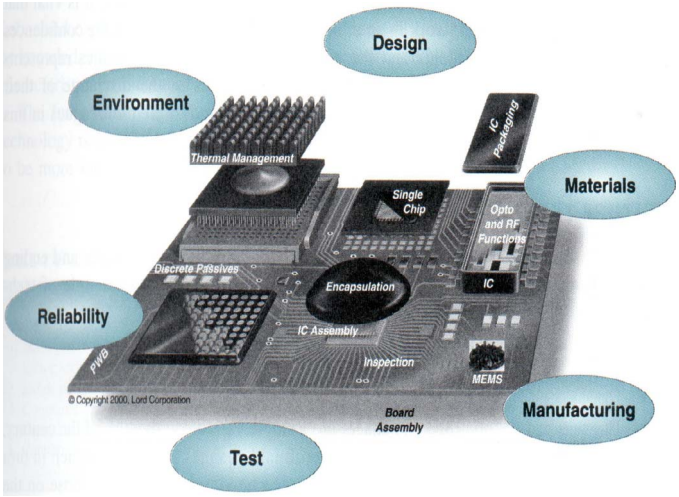

Fig 4: Major areas covered in the board level electronics systems packaging course in IISc

This program is similar to the Design-Build-Operate (DBO) courses in Georgia Tech [3, 4]. IISc faculty with their previous experiences in hands-on experience in designing hands-on courses, were involved in this set-up process along with the Georgia Tech faculty members. The first DBO course was offered in Fall 1999 for the substrate fabrication and the second DBO was offered in Jan 2000 for PWB Assembly and reliability test. This international collaboration stood out as an excellent example of global outreach of PRC and faculty exchanges between the two universities.

Packaging Research in IISc

In an effort to integrate research into education continuously, CEDT has been active in research in the areas of board level fabrication and assembly. One of the more recent projects funded is a project from the Ministry of Information Technology (MIT), Government of India, for a microvia research project that utilizes Sequential Build Up technology (SBU) for medium-dense boards. The project worth USD 300,000 over a 2-year period has enabled CEDT to have a class 1000 clean room and install advanced imaging, wet-processing and analytical equipment in its laboratory. The project is primarily focused on photo-via process to create microvias and build 4-6 layer PWBs for digital applications.

Multimedia Education Modules developed by CEDT

The Packaging Research Center (PRC) embarked on national and international electronic packaging programs involving professional organizations, other universities, and the microsystems packaging industry. In long-distance education, the joint effort between the PRC and Components, Packaging and Manufacturing Technology (CPMT) Society of the IEEE led for the first time to the start of educational sessions at the International IEEE Electronic Components and Technology Conference (ECTC) [5, 6]. The primary goal of this activity is to achieve one or more of the following items:

- Innovative curriculum developments to address the needs of packaging students and working professionals.
- Implementations of shared or multimedia courses, modules, simulations, virtual labs.

The Indian Institute of Science was awarded a fellowship to develop a set of educational modules and the objectives of developing these modules are for the trainee or the student to understand substrate and assembly technology, electrical, thermal and reliability issues of high density and high-frequency PCBs and acquire the ability to design such boards using standard commercially available CAD tools. The modules have extensive illustrations in the form of slides and serve as an advantage for classroom study. These presentations are hosted at the following website and are due for review from time to time for upgrades:

http://www.prc.gatech.edu/academics/elpkg/index.htm

These represent about 42 hours of lectures which is almost equivalent to one semester-long course in packaging. The topics chosen are specialized and they are the following:

1. Overview of electronics packaging
2. Semiconductor packaging
3. PWB Design Process
4. Electrical aspects of PWBs
5. Manufacturing processes
6. Joining methods in electronics
7. Surface Mount Technology and Processes
8. Quality Management in PWB manufacture

CEDAP

In the year 2004, PRC set a goal for forming an International Center in India called CEDAP (Center for Electronics Design and Advanced Prototypes) involving Georgia Institute of Technology, Indian Institute of Science and the Indian Electronic Industry at Bangalore, India. It is intended to be physically located in the campus of IISc during the year 2005.

The goal of such a Center is to develop short to long term collaborations between the above entities to serve India's needs in the emerging hardware design, modeling and advanced packaging technologies including prototype fabrication leading to India becoming a global player in the hardware development.

The initial goals suggested are Consulting Services to help educate the Indian Electronic Industry, Educational programs in Fundamentals of Packaging, Design and Electrical issues, Mechanical and thermal modeling, Packaging Technologies-IC Packaging, Systems Packaging, Test, Assembly, Thermal Management and Reliability and finally research collaborations. CEDAP will also work together with IEEE-CPMT Chapters of India to conduct workshops, seminars and periodic conferences in electronics packaging in India.

Conclusion

One of the primary objectives of engineering institutions worldwide is to produce students who can be gainfully employed by industry. For this to happen in today's competitive industrial environment, it is imperative that graduates are not only equipped with the latest theoretical knowledge in the field, but also with hands-on work experience. Due to the multi-disciplinary nature of electronics systems packaging, the packaging education curricula offers significant challenges that have not been generally faced by academicians dealing with curricula in the classical disciplines in engineering. A successful curriculum in electronic packaging has to draw upon the subject matter in the disciplines of mechanical, electrical, chemical, and materials engineering.

Towards this end, the international collaboration in electronics packaging education between IISc and PRC, Georgia Tech has been greatly beneficial to the improvement of the packaging education in IISc in terms of human resource development, manpower training for industries and advanced research. The involvement of industries into this outreach will be an added advantage. Students and industries now consider PRC as a benchmark for gaining experience and training in their specialized fields within the realm of SOP.

Acknowledgments

The IEEE-CPMT Faculty Fellowship awarded to IISc is also gratefully acknowledged by the faculty members of CEDT, IISc.

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