Influence of Placement of Small Space Vectors on the Performance of PWM Techniques for Three Level Inverters

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Abstract—The performance of three level inverters depends **on** the **PWM** technique. The three level space vector **PWM (SVPWM)** has improved performance in terms of the THD and the D.C. bus mid point voltage balance compared to three level sine triangle **PWM (SPWM).** The objective **of** this paper is to study the importance of the space vectors, the influence of their placement in the switching sequence **on** the performance of the **PWM** techniques and address the basic issue **of** why the **SVPWM** has superior performance over **SPWM** technique. Such a basic understanding will help in designing optimal **PWM** with desired performance. The study has shown that the superior performance of **SVPWM** is because of the placement **of** the small space vectors as the beginning and ending vectors in each sequence, with equal dwell times. The simulation results are presented to validate the theoretical observations. The **SVPWM** is implemented **on** a general purpose **DSP** based digital controller and applied to constant *v/f* drive.

Index Terms— Three Level Inverters, Diode Clamp Three Level inverters, Space Vector **PWM (SVPWM),** Sine Triangle **PWM (SPWM).**

I. INTRODUCTION

The circuit diagram of the three-level diode clamp VSI is shown in fig 1. Each pole can he connected to positive D.C. bus (state I) or D.C. bus mid point (state 0) or negative D.C. bus (state −1). Fig. 2 shows the space vectors of the three-level inverter on $a-\beta$ plane. There are $2^3 = 21$ inverter states, which can be used to produce 19 space vectors. The space vectors $\bar{V}7, \bar{V}9, \bar{V}11, \bar{V}13, \bar{V}15$ and $\bar{V}17$ with magnitude V_{dc}, form the set of six large space vectors. Similarly the set of six medium space vectors consists $\bar{V}8, \bar{V}10, \bar{V}12, \bar{V}14, \bar{V}16$ and $\bar{V}18$ with magnitude $0.866V_{dc}$. Each of the medium and large vectors can be generated by only one inverter state a!; defined in fig. 2. There are six small vectors, $\bar{V}1$ to $\bar{V}6$, with magnitude $0.5V_{dc}$. Each of these small vectors can he generated by two inverter states as defined in fig. 2 and table I. The zero space vector, $\bar{V}0$, can be generated by three inverter states namely (0 0 0) or (1 1 I) **or** (-1 -1 -1).

Several types of PWM techniques have been developed for three-level diode clamp inverters [2-16]. These modulation techniques can be grouped into two categories: sine triangle PWM (SPWM) and space vector PWM (SVPWM). In the case of three level diode clamp voltage source inverters the performance of the PWM techniques are characterized by the output current ripple, *THD*, D.C. bus mid point 'voltage imbalance and common mode voltage variation. A large variation of D.C. bus mid point voltage will disturb the half wave symmetry and will give rise to even harmonics. The

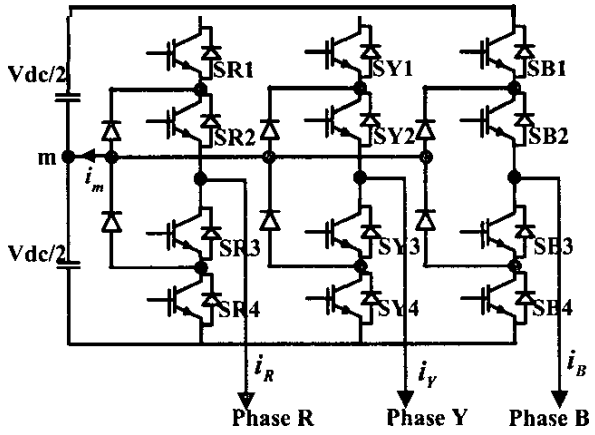


Fig. 1 Circuit digram of three level diode clamp inverter

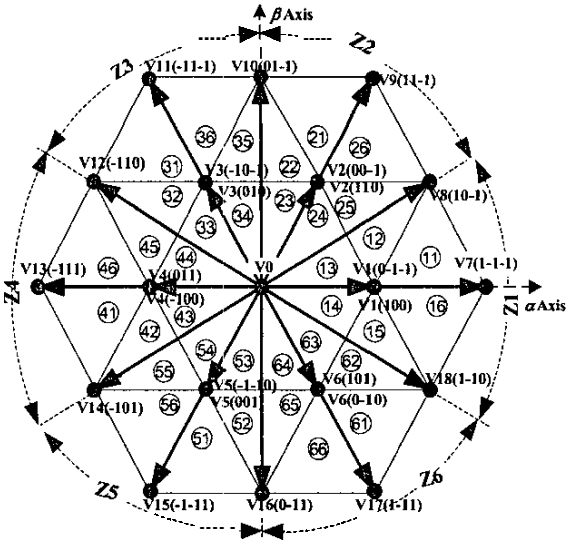


Fig. 2 Space vectors of three level diode clamp inverter

presence of even harmonics will not only affect the *THD* hut also affects the performance of the drive [13]. Even though several **PWM** schemes are developed to address some of the specific problems like improving the *THD* [2-9], reducing the D.C. bus imbalance [10-14], minimizing the common mode voltage [15-17], there is still need to develop an optimal **PWM** algorithm that can result in desired overall performance. The objective of this paper is to study the switching space vectors of the **SVPWM** and **SPWM** techniques and establish a basic relation between the switching vectors and the performance of the **PWM** techniques. Such a basic understanding will help in designing the optimal **PWM** algorithms with desired performance.

Based on the above study it is shown that it is the proper choice of small space vectors and their placement at the beginning and end of the switching sequences with equal dwell time, which results in low voltage ripple and hence low *THD*. **SVPWM** techniques employ this type of sequence; hence their performance is superior compared to other **PWM** techniques in terms of *THD*. It is also illustrated that such an arrangement will result in reduced D.C. bus mid point voltage imbalance and reduced common mode voltage variation. Thus the **SVPWM** sequence has superior overall performance compared to other **PWM** techniques in the linear range of the modulation. Another contribution of this paper is that the region in which the given small vector has improved performance is established; thereby removing the ambiguity in the choice of small vectors.

The principles of **SVPWM** and **SPWM** are reviewed in section II. In section III, the influence of the placement of space vectors on voltage ripple and flux ripple is established, The mean square value of the flux ripple of **SVPWM** is computed and plotted for the entire linear range of the modulation. The **SVPWM** and **SPWM** algorithms are simulated and the *WTHD* of the line voltages are presented. The **SVPWM** algorithm is applied to an experimental three level diode clamp VSI based constant *v/f* drive. The experimental results are given in section **IV.**

II. REVIEW OF THREE LEVEL PWM TECHNIQUES

A. SVPWM for Three level Inverters:

In space vector approach to **PWM** the reference vector $\bar{V}_r$ is sampled at regular intervals T_S . The sampled reference vector is approximated by time averaging the nearest three vectors $\bar{V}_x$,$\bar{V}_y$ and $\bar{V}_z$ according to (1)

$$\bar{V}_r T_S = \bar{V}_x T_x + \bar{V}_y T_y + \bar{V}_z T_z, \qquad (1)$$

where, T_x, T_y and T_z are the intervals of $\bar{V}_x, \bar{V}_y$ and $\bar{V}_z$ respectively and $T_S = T_x + T_y + T_z$.

In (1), for $m > 0.433$, where m is the modulation index, defined as the ration between the magnitude of $\bar{V}_r$ to the V_{dc},

TABLE I
SMALL VECTORS, THEIR STATES AND D.C. BUS MID POINT CURRENT

Sector Z	Small vector $\bar{V}_z$	Small vectors and mid point current			
		$\bar{V}_{zx}$	$i_{mzx}(t)$	$\bar{V}_{zy}$	$i_{mzy}(t)$
1	$\bar{V}_1$	100	i_R	0-1-1	$-i_R$
2	$\bar{V}_2$	110	$-i_B$	00-1	i_B
3	$\bar{V}_3$	010	i_Y	-10-1	$-i_Y$
4	$\bar{V}_4$	011	$-i_R$	-100	i_R
5	$\bar{V}_5$	001	i_B	-1-10	$-i_B$
6	$\bar{V}_6$	100	$-i_Y$	0-10	i_Y

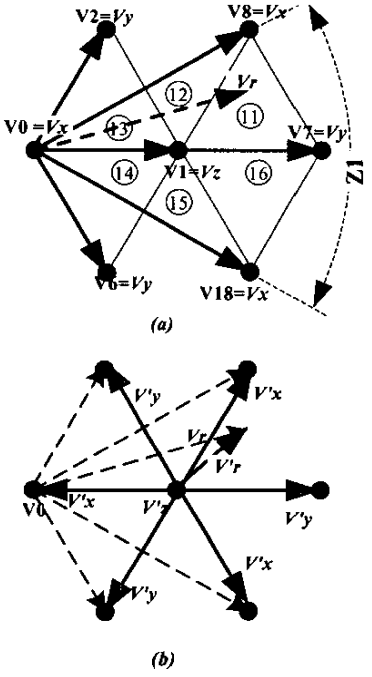


Fig.3.(a) Space vectors associated with sector 1.
(b) Mapping of the vectors of sector 1 to fictitious vectors.

all the nearest three vectors are non zero vectors and there is no common vector in all the regions of the space phasor. The solution of (1), can he simplified by exploring the symmetry in the space vector plane. The entire space vector plane is divided in to six symmetrical sectors, each of sixty degrees interval as shown in fig.2. Each sector Z, where $Z = 1,2,...6$, is associated with one small vector $\bar{V}_z$ at the center and six other vectors at the vertices of the hexagon. These small vectors are defined in table I. The small vector $\bar{V}_1$ and other six vectors of sector 1 are redrawn in fig.3 (a). The vectors of the other sectors are phase displaced by $(Z-1)\pi/3$ radians. All the vectors of a given sector can be mapped to seven fictitious vectors, with small vector as the origin according to (2).

$$\vec{V}_r' = \vec{V}_r e^{j(Z-1)\pi/3} - \vec{V}_1$$
$$\vec{V}_x' = \vec{V}_x e^{j(Z-1)\pi/3} - \vec{V}_1$$
$$\vec{V}_y' = \vec{V}_y e^{j(Z-1)\pi/3} - \vec{V}_1 \text{ and} \quad (2).$$
$$\vec{V}_z' = \vec{V}_z e^{j(Z-1)\pi/3} - \vec{V}_1 = 0$$

The mapping of the all the seven vectors of sector in to seven fictitious vectors is illustrated in fig. 3(b). The magnitude of $\vec{V}_z'$ is always zero and (1) will have only two unknowns as in (3).

$$\vec{V}_r' T_s = \vec{V}_x' T_x + \vec{V}_y' T_y \quad \text{and} \quad T_z = T_s - T_x - T_y \qquad (3)$$

The T_x, T_y and T_z are computed using (3).

The samples will have sequences $\vec{V}_{zx} \rightarrow \vec{V}_x \rightarrow \vec{V}_y \rightarrow \vec{V}_{zy}$ and $\vec{V}_{zx} \leftarrow \vec{V}_x \leftarrow \vec{V}_y \leftarrow \vec{V}_{zy}$ alternatively, with the dwell times T_{zx}, T_x, T_y and T_{zy} respectively, where $T_{zx} = T_{zy} = T_z/2$. Unlike two level inverters, the $\vec{V}_z$ vector will change from sector to sector. So there will be one additional switching during sector change over. These SVPWM sequences will guaranty that only one switch will switch during state transition.

B. *SPWM for* ***Three level Inverters:***

There are different types of SPWM algorithms. The most popular type of SPWM employs two carrier signals. The carrier signals may be in phase or out of phase [3]. The SPWM employing two carrier signals, which are in phase is shown in fig. **4.** The switching sequences are similar to that of SVPWM but the dwell time T_z of the small vectors is unequally divided between $\vec{V}_{zx}$ and $\vec{V}_{zy}$ space vectors such that $T_{zx} + T_{zy} = T_z$ [5-7]. The sequences guaranty that only one switch will change status during state transition.

III. SIGNIFICANCE OF PLACEMENT OF SMALL VECTORS ON THE PERFORMANCE OF PWM TECHNIQUES

A. *Effect of* ***Placement of Small Vector on*** *THD*

The difference between the inverter output voltage in the j^{th} state of the switching sequence ($\vec{V}_j$) and the reference voltage ($\vec{V}_r$) will result in voltage ripple as defined in **(4).**

$$\Delta\vec{V} = \vec{V}_j - \vec{V}_r \qquad (4)$$

The voltage ripple causes the **flux** ripple in the machine: which is responsible for the current ripple and harmonics.

The magnitude of the **flux** ripple $\Delta\psi$, can be easily computed by resolving the voltage ripple in to alpha and beta components as in **(5).**

$$\Delta\psi_\alpha = \int \Delta V_\alpha \, dt = \int (V_{j\alpha} - V_{r\alpha}) \, dt \quad \text{and}$$
$$\Delta\psi_\beta = \int \Delta V_\beta \, dt = = \int (V_{j\beta} - V_{r\beta}) \, dt \qquad (5)$$

The mean square value of the **flux** ripple over a sector, defined in (6) can be taken as **a** measure of *THD* to study the

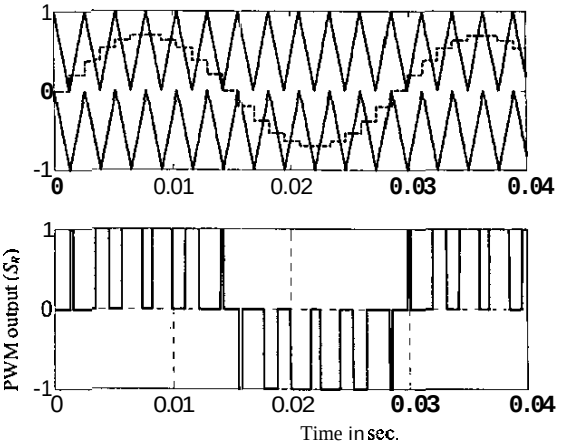


Fig. **4.** SPWM: **Carrier** and modulating signals and PWM output

performance of the PWM techniques [2,3]

$$\Delta\psi^2 = \frac{6}{N}\sum_{k=1}^{N} \Delta\psi_k^2 \ , \qquad (6)$$

where N is the number of samples per sector and $\Delta\psi_k^2$ is the square of the magnitude of the **flux** ripple of the k^{th} sampling interval computed over one sampling interval (T_s), using $\Delta\psi_k^2 = \Delta\psi_{k\alpha}^2 + \Delta\psi_{k\beta}^2$. The aandpcomponents of the $\Delta\psi_k^2$ over one sampling interval are computed as follows.

$$\Delta\psi_{k\alpha}^2 = \frac{1}{T_s}\left[\int_0^{Tzx} (V_{zx\alpha} - V_{r\alpha})^2 \, dt + \int_{Tzx}^{Tzx+Tx} (V_{x\alpha} - V_{r\alpha})^2 \, dt + \right.$$
$$\left. + \int_{Tzx+Tx}^{Tzx+Tx+Ty} (V_{y\alpha} - V_{r\alpha})^2 \, dt + \int_{Tzx+Tx+Ty}^{Ts} (V_{zy\alpha} - V_{r\alpha})^2 \, dt \right]$$

$$\Delta\psi_{k\beta}^2 = \frac{1}{T_s}\left[\int_0^{Tzx} (V_{zx\beta} - V_{r\beta})^2 \, dt + \int_{Tzx}^{Tzx+Tx} (V_{x\beta} - V_{r\beta})^2 \, dt + \right.$$
$$\left. + \int_{Tzx+Tx}^{Tzx+Tx+Ty} (V_{y\beta} - V_{r\beta})^2 \, dt + \int_{Tzx+Tx+Ty}^{Ts} (V_{zy\beta} - V_{r\beta})^2 \, dt \right]$$

Fig. **5** and 6 show the variation of alpha and beta components of the voltage ripple and **flux** ripple over one sampling interval (with Ts=1.7 millisecond., m=0.4, k=4 and N=5) for three different combinations of placement of small vectors.

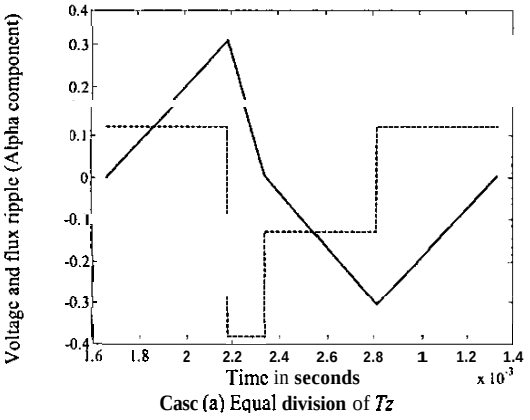
Case (a) CSVPWM sequences: The dwell time T_z is equally divided between $\vec{V}_{zx}$ and $\vec{V}_{zy}$ (Fig. 5a and 6a).

Case (b) SPWM: The dwell time T_z is unequally divided between $\vec{V}_{zx}$ and $\vec{V}_{zy}$ such that $T_{zx} \neq T_{zy}$ (Fig. 5b and 6b).

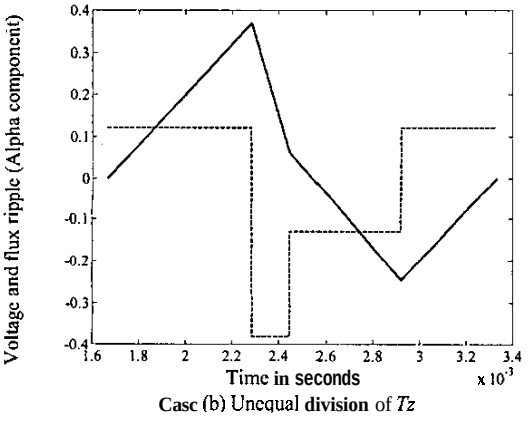
Case (c) Clamping or discontinuous PWM sequences: No division of the dwell time T_z. The small vector is placed either at the beginning or at the end (Fig. 5c and 6c).

The **flux** ripple and the mean square value of the **flux** ripple are low for case (a) and are high for case (c). Their values are in between for case (b). From the above analysis following observations can be drawn.

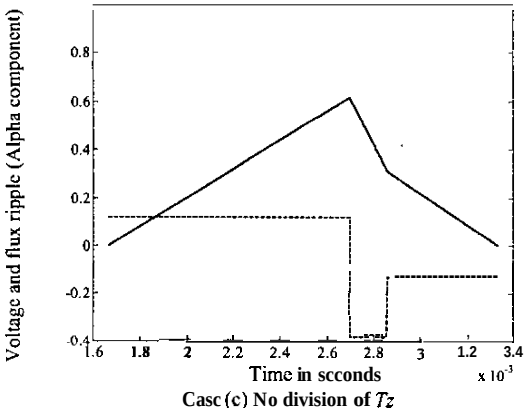
- The voltage ripple, hence the **flux** ripple is a function of the dwell time of the space vectors and their placement in the switching sequence. **If** the space vector is close to the reference vector the dwell time of the space vector will be high and the voltage ripple will be low.
- For the sector definition of fig. 2, for a given sector, the small vector associated with the sector will be the nearest space vector for **all** the samples in the region $0.25 \le m \le 0.75$. Hence for $0.25 \le m \le 0.75$, T_z is greater than T_x **and** T_y . In SVPWM T_z is equally split into two halves between $\bar{V}_{zx}$ and $\bar{V}_{zy}$, whereas in the case of SPWM the splitting of T_z is



Casc (a) Equal division of Tz

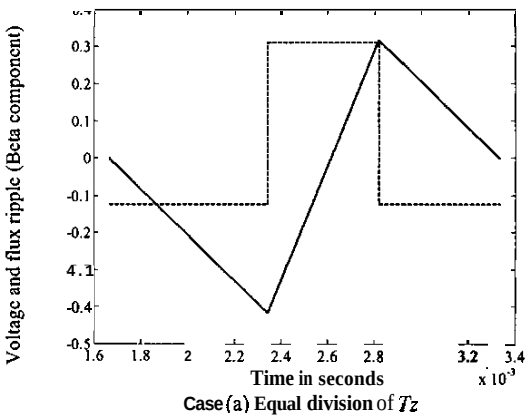


Casc (b) Unequal division of Tz

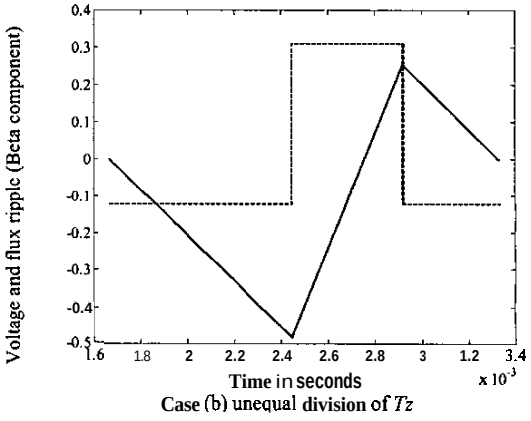


Casc (c) No division of Tz

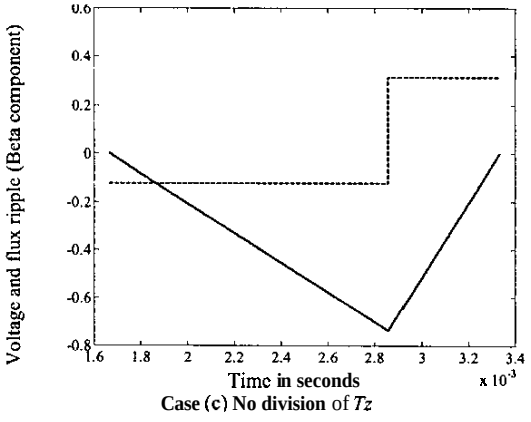
Fig. 5. The Variation of alpha component of voltage ripple (— — —) and flux ripple (———) over one smapling interval. (*Ts=1.7 msec, m=0.4,k=4 and N=5*) (a) Equal Division of Tz interval (b) Unequal division of Tz intcrval Tzx>Tzy (c) No division of Tz interval (The flux ripple is magnified by a factor of 5000)



Case (a) Equal division of Tz



Case (b) unequal division of Tz



Case (c) No division of Tz

Fig. 6. The Variation of beta component of voltage ripple (— — —) and flux ripple (———) over one smapling interval. (*Ts=1.7 msec, m=0.4,k=4 and N=5*) (a) Equal Division of Tz interval (b) Unequal division of Tz interval Tzx>Tzy (c) No division of Tz interval (The flux ripple is magnified by a factor of 5000)

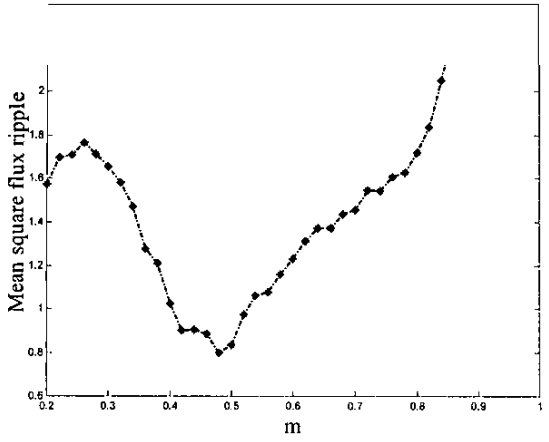


Fig. 7. Mean square flux ripple v/s m

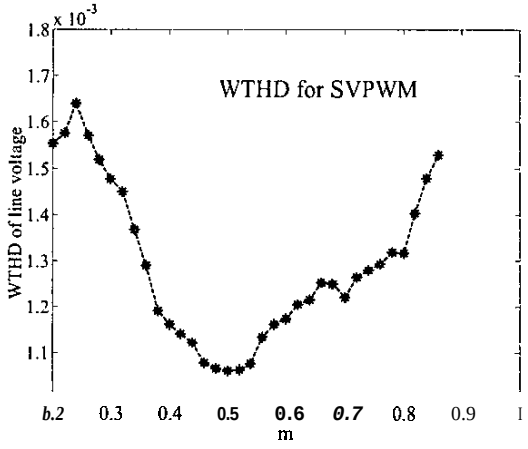


Fig.8. *WTHD* v/s m **for SVPWM**

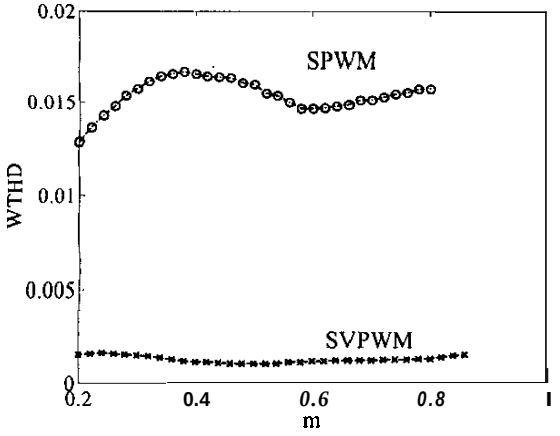


Fig. 9 WTHD v/s m **for** SVPWM and **SPWM**

unequal. This is the reason why the *THD* is high in the case of SPWM compared to SVPWM.

- As m is increased beyond 0.75, the T_x or T_y will be larger than T_z. Hence there is little or no influence of splitting the dwell time of small vectors. So the voltage ripple, the flux ripple and the *THD* will increase at higher values of ***m*** especially at over modulation region. **Also** for a given switching frequency, the sampling frequency of clamping sequences will be 1.5 times higher than that of conventional PWM schemes. This is the reason why in over modulation region, for a given switching frequency (*fsw*), the *THD* of clamping sequences will be comparable or better, compared to that of conventional PWM algorithms.

In the case of SVPWM, the mean value of the square of the flux is computed from the simulation results for the linear range of ***m***. For *fsw*=2.5KHz, the variation of mean square value of the flux ripple in the linear range of ***m*** is plotted in fig.7. As expected the mean square value of the flux ripple is low at and around $m=0.5$ and rises as one moves away from $m=0.5$ in both the directions. This is in agreement with the theoretical observations given above. The SVPWM and SPWM algorithms are simulated using MATLAB-SIMULINK toolbox. The *WTHD* of the line voltage is computed from the simulation results. *WTHD* is proportional to the *THD* of the motor no load current and can be taken as a measure of performance [8]. The variation of *WTHD* in the linear range of ***m*** **is** shown in Fig. 8. From fig.7 and X, It can be seen that *WTHD* varies similar to the mean square value of flux ripple and **is** low at and around m=0.5 and increases as ***m*** **is** either increased or decreased. So the mean square value of flux can also be taken as the index of the *THD*, similar to *WTHD*. Comparative results of *WTHD* of SPWM and SVPWM are shown in fig.9, and the SVPWM has improved *WTHD* compared to that of SPWM.

B. Effect of Placement of Small Vector on D.C. Bus Mid Point Voltage

In three level diode clamp inverters, the D.C. bus capacitors carry the load current. The unequal loading of the upper and lower capacitors causes the mid point voltage to fluctuate. The D.C. bus rnid point voltage variation (ΔV_m) can be estimated from the D.C. mid point bus current (i_m) using (7).

$$\Delta V_m = \frac{1}{C}\int_o^{Ts} i_m(t)dt = \frac{1}{C}\left[\int_0^{Tzx} i_{mzx}(t)dt + \frac{1}{C}\int_{Tzx}^{(Tzx+Tx)} i_{mx}(t)dt + \int_{(Tzx+Tx)}^{(Tzx+Tx+Ty)} i_{my}(t)dt + \int_{(Tzx+Tx+Ty)}^{Ts} i_{mzy}(t)dt\right] \quad (7)$$

The small vectors can be used to reduce ΔV_m and this property is extensively used to design SVPWM techniques to minimize the D.C. bus imbalance [10 –14]. The i_m due to the two small vectors will be equal and opposite that is $i_{mzx}(t) = -i_{mzy}(t)$ as given in table I. In the case of SVPWM switching sequences, the dwell time of $\bar{V}_{zx}$ and $\bar{V}_{zy}$ states will be equal. The ΔV_m due to these states is perfectly cancelled in each sampling interval, so they do not contribute for the D.C. bus capacitor voltage imbalance. In SPWM, the

dwell time of $\bar{V}_{zx}$ and $\bar{V}_{zy}$ will he different, so the ΔV_m due to these states will be non-zero and there will be D.C. bus imbalance. in the case of clamping sequences, only one of the states of $\bar{V}_z$ is used, so there will be large imbalance in D.C. bus mid point voltage due to small vectors. Thus, the placement of small vectors at the beginning and end state with equal dwell time helps in reducing the D.C. bus imbalance. As far as $\bar{V}_x$ and $\bar{V}_y$ states are concerned, if these states fall in the set of medium or small vectors, then they contribute for the D.C. bus imbalance. The mid point current due to zero and large vectors will be zero, so they do not contribute for the D.C. bus imbalance. Under balanced three phase conditions, as in drives, the D.C. bus balance can be achieved over a cycle of the fundamental if the PWM sequences have half wave symmetry. If these sequences have three-phase symmetry also, then the D.C. bus can be balanced over every 1/3rd period of the fundamental cycle. Compared to SPWM, SVPWM approach gives better flexibility in getting three phase and half wave symmetry, one such SVPWM is given in [8]. These sequences are generally employed for low switching frequency applications.

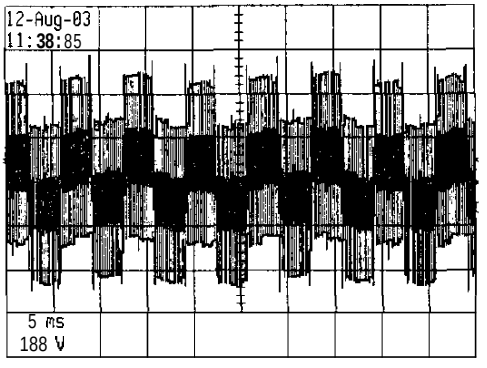


Fig 10 Experimental waveform of v_{nm} for SVPWM with Fs=50Hz, V_{dc}=570V and fsw=2.5KHz.

C. *Effect* of *Placement* of *Small Vector on Common Mode Voltage*

The common mode voltage variation, v_{ng} is given by $v_{ng} = v_{nm} + v_{mg}$, where n,m and g are the motor stator neutral, D.C. bus mid point and system ground points respectively. So the common mode voltage depends on the voltage v_{nm}, which is a function of space vector as defined by $V_{nm} = \frac{V_{dc}}{6}(S_R + S_Y + S_B)$, where (S_R, S_Y, S_B) is the inverter state. The zero space vectors VO (111) and VO (-1-1-1) will have highest value of $V_{nm} = V_{dc}/2$. The sequences which use small vectors at the beginning state and ending state in the switching sequence of the sampling interval, will always ensure that, only one of the switches are switched during state transition and for $m<0.433$ only $\bar{V}_0$ (000) vector is used. Thus the zero vectors $\bar{V}_0$ (111) and $\bar{V}_0$ (-1-1-1) are avoided. The SVPWM and SPWM, both satisfy these conditions. But the clamping sequences will result in higher common mode voltages as the clamping sequences use these zero states [9]. The experimental waveform of V_{nm} for SVPWM is given in fig 10. It should be noted that the change in common mode voltage is limited to $(1/6)V_{dc}$ and peak is limited to $(1/3)V_{dc}$.

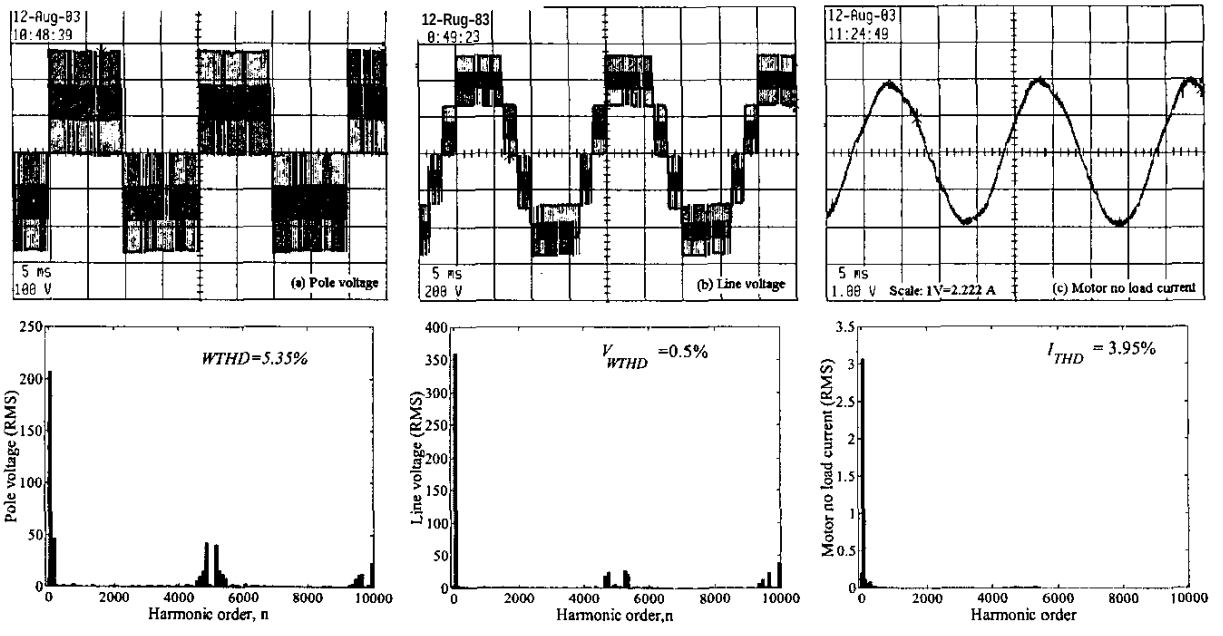


Fig. 11. Experimental results of SVPWM (Fs=50Hz, V_{dc}=570V, fsw=2.5 KHz): Pole voltage, Line voltage, Motor no load current and their harmonic spectra

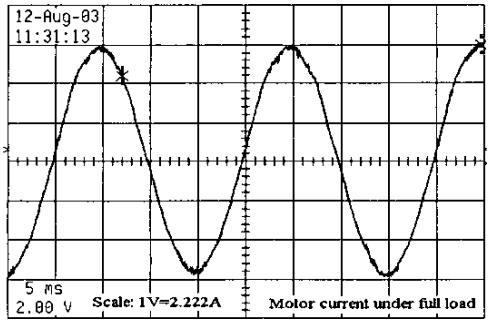


Fig. 12. Experimental results of SVPWM (Fs=50Hz, V_{dc}=570V, fsw=2.5 KHz): Motor current at full load

IV. EXPERIMENTAL IMPLEMENTATION

The SVPWM is implemented experimentally on TMS320 F240 DSP based digital controller. From the sampled reference vector the sector and sub-sectors are decided according to the algorithm given in section 11. The dwell time Tx, Ty and Tz of nearest three vectors are calculated using (3) For a given sector and sub-sector the six PWM outputs of full compare unit of the event manager module (EVM) are programmed independently to generate the required PWM sequence. These six outputs are used to generate gate signals for the upper six devices of the inverter. These outputs are complemented externally to generate gate signals for the lower six devices. The necessary dead times are generated externally. The SVPWM is applied to constant v/f drive consisting of 415V, 50Hz, 3 phase, 3KW, 8A, 1425 rpm, induction motor powered from three level IGBT based diode clamp inverter with D.C. bus voltage set to 570 volts. The typical experimental waveforms of phase voltage, line voltage and motor no lad current and their corresponding harmonic spectra at fundamental frequency Fs=50Hz, V_{dc}=570V, fsw=2.5KHz, are given in fig.11. The THD of the motor no load current gives a better measure of harmonic currents. As the load current increases, the fundamental component will increase as a result the current waveform will improve. The motor current under full load is shown in fig. 12. The THD of motor current under no load and full load conditions, computed from the experimental waveforms is 3.95% and 1.46% respectively.

V. CONCLUSIONS

The switching sequences of SVPWM and SPWM are analyzed. It is shown that even though the switching sequences of both the techniques are same, it is the placement of small space vectors as the beginning and ending state in each sequence, with equal dwell time, makes SVPWM superior compared to SPWM in terms of ***THD***, current ripple and D.C. bus voltage imbalance. The mean square value of the flux ripple for SVPWM is plotted over entire linear range of m and it shows that the flux ripple and hence the THD will be low for m=0.5 and will increase as m is increased or reduced. Also it can be concluded that the placement of small vector has not much influence on ***THD*** at over modulation region. So in the over modulation region, for a given switching frequency, the clamping sequences will have better ***THD*** than the conventional PWM techniques.

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