Digital Implementation of a Line Current Shaping Algorithm for Three Phase High Power Factor Boost Rectifier without Input Voltage Sensing

Souvik Chattopadhyay, V. Ramanarayanan
Power Electronics Group
Department of Electrical Engineering,
Indian Institute of Science, Bangalore 560012, India
souvik@ee.iisc.ernet.in ,vram@ee.iisc.ernet.in

Abstract: **In this paper the implementation of a simple yet high performance digital current mode controller that achieves high power factor operation for three phase Boost rectifier is explained. This objective is achieved without input voltage sensing and without transformation of the control variables into rotating reference frame. The controller uses resistor emulator concept for shaping of input current like input voltage in discrete domain. In implementation Texas Instruments's DSP based unit TMS320F240F EVM is used as the digital hardware platform. The algorithm is tested on a 4Kw , 670V DC Output, Boost rectifier. The execution time of the control algorithm is found to be less than 40μsec.**

I. INTRODUCTION

Boost circuit has emerged as the most widely used topology for three phase high power factor rectification. The control strategy most often employed for Boost rectification controls the active and reactive components of the line current. For this purpose, the sensed currents, after three phase to two phase conversion, need to be transformed from stationary reference frame to the synchronously rotating reference frame of line frequency, so that they appear as dc quantities to the closed loop controller. As a result a PLL (Phase Locked Loop) becomes a necessity, which is not so easy to design, if various non-idealities like frequency variation and distortions in the line voltage waveform as would be present in a real life system, are to be taken into account.

The controller proposed in this paper eliminates the need for transforming any quantity from stationary reference frame to synchronously rotating reference frame. As a consequence the PLL is not required. The control objective is defined as : shape the line current like line voltage. This would ensure high power factor operation of the rectifier. In this controller, the switching states are determined by using two decoupled current mode controllers in α and β axes. Both are stationary reference frames and orthogonal to each other. However, the information obtained from the switching duty ratios of the α and β axis controllers are not directly useful to generate switching pulses of a three phase converter. This is due of the reason that the switching pulses of the converter should be generated in such a way that both the conditions imposed by the α and β axis controllers are satisfied simultaneously in each switching

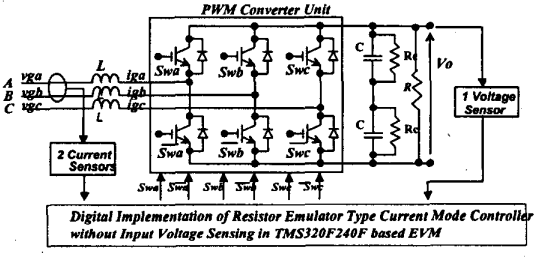

Fig.1 Overall schematic of three phase high power factor Boost rectifier

period. Some of the vectors produced by the switching of PWM converter have components on both the axes. So by taking the components on α and β axes, the controller determines the durations for which each of the two active vectors have to be applied in each switching period. The remaining time of the switching period is to be used as the null vector duration. This way both the equations can be satisfied simultaneously . Along with this, the self synchronizing algorithm keeps track of the sector in which the voltage vector must lie inorder to satisfy the control objective.

II. CONTROLLER

We can define the control objective of a three phase high power factor Boost rectifier, shown in Fig.1, as

$$\overline{i_g} = \frac{\overline{v_g}}{R_e} \tag{1}$$

where R_e is the emulated resistance of the rectifier. The $\overline{(\ )}$ above a variable indicates a space phasor. Our definition of voltage vectors and the corresponding sectors are shown in Fig.2. The mathematical description of the input voltage vector is

$$\overline{v_g} = v_{ga} + v_{gb}e^{j\frac{2\pi}{3}} + v_{gc}e^{\frac{j4\pi}{3}} \tag{2}$$

The current vector needs to be scaled by $\frac{2}{3}$ inorder to maintain power balance between input and output .

$$\overline{i_g} = \frac{2}{3}(i_{ga} + i_{gb}e^{j\frac{2\pi}{3}} + i_{gc}e^{j\frac{4\pi}{3}}) \tag{3}$$

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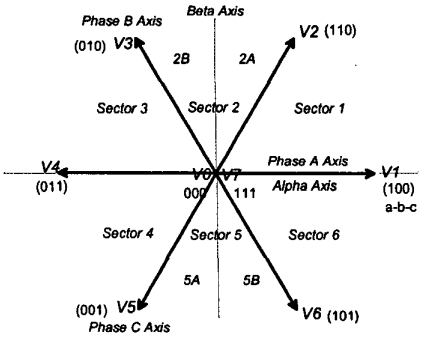


Fig.2 Voltage vectors produced by PWM converter

If we take components along α and β axes, which are stationary and orthogonal to each other, the control objective can be expressed in terms of two scalar equations

$$i_{g\alpha} = \frac{v_{g\alpha}}{R_e} \tag{4}$$

$$i_{g\beta} = \frac{v_{g\beta}}{R_e} \tag{5}$$

, as shown in Fig. 3.

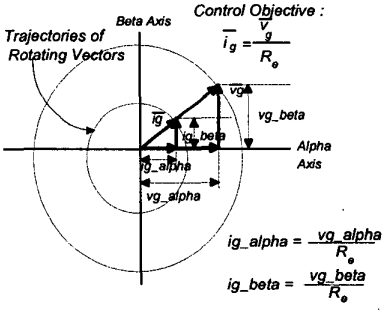


Fig.3 Control objectives in alpha and beta axes

This is equivalent to control of two single phase Boost rectifiers, one in α axis and the other in β axis, as shown in Fig.4. Let us first assume that the duty ratios d_α and d_β of these two switches Q_α and Q_β can be independently controlled. So, we can write,

$$i_{g\alpha pn} = \frac{V_o(1-d_\alpha)}{R_e} \tag{6}$$

$$i_{g\beta pn} = \frac{V_o(1-d_\beta)}{R_e} \tag{7}$$

, V_o is the regulated output of the three phase rectifier. Conceptually this is eqivalent to two current sources charging the same capacitor for voltage output. The control structure is also shown in Fig.4. In continuous time domain, $i_{g\alpha pn}$and $i_{g\beta pn}$ can be made to represent peak current [1], average current [2], or end of the period current [3] of the

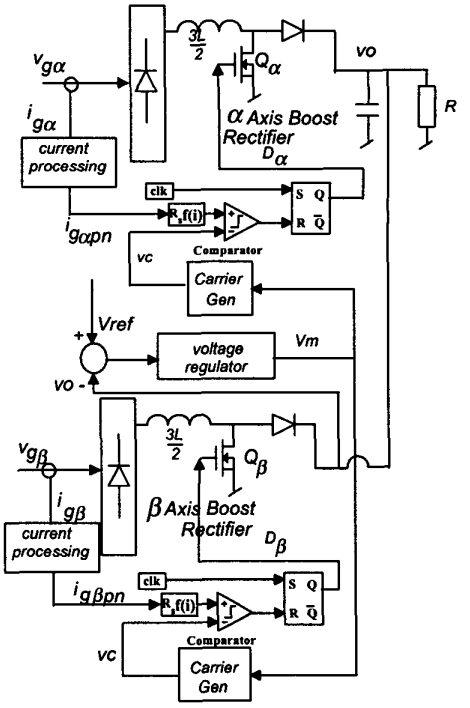


Fig.4. Functional representation of 3ph high power factor Boost rectifier with two independent single phase rectifiers in current mode control structure

inductor in every switching period T_s. This is shown in Fig. 5(a) ,5(b) and 5(c) respectively. However, in discrete implementation, current is sampled only once in a switching period. So, unless the sampling instant in a period is varied [4], the control objectives shown in Fig.5(a) or 5(b) can not be implemented. In contrast, Fig.5(c) is ideal for digital implementation, because the sampling instant can be kept fixed at the beginning of every switching period. We can calculate the duty ratios $d_a[n]$ and $d_\beta[n]$ from expressions (6) and (7), after replacing $\frac{V_o R_s}{R_e}$ by V_m in (4) and (5).

$$d_a[n] = (1 - \frac{i_{g\alpha pne}[n-1]R_s}{V_m}) \tag{8}$$

$$d_\beta[n] = (1 - \frac{i_{g\beta pne}[n-1]R_s}{V_m}) \tag{9}$$

The suffix $'e'$indicates that the current is sampled at the end of the period. It should be noted that the current at the end of period $[n-1]$is same as the current at the beginning of period $[n]$.This is shown in Fig.5(d). Here, R_s is the current sensing resistance. However, we need to satisfy (6) and (7) simultaneously in every switching period. So, from $d_a[n]$ and $d_\beta[n]$, we have to determine the time duration $T_1[n]$ and $T_2[n]$,for the two active vectors A_{v1}

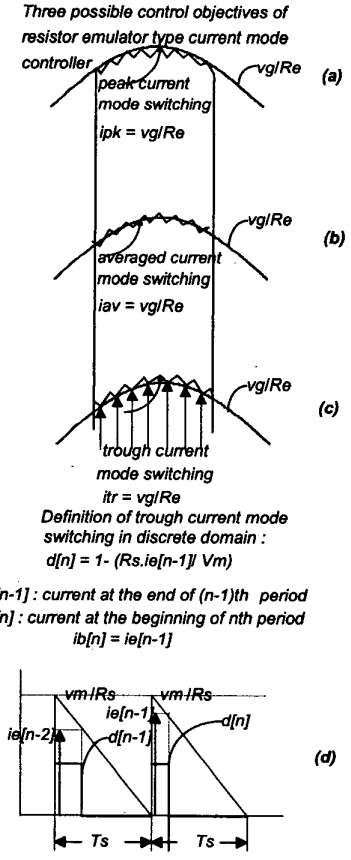


Fig.5 Discrete version of resistance emulator type current mode controller

and A_{v2} respectively, to effectively produce the same volt-sec on each axis as demanded by the independent controllers. The remaining time $T_o[n]$ of the period should be used for the null vector A_o. From Fig.6, it can be noted that if the active vectors A_{v1} and A_{v2} for sectors $1, 3, 4$ and 6 are identified as in *Table I*, then the corresponding time $T_1[n]$ and $T_2[n]$, needed for synthesis of any vector (P, Q, R or S) with an angle θ with respect to the α axis of the segment, can be obtained by solving the following simultaneous equations.

$$(\tfrac{1}{2}).T_1[n] + T_2[n] = (1-d_a[n])T_s \quad (10)$$

$$(\tfrac{\sqrt{3}}{2})T_1[n] = (1-d_\beta[n])T_s \quad (11)$$

Similarly for sectors $2A, 2B, 5A$ and $5B$,as shown in Fig.7, *Table II* gives the selection of vectors. The simultaneous equations (12) and (13) can be used to solve for $T_1[n]$ *and* $T_2[n]$.

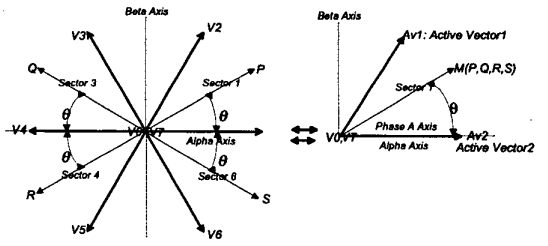


Fig.6 Mapping of P,Q,R,S vectors into M in Sector 1 of positive alpha-beta axis for solution of T1 and T2
For example : $A_{v1} = V_3$ and $A_{v2} = V_4$ for vector Q

Sector	A_{v1}	A_{v2}
1	*V2*	*V1*
3	*V3*	*V4*
4	*V5*	*V4*
6	*V6*	*V1*

TABLE I

$$(\tfrac{1}{2}).T_1[n] - (\tfrac{1}{2}).T_2[n] = (1-d_a[n])T_s \quad (12)$$

$$(\tfrac{\sqrt{3}}{2}).T_1[n] + (\tfrac{\sqrt{3}}{2}).T_2[n] = (1-d_\beta[n])T_s \quad (13)$$

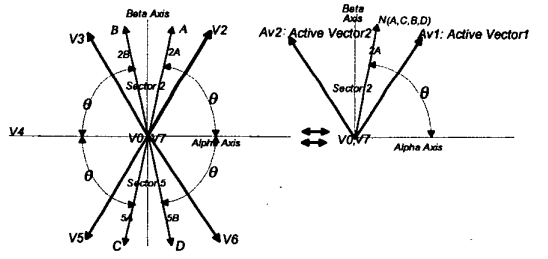


Fig.7 Mapping of A,B,C,D vectors into N in Sector 2A of positive alpha-beta axis for solution of T1 and T2
For example : $A_{v1} = V_2$ and $A_{v2} = V_3$ for vector A whereas $A_{v1} = V_3$ and $A_{v2} = V_2$ for Vector B

Sector	A_{v1}	A_{v2}
1	*V2*	*V1*
3	*V3*	*V4*
4	*V5*	*V4*
6	*V6*	*V1*

TABLE II

It can be seen that input voltage need not be sensed for computation of $T_1[n]$ and $T_2[n]$. However the sector information should be known for appropriate selection of active vectors. This controller implements self-synchronization of the converter switching with respect to line voltage based on the following logic: as long as the sector selection is correct , the α and β axis modulators will produce duty ratios less than 1, i.e, $d_\alpha[n] < 1$ *or* $d_\beta[n] < 1$. Further $T_2[n] > 0$ also has to be true for the modulator to operate in the unsaturated region. When any one of these conditions are violated , the next sector in sequence is chosen, as shown in Fig.8.

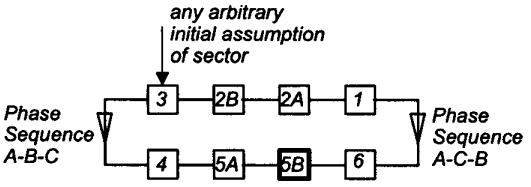


Fig.8 Sequence of sector change to be followed to eventually synchronize with the location of voltage vector : for example if the voltage vector is in sector 5B and the initial assumption of sector is 3 then 3,4 and 5A will not produce acceptable solution but the modulator will lock at sector 5B(A-B-C)

This sector change can take place in the same switching cycle in which the modulator had saturated because of initial incorrect selection of vectors. After that the modulator will recalculate the duty ratios, which won't saturate now as the sector selection is correct.

The current processing function of the modulator is explained below. First, the two phase currents $i_{ga}[n]$and $i_{gb}[n]$ are sensed and converted to $i_{g\alpha}[n]$ and $i_{g\beta}[n]$ by standard three phase to two phase transformation. However, the modulators work on DC quantities, so based on the sector information, we generate $i_{g\alpha pn}[n]$ and $I_{g\beta pn}[n]$, as shown in *Table III,* and use them in the modulator for calculation of duty ratios.

Sector	$i_{g\alpha pn}[n]$	$i_{g\beta pn}[n]$
1	$i_{ga}[n]$	$i_{g\beta}[n]$
2*A*	$i_{ga}[n]$	$i_{g\beta}[n]$
2*B*	$-i_{ga}[n]$	$i_{g\beta}[n]$
3	$-i_{ga}[n]$	$i_{g\beta}[n]$
4	$-i_{ga}[n]$	$-i_{g\beta}[n]$
5*A*	$-i_{ga}[n]$	$-i_{g\beta}[n]$
5*B*	$i_{ga}[n]$	$-i_{g\beta}[n]$
6	$i_{ga}[n]$	$-i_{g\beta}[n]$

TABLE III

The control algorithm is implemented on Texas Instruments DSP based-unit TMS320F240F EVM. It has three 16-bit registers CMP1, CMP2 and CMP3 to control the individual duty cycle of the switches as shown in Fig9. The values that need to be loaded on these registers to generate symmetrical PWM pulses are given in *Table IV.* The switch dead time is controlled by dead time control register . The six output signals are available on dedicated PWM output pins PWM1 to PWM6. If odd numbered signal is used for driving top device then even numbered i.e, odd number plus one, signal should be used for the bottom device.

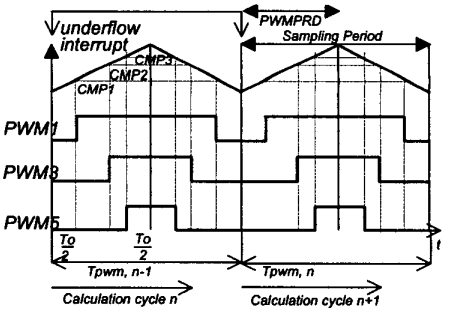


Fig.9 Generation of symmetrical PWM signals using Full Compare Unit of the TMS320F240 DSP Controller

Sector	*CMP1*	*CMP2*	*CMP3*
1	$T_x = (T_s - T_1 - T_2)/2$	$T_x + T_2$	$T_x + T_2 + T_1$
2*A*	$T_x + T_2$	$T_x = (T_s - T_1 - T_2)/2$	$T_x + T_2 + T_1$
2*B*	$T_x + T_1$	$T_x = (T_s - T_1 - T_2)/2$	$T_x + T_2 + T_1$
3	$T_x + T_2 + T_1$	$T_x = (T_s - T_1 - T_2)/2$	$T_x + T_1$
4	$T_x + T_2 + T_1$	$T_x + T_1$	$T_x = (T_s - T_1 - T_2)/2$
5*A*	$T_x + T_2 + T_1$	$T_x + T_2 + T_1$	$T_x = (T_s - T_1 - T_2)/2$
5*B*	$T_x + T_2$	$T_x + T_2 + T_1$	$T_x = (T_s - T_1 - T_2)/2$
6	$T_x = (T_s - T_1 - T_2)/2$	$T_x + T_2 + T_1$	$T_x + T_2$

TABLE IV

III. DCM OPERATION

The modulator proposed in this paper is capable of shaping the input current like input voltage as long as the converter operates in CCM. We have shown in Fig. 4 that functionally a three phase Boost rectifier works like two single phase Boost rectifiers connected to the same output capacitor. For DCM analysis we need to consider any one of these two single phase converters as the other works in a similar manner using the same values of circuit components and also switching at the same frequency. Normally in DCM analysis inductor current is considered to be zero at the beginning of a switching cycle and the condition is derived for it to become zero again before the end of the switching cycle. We can not apply the same condition here as the modulator will produce duty ratio equal to one if the inductor current is zero at the beginning of a switching cycle, therefore the current in the same period can only increase. However in the subsequent cycle the inductor current can fall to zero and may reverse if bi-directional current switches are used. The following analysis derives the condition for the DCM operation of the equivalent

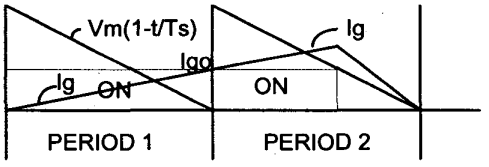


Fig.10 The inductor current of the converter is at the boundary between the Continuous and Discontinuous Conduction Mode of operation . The current is zero at the beginning of period 1 and falls to zero at the end of period 2.

single phase rectifier. The assumption made here is that the input voltage in two consecutive switching periods remains constant as the switching frequency is much higher than the line frequency.

The initial current for the present period when the converter enters into DCM is

$$I_{go} = \frac{2v_g}{3L}T_s \tag{14}$$

The duty ratio can be solved for d as

$$d = 1 - \frac{\frac{2v_g}{3L}T_s}{\frac{V_o}{R_e}} \tag{15}$$

from Fig.10, the condition for the DCM operation can be derived as

$$I_{go} + \frac{2v_g}{3L}dT_s < \frac{2(V_o - v_g)}{3L}(1-d)T_s \tag{16}$$

By replacing d in (16) by the expression of (15) we can get

$$\frac{3L}{RT_s} < M_g^2 \tag{17}$$

M_g is defined as the ratio of the peak input to output voltage

$$M_g = \frac{V_{g,peak}}{V_o} \tag{18}$$

R is load of the three phase Boost rectifier. The load resistance of the equivalent single phase rectifier is $2R$ since both the α axis and β axis rectifiers charge the output capacitor in parallel. Similarly from voltage and power balance conditions we get $\frac{3}{2}L$ as the inductance of the equivalent single phase rectifier, where L is the per phase inductance of the three phase system . Expression (17) shows that the converter can either be in CCM or in DCM , i.e, over a line half cycle it can not change from DCM to CCM and then from CCM to DCM as happens in [2].

IV. LOW FREQUENCY MODEL

The objective of this section is to develop a low frequency ,i.e, much lower than four times the line frequency, small signal, linear model of the three phase Boost rectifier controlled by the current mode modulator explained in this paper ,such that the voltage control transfer function $G_v(s) = \frac{\tilde{V}_o(s)}{\tilde{V}_m(s)}$ can be derived. This is required for the design of the voltage regulator, as shown schematically in Fig.11 .

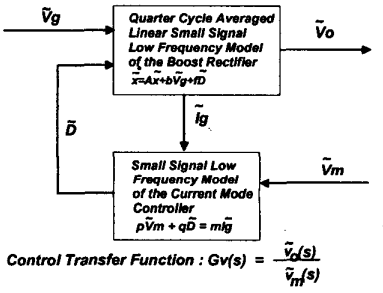


Fig.11 Definition of the Control Transfer Function $G_v(s)$ for the linear, low frequency, small signal model of the three phase Boost rectifier

We use the equivalent circuit of Fig.4 and average all the variables over quarter cycle of the line frequency waveform. The averaged variables of α and β axis rectifiers then become equal, and are no more unique. Therefore in subsequent analysis the variables are denoted by capital letters and are used without any suffix α or β. This results in an equivalent single phase system , with two states , the low frequency dynamics of which can be expressed as

$$\frac{3}{2}L\frac{dI_g}{dt} = V_g - (1-D)V_0 \tag{19}$$

$$C\frac{dV_o}{dt} = \frac{I_g}{(1-D)}M_g^2 - \frac{V_o}{R} \tag{20}$$

The low frequency model of the modulator is given by

$$V_m(1-D) = I_{ge}R_s \quad (21)$$

The more accurate relationship between I_g and I_{ge} can be expressed by (22), however in order to keep the derivation simple we ignore the effect of ripple on the inductor current and use the approximation of (23).

$$I_{ge} + \frac{V_g T_s}{3L} - \frac{(v_g i_{ge})_m R_s T_s}{3LV_m} = I_g \quad (22)$$

$$I_{ge} = I_g \quad (23)$$

The low frequency , small signal ,denoted by (~) over the variable, linear model of the converter can be expressed as

$$\frac{3}{2}L\frac{d\widetilde{I_g}}{dt} = \widetilde{V_g} - (1-D)\widetilde{V_0} + V_o\widetilde{D} \quad (24)$$

$$C\frac{d\widetilde{V_o}}{dt} = M_g^2 I_g\widetilde{D} + M_g^2(1+D)\widetilde{I_g} - \frac{\widetilde{V_o}}{R} \quad (25)$$

Using (21) and (23) , the low frequency ,small signal linear model of the modulator can be obtained

$$(1-D)\widetilde{V_m} - V_m\widetilde{D} = R_s\widetilde{I_g} \quad (26)$$

Now we can follow the same procedure as described in [5] to eliminate $\widetilde{I_g}$ and $\widetilde{D}$ from (25) using (24) and (26) inorder to determine the voltage control transfer function.

$$\frac{\widetilde{V_o}(s)}{\widetilde{V_m}(s)} = \frac{M_g^2(1-D^2)(1+\frac{3(1-D)sL}{2(1+D)M_g^2R})}{K[1+s(\frac{3LV_m}{2RV_o}+CR_s)\frac{1}{K}+s^2LC\frac{3V_m}{2V_o}\frac{1}{K}]} \quad (27)$$

The constant K is replacement of the expression

$$K = \frac{R_s}{R}(2D-D^2) + M_g^2(1-D^2)\frac{V_m}{V_o} \quad (28)$$

V. DIGITAL IMPLEMENTATION IN TMS320F240:

All the functions of the controller are implemented on the digital hardware platform of TMS320F240 Evaluation board. In each sampling period of 100μ sec, the ADC samples two phase currents and the DC output voltage with a total conversion time of 13μ sec. The GP timer 1 is put in continuous up down counting mode as shown in Fig.9, in the initialization part of the program. The execution of the control loop is initiated by the GP timer1 underflow interrupt. The current mode control calculations for the two axes are performed each time the control loop is executed. The current mode controllers receive as input the output of the DC voltage regulator. The duration for which each switch of the three phase converter is to be turned ON is computed from the timing results of the two current mode controllers. These values are loaded to the Full compare units of the Event Manager Module. Necessary adjustments to the basic ON and OFF times of each switch are performed in the Dead band units. The Output logic units determine the logic level of each PWM output. The execution time of the control algorithm is found to be about 40 μsec with a CPU clock frequency of 20MHz.

VI. EXPERIMENTAL RESULTS

The control algorithm is tested for experimental verification on a 4 Kw, 670V regulated DC Output Boost rectifier unit. The line inductance is 3.6mH/phase, PWM Period of the IGBT based converter is 50μ Sec. The line current and voltage waveforms are analyzed using *'LEM'* made *HEME ANALYST 2060* meter. Power factor greater than 0.995 and T.H.D less than 5% are achieved on line current over a load range of 20% to 110%.

Fig.12 verifies the high power factor operation by showing the phase voltage and phase current waveforms.

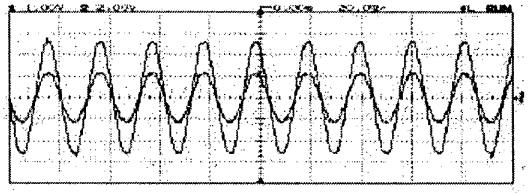
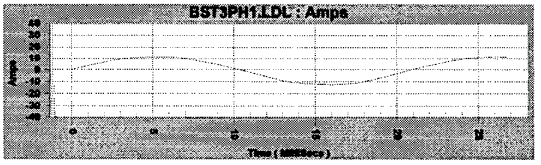


Fig.12 CH1: Phase Current, Scale 1V=> 5 Amps
CH2: Phase Voltage, Scale 1V=> 70 Volts

The experimental waveforms shown in Fig.13 to 16 are obtained for the test condition of 3.95Kw output , 270V AC(L-L) input, 670V DC output. Some of the variables , for example, i_{ga}, are displayed through unipolar DAC of on board TMS320F240 EVM, so 2.5V DC shift can be seen.



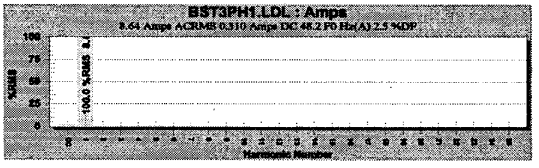


Fig.13(a)

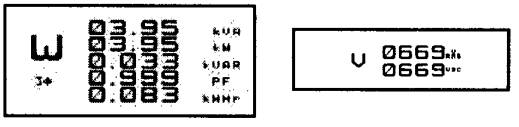


Fig.13(b)

Fig.13 Measurement results from LEM HEME ANALYST 2060. (a) Line Current (RMS 8.64A,DF 2.5%)
(b) Measurement of 3Phase power 3.95Kw at p.f 0.999 and regulated DC voltage output at 669V(front panel reading of the meter is shown), input voltage is 263V rms (line to line) with DF of the line voltage is1.8% (not shown)

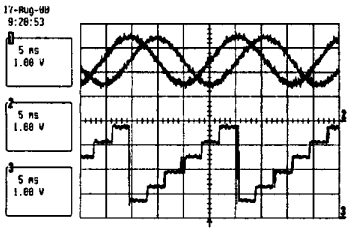


Fig.14 (a)

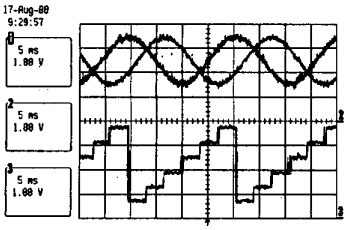


Fig.14 (b)

*Fig.14 Experimental results (a) Ialpha(ch1),Ibeta(ch2) and Sector(ch3) (b) Ia(ch1), Ib(ch2) and Sector display ('1' to '6') (ch3) ,Current Scale : 1V = 12.2Amps, Sector Scale : '1' = 0.625V * Note that the current signals are unipolar because of the unipolar DAC*

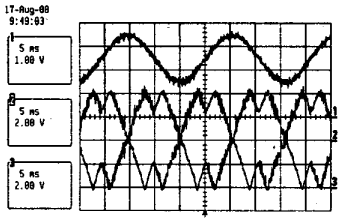


Fig.15(a)

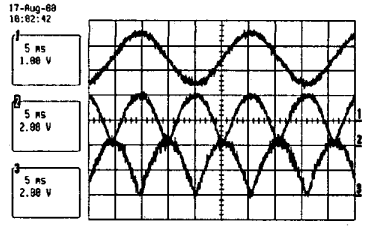


Fig.15(b)

Fig.15 Experimental results (a) Ialpha(ch1),T1 (ch2) and T2(ch3)(b) Ialpha(ch1) ,Toff_alpha(ch2) and Toff_beta(ch3) Current Scale: 1V = 12.2Amps Time Scale : 1V = 10.2μ Sec Note that the signals are unipolar because of the unipolar DAC*

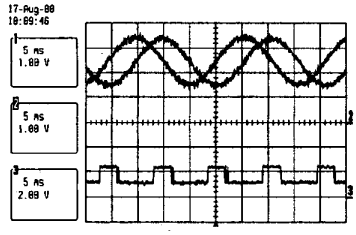


Fig.16(a)

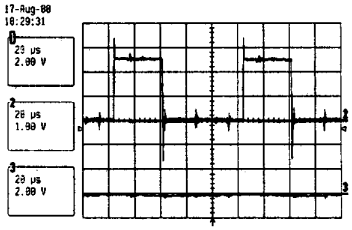


Fig.16(b)

Fig.16 Experimental results (a) Ialpha(ch1), Ibeta(ch2) and A signal showing the mapping all sectors into Sector1(Low level) and Sector2A (High level)(ch3) (b) Control loop time i.e :signal high duration(ch1)

VII. CONCLUSION

This paper describes the DSP based implementation of a discrete current mode control algorithm that performs high power factor rectification for a three phase Boost converter. The salient features of this controller are : (1) No input voltage sensing is required, as switching pulses get self-synchronized with the line frequency, (2) No need to use PLL, as the controller works in stationary reference frame, (3) Two decoupled fixed frequency current mode controllers are used to generate the equivalent ON and OFF durations, (4) A combined switching strategy is developed in the form of space vectors to simultaneously satisfy the timing requirements of both the current mode controllers in a switching period. In conclusion, it can be said that, this method of control of three phase high power factor Boost rectifier provides comparable or better performance over existing methods with a much simpler control structure.

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