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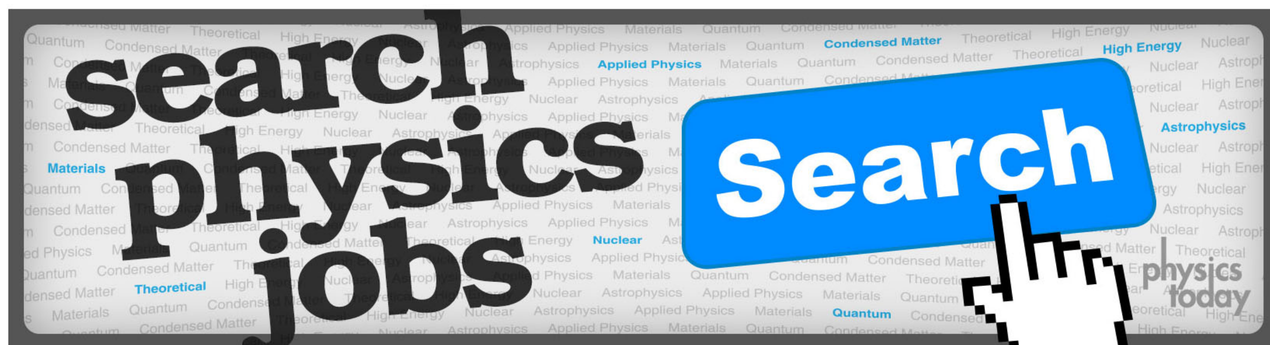

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AIP ADVANCES **5**, 117122 (2015)

DLTS analysis of amphoteric interface defects in high-TiO_2 MOS structures prepared by sol-gel spin-coating

Arvind Kumar, Sandip Mondal, and K. S. R. Koteswara Rao[a]
Department of Physics, Indian Institute of Science, Bangalore, 560012, India

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High-κ TiO_2 thin films have been fabricated from a facile, combined sol – gel spin – coating technique on p and n type silicon substrate. XRD and Raman studies headed the existence of anatase phase of TiO_2 with a small grain size of 18 nm. The refractive index 'n' quantified from ellipsometry is 2.41. AFM studies suggest a high quality, pore free films with a fairly small surface roughness of 6 Å. The presence of Ti in its tetravalent state is confirmed by XPS analysis. The defect parameters observed at the interface of Si/TiO_2 were studied by capacitance – voltage (C – V) and deep level transient spectroscopy (DLTS). The flat – band voltage (V_{FB}) and the density of slow interface states estimated are – 0.9, – 0.44 V and 5.24×10^{10}, 1.03×10^{11} cm^{-2}; for the NMOS and PMOS capacitors, respectively. The activation energies, interface state densities and capture cross – sections measured by DLTS are $E_V + 0.30$, $E_C - 0.21$ eV; 8.73×10^{11}, 6.41×10^{11} eV^{-1} cm^{-2} and 5.8×10^{-23}, 8.11×10^{-23} cm^2 for the NMOS and PMOS structures, respectively. A low value of interface state density in both P- and N-MOS structures makes it a suitable alternate dielectric layer for CMOS applications. And also very low value of capture cross section for both the carriers due to the amphoteric nature of defect indicates that the traps are not aggressive recombination centers and possibly can not contribute to the device operation to a large extent. © *2015 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License.* [http://dx.doi.org/10.1063/1.4935749]

I. INTRODUCTION

In order to achieve the continuous downscaling and enhanced performance of complementary metal oxide semiconductor (CMOS) devices, intense research is devoted in probing the high-permittivity (κ) dielectric materials, to substitute the conventional SiO_2 with its excessive gate leakage current due to direct tunneling at thicknesses of ≤ 1.2 nm.[1–3] Among the various high-κ dielectrics reported so far, titania seems to be a suitable alternative owing to its exceptional physico-chemical and optoelectronic properties.[4–8] The dielectric constant of titania is very high, with rutile form exhibited higher values (10 – 170) as compared to anatase form (40).[9,10] The deposition of titania by the vacuum based processes are extensively investigated, but requires additional care during the process.[11–14] Alternatively, solution based process is quite attractive, as the crystalline titania can be obtained with high purity and chemical homogeneity.[15] In addition the solution deposition process is a simple and cost effective approach for the fabrication of large area films with diverse compositions and is applicable to flexible and transparent electronic device systems. Recently, the effects of the processing variables on the chemical composition, interfacial reactions, and dielectric properties of TiO_2/Si films deposited by a sol-gel route have been reported.[16–19] In spite of the numerous applications of TiO_2/Si stack, there are only a few reports in the literature that deal with the electrical properties of solution based TiO_2 films deposited on Si substrate.[20,21] A better quantitative understanding of interface traps, capture cross – sections permits the exact calculation of surface recombination rates, which might have a significant influence on the device performance

[a]Email: ksrkrao@physics.iisc.ernet.in; raoksrk@gmail.com

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such as reliability and mobility degradation.[22] Deep – level transient spectroscopy (DLTS) allows an estimation of density of localized states, position in Si band gap and their capture cross – sections at the oxide – semiconductor interface with improved accuracy than the capacitance – voltage and conductance technique. In metal – oxide – semiconductor (MOS) structures, the DLTS method consists of filling the interface trap during the pulse, then analyzing the emission rate during a temperature scan.[23–25]

In this work the TiO_2 films were fabricated by a facile route, combined sol – gel spin–coated process; it severely reduces the cost of the fabrication process. Thus made films were characterized and found to have good quality, further TiO_2 films have been incorporated in to the MOS structure for electrical characterization. The TiO_2/Si interface state density (D_{it}), capture cross – section (σ_p) of traps present has been investigated by sensitive DLTS technique.

II. EXPERIMENTAL

A. Sample Preparation and MOS capacitor fabrication

The TiO_2 film was fabricated on Si substrate as reported previously from our group.[26,27] Briefly, the titanium isopropoxide (TTIP) precursor solution was spin – coated on oxygen plasma treated p and n-type Si (100) substrates (4000 rpm, 30s) and then baked on a hot plate at 100 °C for 5 min. Prior to the deposition of TiO_2 thin films, Si wafer was cleaned with piranha solution (H_2SO_4:H_2O_2 is 3:1) followed by 1% HF dipping for 10 s to remove any native oxide layer and dried under nitrogen ambience. The piranha cleaned Si substrates were treated with O_2 plasma for 20 min in an oxygen plasma chamber (Harrick Scientific Corp.) at 0.008 mbar to resolve the problem of poor adhesion between TiO_2 thin films and Si substrate. The obtained films were subjected to annealing at 600 °C for 1 h in a preheated horizontal furnace. The electrical exploration was carried out using metal–Oxide–semiconductor (MOS) structure with Ag as a back contact. The Al metal was evaporated using thermal evaporation method through a metal shadow mask with a circular hole (d = 288 µ) on the samples as front contacts. The Al gate layer has a thickness of 200 nm. [Figure S1, flow chart diagram for the preparation of TiO_2 thin films].[51] Hereafter, we refer MOS structures fabricated on p-Si and n-Si substrates as NMOS and PMOS, respectively. DLTS measurements, the devices were mounted on T05 header.

B. Characterization

The X-ray diffraction patterns were recorded over a 2θ range of 20 – 80° at a scan rate of 2° per min on a Rigaku X-ray diffractometer under GIXRD (glancing incidence x-ray diffraction) mode. GIXRD mode is preferred due to small thickness of the film. The operating voltage and operation current were 40 kV and 30 mA, respectively. The Raman spectra were obtained in back–scattering configuration using a Horiba JobinYvon Lab RAM HR instrument. The excitation wavelength was 514.5 nm line using argon ion laser. The acquisition was 10 s and data was recorded using < 3 mW of laser power (at the laser head) with the spectral resolution was 0.4 cm^{-1}. The spectroscopic ellipsometry (SE) parameter allows the estimation of thicknesses and refractive index of the films. The measurements were performed using variable angle spectroscopic ellipsometry (M-2000, J.A. Woollam Co., Inc., USA). The experimental and fitted Ψ-Δ-λ plot of TiO_2 thin films is shown is figure S2.[51] The average thickness of the dielectric layer was found 91 nm. The thickness of the dielectric layer is verified with cross sectional SEM (figure S3).[51] The film surface roughness was measured by AFM (NDMDT Russia). The X-ray photoelectron Spectroscopy measurement was performed on an AXIS ULTRA from AXIS 165, using monochromatic Al Kα as the excitation source. All binding energies were calibrated to the C 1s peak at 284.8 eV of the surface adventitious carbon. Area of the device is measured by optical microscope and it was different from the mask area due to shadow effect. Metal – Oxide–Semiconductor (MOS) capacitors were used to investigate the electrical properties of the TiO_2 films. Capacitance – voltage (C–V) characteristics were estimated using an Agilent 4294A Precision Impedance Analyzer at 1 MHz with 5 mV AC modulation signal. DLTS measurements have been performed at temperatures ranging from 100 – 350 K

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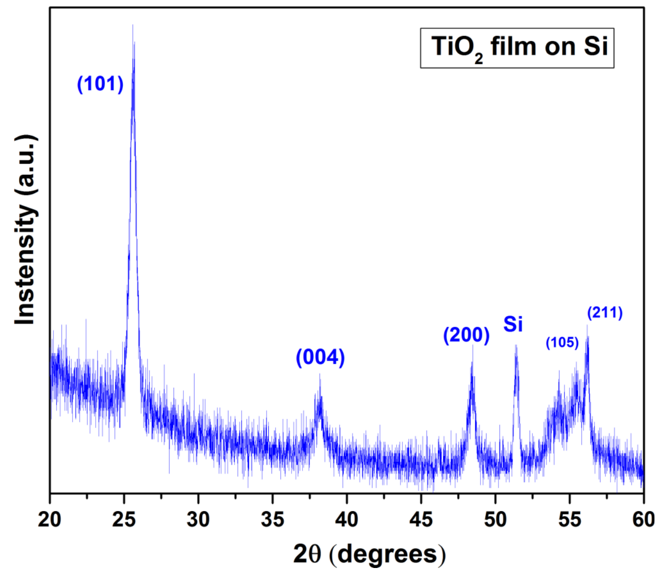

FIG. 1. XRD Spectra of 600 ^{0}C annealed TiO_2 film deposited on Silicon substrate.

in a liquid nitrogen cryostat. A pulse generator (HP 8112A) and a very sensitive Boonton 7200 capacitance meter at 1 MHz frequency integrated to a homemade automated boxcar – averaging unit was used for DLTS measurements.

III. RESULTS AND DISCUSSION

A. Structural Characterization

Figure 1 shows the XRD of the film. The as deposited film was amorphous and 600 °C annealed films shows anatase phase of TiO_2. The (101) reflection is the only prominent peak and the intensity of other diffraction planes in the patterns are very small. The grain size of the films was calculated from the full width at half maximum intensity (β) of the prominent (101) peak using Debye–Scherrer's equation

$$D = \frac{0.89\lambda}{\beta \cos\theta} \tag{1}$$

Where, λ is the wavelength of the X-rays and θ the Bragg diffraction angle. The average grain size was found to be 18 nm.

The Raman spectra of TiO_2 films are shown in Figure 2. According to Factor group analysis, anatase has six Raman active modes (A_{1g}+$2B_{1g}$+$3E_g$), three infrared active modes (A_{2u}+$2E_g$) and one vibration of B_{2u}, which is inactive in both infrared and Raman spectra.[28] The film annealed at 600 °C showed intense band at 143 cm^{-1} followed by weak bands at 396, and 637 cm^{-1}, which were assigned respectively to $E_g(\upsilon_6)$, B_{1g} (υ_4), and $E_g(\upsilon_1)$ modes of anatase. The results of Raman analysis were in outstanding agreement with XRD analysis. The prominent band of anatase at 198 and 516 cm^{-1} could not be observed, as they overlap with Raman peaks of Si substrate. This information was confirmed by the presence of all the Raman peaks when TiO_2 was deposited on quartz substrate.

Figure 3(a) and 3(b) shows the AFM images of annealed TiO_2 thin films in two and three dimensions, taken by the instrument ND – MDT in non – contact mode of operation with the help of 100 μ scanner. High quality films, without any crack and with small surface roughness 6 Å were observed for the films deposited here. The small surface roughness (smooth surface) is desirable for the device operation, as it is helpful to enhance the mobility of channel layer.[1]

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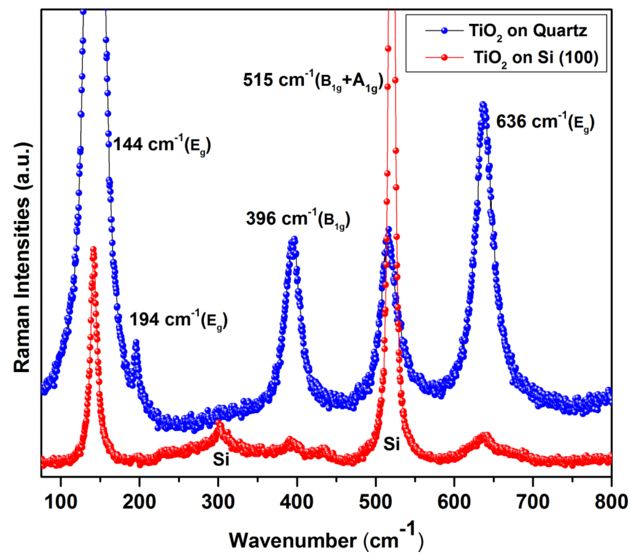
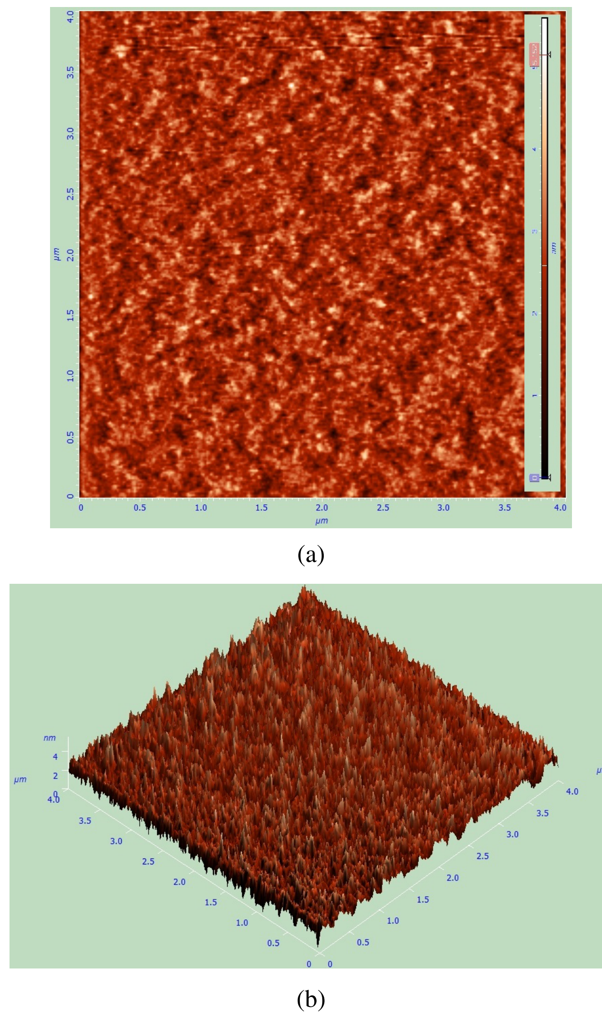


FIG. 2. Raman Spectra of 600 ^{0}C annealed TiO_2 film on Silicon and quartz substrates.



(a)

(b)

FIG. 3. AFM images of 600°C annealed TiO_2 film on Si (100); a) Two dimensional view; b) Three dimensional view.

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The porosity of the films was calculated using Eq. (2)[29]

$$Porosity = 1 - \frac{n^2 - 1}{n_d^2 - 1} \tag{2}$$

where n is the refractive index of the films calculated from refractive index as a function of wavelength at 550 nm (shown in figure S4), n_d is the refractive index of pore free anatase TiO_2 film having a value of 2.52.[29,30,51] We observed relatively high value of refractive index 2.41 for the films annealed at 600 °C that is in close agreement with the pore free anatase TiO_2.[19,29] The high value of refractive index for our films suggests relatively a dense film, which is in consistent with our AFM studies. The porosity calculated using Eq. (2) is 10 %.

Figure 4(a) shows the XPS survey scan spectra of the 600°C annealed TiO_2 films. The XPS measurements were carried out to investigate the valence state of titanium as well as oxygen vacancy, which is a major defect sites in TiO_2. Figure 4(b) shows the Ti 2p XPS core level spectra of 600 °C annealed films. The core level binding energy of Ti $2p_{3/2}$ and Ti $2p_{1/2}$ are ~459.71 and 465.50 eV respectively. The Ti 2p signals are highly symmetric, and no shoulders were observed towards the lower energy sides. This concludes that the defect concentration with Ti^{3+} is extremely low. The difference of 5.79 eV between the peaks indicates the presence of titanium in its tetravalent state[31,32] Figure 4(c) shows the O1s XPS core level spectra of 600 °C annealed TiO_2 films. The

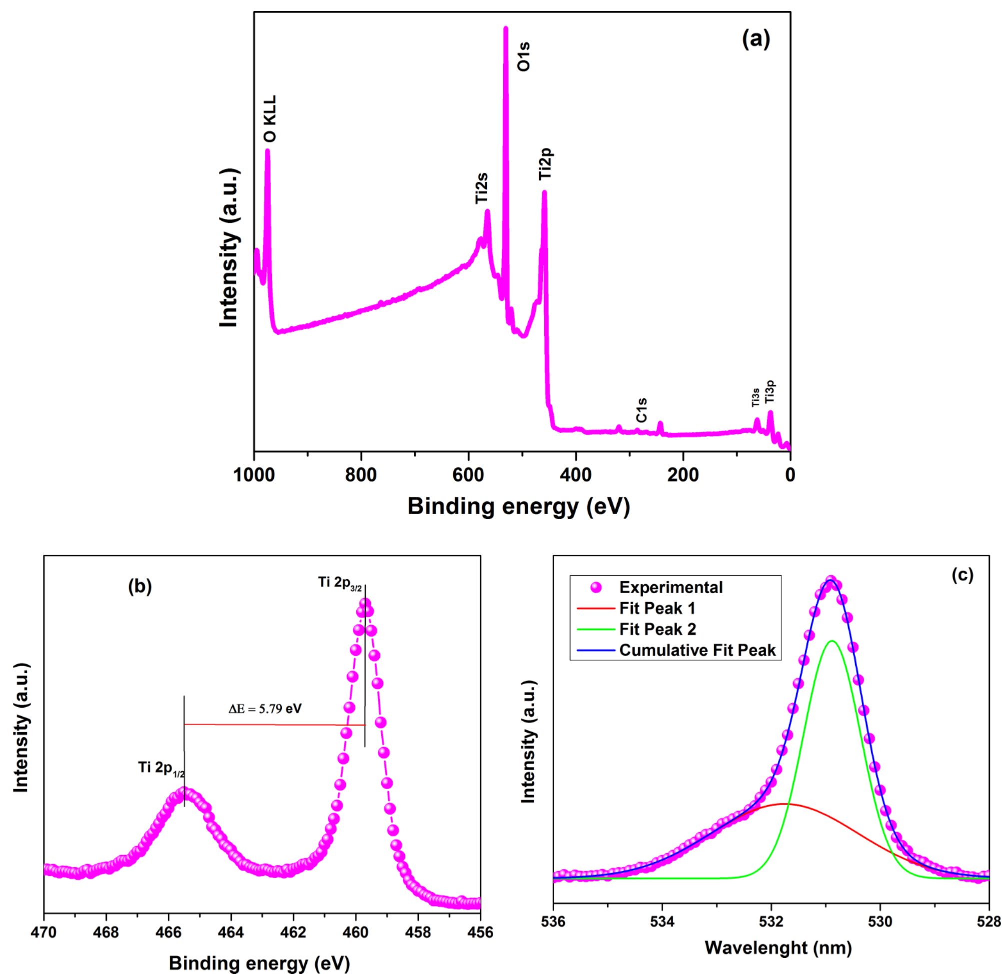

FIG. 4. (a) XPS survey scan spectra of 600 °C annealed TiO_2 films. (b) Ti 2p XPS core level spectra of 600 °C annealed TiO_2 films. (c) O1s XPS core level spectra of 600 °C annealed TiO_2 films.

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strong photoelectron signals ~530.0 eV is assigned to bulk lattice oxygen.[33] The slightly asymmetric nature is attributed to the presence of residual or contaminated hydroxyl species on the TiO_2 surface during the fabrication or characterization process.[34]

B. Electrical Characterization

1. Capacitance–Voltage characteristics

Prior to DLTS measurements C-V measurements were performed to define the proper bias for DLTS experiment and to extract various parameters, such as doping density of Si used, flat band voltage (V_{FB}), change in flat band voltage (ΔV_{FB}), number of slow traps, oxide accumulation and depletion capacitance of NMOS and PMOS. High frequency C-V characteristics of both type Al/TiO_2/Si MOS device depicts in Figure 5. The schematic diagram, micrograph of device mounted on TO5 header is shown as inset (a) and (b) of the figure 5. The C – V characteristic shows proper accumulation, depletion and inversion region with a small hysteresis (ΔV_{FB} = 10 mV for NMOS, ΔV_{FB} = 20 mV for PMOS), while sweeping the voltage from -3 to 3 and again back to -3. The hysteresis (change in flat band voltage) was caused by charge trapping (slow interface states) at the interface. Through Columbic force these interface states can interact with carriers in channel and bring down the carrier mobility.[35] Therefore, the charges at the interface of TiO_2/p-Si need to be reduced. Small densities of slow interface states 5.24×10^{10} cm^{-2} for NMOS and 1.03×10^{11} cm^{-2} for PMOS were estimated for our device using the Eq. (3).[36]

$$N_{SIT} = \frac{C_{ox}\Delta V_{FB}}{q} \tag{3}$$

Where (ΔV_{FB}) is change in flat band voltage, 'C_{OX}' is the accumulation capacitance and 'q' is the electronic charge.
The dielectric constant were calculated from accumulation capacitance using Eq. (4).[1]

$$k = \frac{C_{ox}t_{ox}}{\varepsilon_0 A} \tag{4}$$

Where, C_{ox} is the accumulation capacitance, A is the area of top gate electrode, t_{ox} is the thickness of TiO_2 films incorporated in to the MOS structure and ε_0 is the permittivity of free space. The

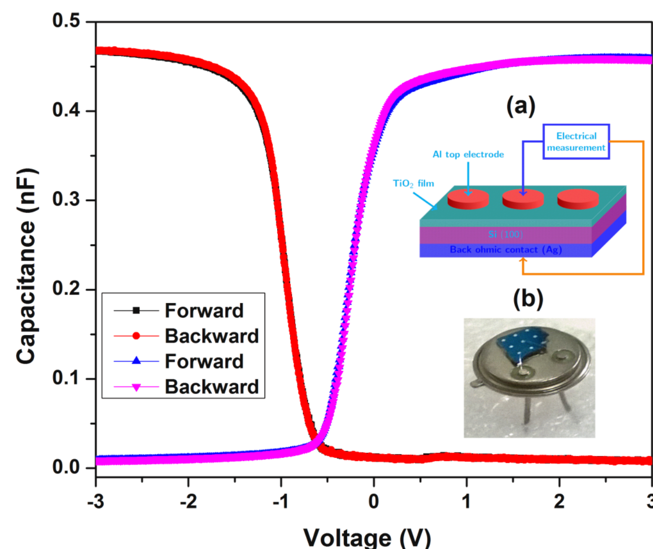

FIG. 5. Capacitance -Voltage (C-V) characteristic of Al/TiO_2/Si (100) NMOS and PMOS structure. Inset: (a) shows the device schematic diagram; (b) shows the device micrograph of Al/TiO_2/Si (100) MOS structure mounted on TO5 header for DLTS measurement.

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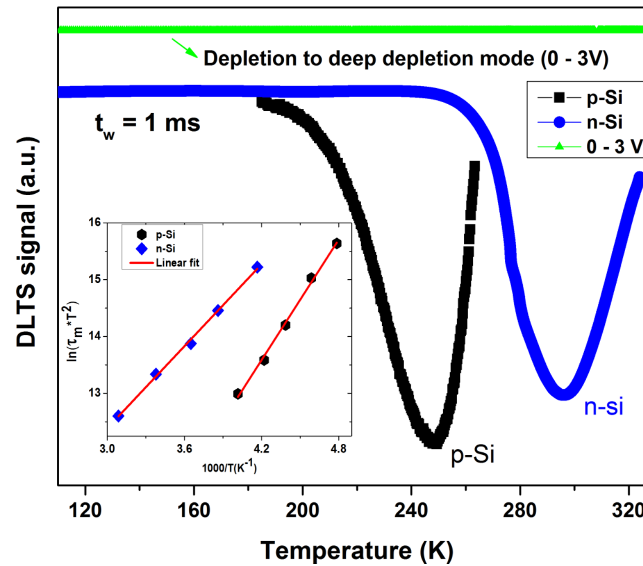

FIG. 6. DLTS spectra of Al/TiO_2/Si (100) MOS structure for p and n type Si substrate at rate windows (t_w) = 1 ms. DLTS spectra under bias pulse from depletion to deep depletion (0 to 3 V) is also shown in figure and found to have no peak in the entire temperature scan. Inset: Corresponding Arrhenius plot of both type Al/TiO_2/Si (100) structures extracted from DLTS spectra.

Equivalent oxide thickness (EOT) was estimated to be ~ 4.5 nm. The flat band voltage (V_{FB}) was – 0.9 V for NMOS and – 0.44 V for PMOS. A narrow hysteresis loop [Change in flat band voltage (ΔV_{FB}) during bidirectional C-V sweep)] indicates a very small amount of trapping charges within the films and interface of TiO_2/Si.

2. DLTS measurements

Figure 6 is the typical DLTS spectra at 1 ms rate window (t_w) for both the type of MOS structure. A peak around 250 K for NMOS and around 296 K was observed for PMOS, when filling pulse is applied from accumulation to depletion region for both the samples (-1.5 to 1 V for p-Si and 1.5 to -1 V for n-Si). The width of the filling pulse was chosen as 5 ms for all the rate windows. With increasing rate window, there is relative change in the strength of the DLTS peak (decreases) and also shifts towards low temperature, which is a commonly observed feature of the DLTS spectra.[22] To confirm the origin of the DLTS signal is indeed from the interface states but not from the bulk, a bias pulse from depletion to deep depletion (0 to 3 V for NMOS) is applied and found to have no peak in the entire temperature scan (Fig 6), which is consistent with the technique normally followed in MOS structures.[37]

The hole emission rate is given by

$$e_p = \sigma_p V_{th} N_v \exp\left[-\frac{(E_T - E_V)}{kT}\right] \tag{5}$$

Where σ_p is the hole capture cross section, V_{th} is the thermal velocity, N_V is the effective density of states, k is the Boltzmann constant, and T is the temperature in Kelvin.
From Eq. (5), a graph can be plotted between $\ln(\tau_m T^2)$ vs 1000/T, frequently known as Arrhenius plot, the activation energy (E_T) is calculated.

$$E_T = 1000 \times 8.617 \times 10^{-5} \times slope \tag{6}$$

The corresponding Arrhenius plots of TiO_2 MOS structures [Inset of fig. 6], which is extracted from DLTS spectra, the slope was found to be 3.48 and 2.40 for NMOS and PMOS respectively. From the slope, the activation energy of the trap (E_T) is estimated to be 0.30 eV for p-Si substrate and

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0.21eV for n-Si substrate. The observed value of activation energy is very close to the P_b0 center (0.25 and 0.27 eV) at Si/SiO_2 interface.[24,38] An activation energy of 0.3 eV and 0.25eV has been reported by Johnson *et al*. for for Si/SiO_2 based NMOS and PMOS structure respectively, however the study of Zhan *et al*. for interface characteristics in HfAlO/Si MOS structure shows 0.33 eV.[39,40] Hence, the value of activation energy obtained in the present study is consistent with Si/SiO_2 (native Oxide) and Si/high-k (non-native Oxide) MOS structure prepared by different deposition methods, though the origin and the nature of the defect is still elusive. However, A. Stesmans *et al*. studied the $Si\text{-}HfO_2$ system and suggested the possible formation of SiO_2 interlayer between Si and HfO_2; that makes the interface well like Si/SiO_2, the similar observation of interfacial properties for the Si/TiO_2 in the present studies.[41] The study also reveals the similar amphoteric nature of $Si\text{-}TiO_2$ interface as in the case of $Si\text{-}SiO_2$.[39]
The interface state density (D_{it}) can be calculated using the relation[42,43]

$$D_{it} = \frac{\varepsilon_{si} C_{ox} N_A \Delta C}{C_0^3 kT \ln(t_2/t_1)} \tag{7}$$

Where 'ε_{si}' is the permittivity of Si, C_{OX} is the accumulation capacitance, N_A is the acceptor doping concentration, ΔC is the DLTS signal, C_o is the depletion capacitance.

The interface states (D_{it}) were estimated 8.73×10^{11} and 6.41×10^{11} eV^{-1} cm^{-2} for NMOS and PMOS, respectively using Eq. (7), which is an order of magnitude higher than $Al/SiO_2/Si$ MOS devices (D_{it} in $Al/SiO_2/Si$ is the benchmark).[44] Still this is an acceptable value for Si/high-k (non – native Oxide) MOS devices and consistent with other deposition methods.[45] A low value of interface state density in both P- and N-MOS structures makes it a suitable alternate dielectric layer for CMOS application.

The capture cross – section (σ) is estimated using insufficient filling DLTS (IF – DLTS) technique. The technique is time consuming but it provides an accurate estimation of capture cross – sections as compared to other methods like Charge pumping CP and variable duty cycle charge pumping (VDCCP).[46] In this method, when the NMOS capacitor gate bias is swept from positive to a negative, the holes get captured by the traps present at the interface. In similar manner when the PMOS capacitor bias is swept from negative to positive the electrons get captured by the traps present at the interface. However, as the probability of filling the traps depends on the pulse width, as it is insufficiently smaller, only a small fraction of the traps will be filled. Hence, the density of traps filled (d_{it}) and the pulse width (t_P) can be expressed as[36]

$$d_{it} = D_{it}[1 - \exp(-\frac{t_P}{\tau_c})] \tag{8}$$

Where, $\tau_c = 1/\sigma_p V_{th} p$ is the capture time constant and p is the density of holes in the valence band. Equation (7) clearly indicates that the DLTS signal (ΔC) is proportional to the interface state density (D_{it}); Hence Eq. (8) can be expressed as

$$\Delta C_{\max}(t_P) = \Delta C_{\max}(t_{LP})[1 - \exp(-\frac{t_P}{\tau_c})] \tag{9}$$

Where, $\Delta C_{max}(t_P)$ and $\Delta C_{max}(t_{LP})$ are the maximum DLTS signals as a function of filling pulse width (t_P), t_{LP} represent the long filling pulse width, where the DLTS signal saturate. Thus the plot of $\ln[1 - \frac{\Delta C_{\max}(t_P)}{\Delta C_{\max}(t_{LP})}]$ verses pulse width (t_P) gives a straight line, the slope of which yields the capture time constant (τ_c). Figure 7 shows the plot of $\ln[1 - \frac{\Delta C_{\max}(t_P)}{\Delta C_{\max}(t_{LP})}]$ as a function of pulse width (t_p). It is found to have non-linear behavior in the entire data range, which is attributed to the different capture rates of the free carrier tail extending into the depletion region, however, the initial part of the plot is fairly linear, which yields a reliable estimation of the capture constant (τ_c).[47] Capture cross- sections (σ_p, σ_n) can be estimated from the relation:

$$\sigma_p = \frac{1}{\tau_c V_{th} p} \tag{10}$$

The value of capture cross – sections estimated from equation (8) was 5.8×10^{-23}, 8.11×10^{-23} cm^2 for NMOS and PMOS interface defects. To the best of our knowledge, this is the first report on

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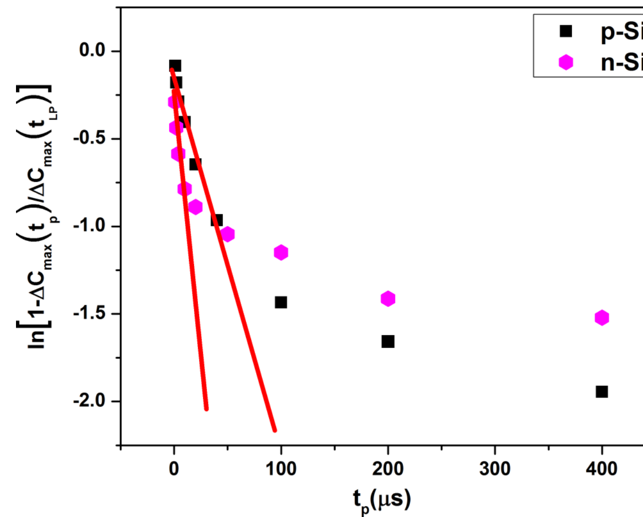

FIG. 7. The Plot of $\ln[1-\frac{\Delta C_{max}(t_P)}{\Delta C_{max}(t_{LP})}]$ as a function of pulse width (t_p), extracted from IF – DLTS spectra. The capture constant is estimated from the linear region of the plot.

the Al/TiO_2/Si MOS structure by DLTS technique. Jeon *et al.* had reported a similar value of 6.53×10^{-22} cm^2 for TiN/Al_2O_3/p-Si MOS capacitor.[48] The capture cross – section 6.44×10^{-22} cm^2 for the HfO_2/Si stack is recently reported by B. Raeissi *et al.* by TSC.[49] Very low value of capture cross indicates that the traps are possibly double acceptor states.[50] The absence of DLTS signal in the depletion – deep depletion mode (0 – 3 V) given in Fig. 6 also exhibits the nature of the traps, indicating that they may be acceptor states. Very low value of capture cross – section for both the carriers due to their amphoteric nature indicates that the traps are not aggressive recombination centers and possibly can not contribute to the device operation to a large extent.

IV. CONCLUSIONS

High quality TiO_2 thin films have been deposited by combined sol – gel spin – coating method. Both XRD and Raman studies directed the presence of anatase phase of TiO_2 with a small grain size of 18 nm. The refractive index measured from ellipsometry is 2.41 with an estimated porosity of 10%. AFM studies also suggest pore free films with small surface roughness of 6 Å and consistent with the results obtained from ellipsometric technique. The interface of Al/TiO_2/Si MOS structure is evaluated with C – V and DLTS techniques. The flat – band voltage (V_{FB}) and the density of slow interface states estimated are – 0.9, – 0.44 V and 5.24×10^{10},1.03×10^{11} cm^{-2} for the NMOS and PMOS structures, respectively. The activation energies, interface state densities and capture cross – sections measured by DLTS are $E_V +$ 0.30, $E_C -$ 0.21 eV; 8.73×10^{11}, 6.41×10^{11} eV^{-1} cm^{-2} and 5.8×10^{-23}, 8.11×10^{-23} cm^2 for the NMOS and PMOS devices, respectively. A low value of interface state density in both P- and N-MOS structures makes it a suitable alternate dielectric layer for CMOS applications. Very low value of capture cross section for both the carriers due to their amphoteric nature indicates that the traps are not aggressive recombination centers and possibly can not contribute to the device operation to a large extent. Hence, a simple and an in-expensive process of combined sol – gel spin – coating method might be a good replacement for the expensive high vacuum deposition techniques in the development of high-κ dielectrics based on MOS structures and the DLTS study can provide a better understanding of TiO_2/Si interfaces.

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[51] See supplementary material at http://dx.doi.org/10.1063/1.4935749 for the TiO_2 thin films fabrication, estimation of thickness and refractive index as a function of wavelength [Fig. S1 – S4].

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