Active Power Decoupling with Reduced Converter Stress for Single-Phase Power Conversion and Interfacing

Sujata Bhowmick and L. Umanand
Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore-560012

***Abstract*—Single-phase DC/AC power electronic converters suffer from pulsating power at double the line frequency. The commonest practice to handle the issue is to provide a huge electrolytic capacitor for smoothening out the ripple. But, the electrolytic capacitors having short end of lifetimes limit the overall lifetime of the converter. Another way of handling the ripple power is by active power decoupling (APD) using the storage devices and a set of semiconductor switches. Here, a novel topology has been proposed implementing APD. The topology claims the benefit of 1) reduced stress on converter switches 2) using smaller capacitance value thus alleviating use of electrolytic capacitor in turn improving the lifetime of the converter. The circuit consists of a third leg, a storage capacitor and a storage inductor. The analysis and the simulation results are shown to prove the effectiveness of the topology.**

***Index Terms*—single-phase, double frequency ripple, Active power decoupling, reduced stress, reliability**

I. Introduction

THE single-phase power electronic converters interfacing a DC storage system or a DC source has the inherent problem of double frequency power ripple. The effect of the same is experienced at the DC bus in terms of double frequency current ripple, leading to double frequency DC bus voltage ripple in standard single phase DC-AC Voltage Source Inverter (VSI). This results in under-utilisation of renewable energy sources (e.g. PV), potential life-shortening for the batteries where the ripple current flows into the battery thus heating up the battery. Further this also leads to grid current distortion. The most common practice to counteract the above scenario is to use huge DC bus capacitor to supply the ripple current component. This passive strategy calls for electrolytic capacitors (because of their high capacitance value). But, the electrolytic capacitors have short end of lifetimes which reduces the overall system reliability[1].

In recent times, it has been reported to address the ripple power issue in active rather than in passive manner. The idea being, compensation of the ripple power using a set of switches to control the state of the storage element. The main motivations for this approach have been,

- Increasing the life of converter by eliminating the weakest point i.e., the electrolytic capacitor from the system
- Using the storage devices more effectively

The approaches vary in the placement of the ripple power buffer circuitry. The main trends being,

- Active ripple power compensation in DC side [2] [3] [4]
- Providing a dedicated energy port to handle ripple power in high frequency(HF) isolated configurations [5] [6] [7] [8]
- Compensating the ripple power in AC side of the converter [9] [10] [11]

Among the above approaches, DC side buffer has been popular because of their reduced switch count, eventhough, controller bandwidth needs to be very high to track the high frequency harmonic rich current. This calls for high switching frequency of the converter, keeping their application limited to low power level.

In the second approach, the buffer circuitry interfaces the line frequency AC side, via a HF transformer either with or without a tertiary winding. Although, control variable is of line frequency, this approach demands for increase in the number of auxilliary switches in large proportion.

Interestingly, AC side compensation topologies have been reported with only a set of two auxilliary switches and a storage device. By compensating the ripple power in the AC stage, down the line stages process only the average power, hence increasing the overall efficiency of the converter.

With advanced control, the auxilliary switches have been reported to add less than 50% kVA rating to the existing H-bridge [12]. The above statement is true for three conditions of load, viz. rectifier (unity power factor (UPF)), inverter (UPF) and STATCOM (Zero power factor (ZPF)) with current lagging voltage. The topology can handle the remaining loading condition (ZPF with current leading voltage) but at the cost of increased current stress on the switches.

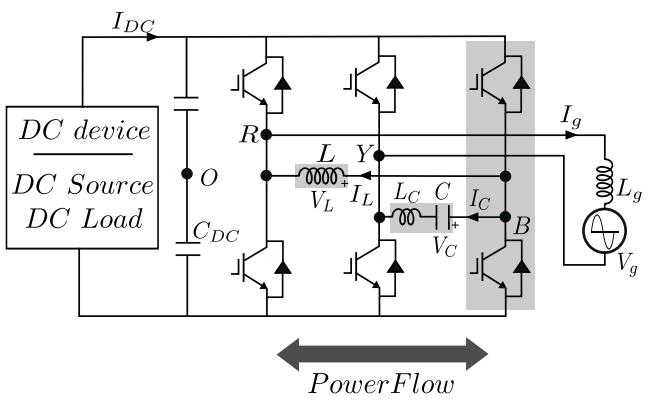


Fig. 1. Circuit diagram of the proposed converter

In this paper, a novel topology is proposed which can handle all loading conditions without further increase in converter kVA rating. In addition, 30% current reduction is achieved in H-bridge legs for UPF operation, leading to reduction in current stress of the switches improving the overall reliability of the system. The above assertions are theoretically shown using the power balance equation and phasor diagrams. Simulation results are presented in further support of the analysis.

The content of the paper has been arranged in the following manner. In section II, the proposed topology is presented along with its operating principle; section III is presented to compare the proposed topology with the existing one; in section IV the simulation results are presented and finally the conclusion has been drawn in section V.

II. Proposed topology

In standard grid connected DC/AC H-bridge configuration, V_g, I_g and L_g denotes grid voltage, grid current and filter inductor respectively. C_{DC}, the DC bus capacitor, is used to filter out the harmonic component of the DC bus current to make I_{DC} fairly constant. O, the midpoint of the DC bus serves the purpose of a virtual ground for the analysis.

The proposed topology is shown in fig. 1. The circuit consists of an AC capacitor (C) with a filter inductor (L_C), a storage inductor (L) and a pair of switches (shown in shaded area) in addition to standard H-bridge configuration. The operation of the circuit is explained below.

The pole voltage of leg R and Y wrt DC bus mid point O are V_{RO} and V_{YO} respectively. The fundamental component of these two voltages are controlled to be equal and opposite. The difference between the two constitutes the grid voltage V_g. The grid current I_g lags V_g by PF angle α. The phase (δ) and magnitude of fundamental component of third leg (B) pole voltage V_{BO} is controlled, which in effect controls capacitor voltage V_C and inductor voltage V_L in order to achieve active power decoupling (APD). The relevant voltages and current are shown in phasor diagram fig. 2.

The instantaneous power drawn from the DC source is constant with APD (neglecting switching harmonics).

Applying power balance:

$$p_C + p_L + p_g = V_{DC} * I_{DC} = constant$$

where, $p_C,\ p_L,\ p_g$ are the instantaneous power of capacitor, inductor and the grid branches (please refer to Appendix for $p_C,\ p_L$ and p_g expression derivation).

In the following discussion, the instantaneous power expressions for grid, inductor and capacitor are derived for an arbitrary PF angle α. Power balance equation is used to obtain the control condition of the APD scheme.

In order to simplify the analysis, the effect of filter inductor L_g and L_C are neglected. The assumption is justified as, their values are generally less than 0.05 per unit (p.u.).

As shown in phasor diagram (fig. 2) V_C and V_L leads V_g by angle θ and ϕ respectively.

$$v_g = V_{gm} \sin \omega t \tag{1}$$

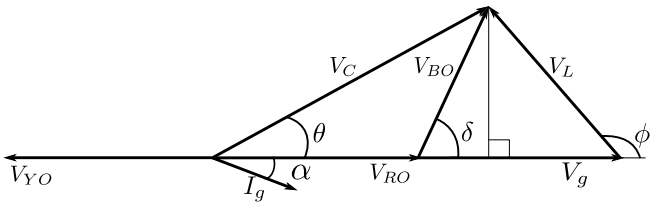


Fig. 2. Phasor diagram for an arbitrary power factor (neglecting drop across L_C and L_g)

$$i_g = I_{gm} \sin(\omega t - \alpha) \tag{2}$$

$$v_C = V_{Cm} \sin(\omega t + \theta) \tag{3}$$

$$i_C = I_{Cm} \sin(\omega t + \theta + \frac{\pi}{2}) \tag{4}$$

$$v_L = V_{Lm} \sin(\omega t + \phi) \tag{5}$$

$$i_L = I_{Lm} \sin(\omega t + \phi - \frac{\pi}{2}) \tag{6}$$

Instantaneous power pumped into AC sink,

$$p_g = v_g * i_g$$

Substituting expression of v_g and i_g from equation (1) and (2), the above equation reduces to

$$p_g = V_g I_g[\cos\alpha - \cos(2\omega t - \alpha)] \tag{7}$$

Power stored in capacitor C,

$$p_C = v_C * i_C \tag{8}$$

Using equation (3) and (4) in equation (8),

$$p_C = \frac{V_C^2}{|X_C|}[\sin 2\omega t(1 - 2\sin^2\theta) + 2\cos 2\omega t(\sin\theta\cos\theta)] \tag{9}$$

Similarly, power stored in inductor,

$$p_L = v_L * i_L \tag{10}$$

Substituting (5) and (6) in (10),

$$p_L = -\frac{V_L^2}{|X_L|}[\sin 2\omega t(1 - 2\sin^2\phi) + 2\cos 2\omega t(\sin\phi\cos\phi)] \tag{11}$$

From fig. 2,

$$V_{BO}\sin\delta = V_C\sin\theta = -V_L\sin\phi \tag{12}$$

Therefore, using equation (9), (11) and (12), the expression for total power stored together in inductor and capacitor,

$$\begin{aligned} p_C + p_L \ = \ & \frac{1}{|X_C|}[\sin 2\omega t(V_C^2 - 2V_{BO}^2\sin^2\delta) \\ & + 2\cos 2\omega t(V_{BO}\sin\delta V_C\cos\theta)] \\ & - \frac{1}{|X_L|}[\sin 2\omega t(V_L^2 - 2V_{BO}^2\sin^2\delta) \\ & - 2\cos 2\omega t(V_{BO}\sin\delta V_L\cos\phi)] \end{aligned}$$

If it is made that, $|X_C| = |X_L|$, the equation above reduces to,

$$= \frac{1}{|X_L|}[\sin 2\omega t(V_c^2 - V_L^2) + 2\cos 2\omega t V_{BO}\sin\delta(V_c\cos\theta - V_L\cos\phi)]$$

$$= \frac{1}{|X_L|}[\sin 2\omega t(V_c^2\cos^2\theta - V_L^2\cos^2\phi) + 2\cos 2\omega t V_{BO}\sin\delta (V_C\cos\theta - V_L\cos\phi)]$$

$$= \frac{1}{|X_L|}(V_C\cos\theta - V_L\cos\phi)[\sin 2\omega t(V_C\cos\theta + V_L\cos\phi) + 2\cos 2\omega t V_{BO}\sin\delta] \quad (13)$$

From figure (2), $(V_C\cos\theta - V_L\cos\phi) = 2V_{RO}$;

$$V_L\cos\phi = -(V_{RO} - V_{BO}\cos\delta);$$

$$V_C\cos\theta = V_{BO}\cos\delta + V_{RO};$$

Therefore, $(V_C\cos\theta + V_L\cos\phi) = 2V_{BO}\cos\delta$;

Substituting these relations into the power equation (13),

$$\begin{aligned} p_C + p_L &= \frac{2V_{RO}}{|X_L|}[\sin 2\omega t(2V_{BO}\cos\delta) + \cos 2\omega t(2V_{BO}\sin\delta)] \\ &= \frac{4V_{RO}V_{BO}}{|X_L|}\sin(2\omega t + \delta) \\ &= \frac{4V_{RO}V_{BO}}{|X_L|}\cos(2\omega t + \delta - \frac{\pi}{2}) \\ &= \frac{V_g(2V_{BO})}{|X_L|}\cos(2\omega t - (\frac{\pi}{2} - \delta)) \quad (14) \end{aligned}$$

Thus, in order to arrive at APD control condition, comparing (7) and (14) one can conclude,

1. $|V_{BO}| = 0.5I_g(in\ p.u.\ sense)\ when\ |X_L| = 1p.u.$ (15)

2. $\delta = \frac{\pi}{2} - \alpha$ (16)

These relationships guide one to select the reference voltage vectors at different loading as well as PF.

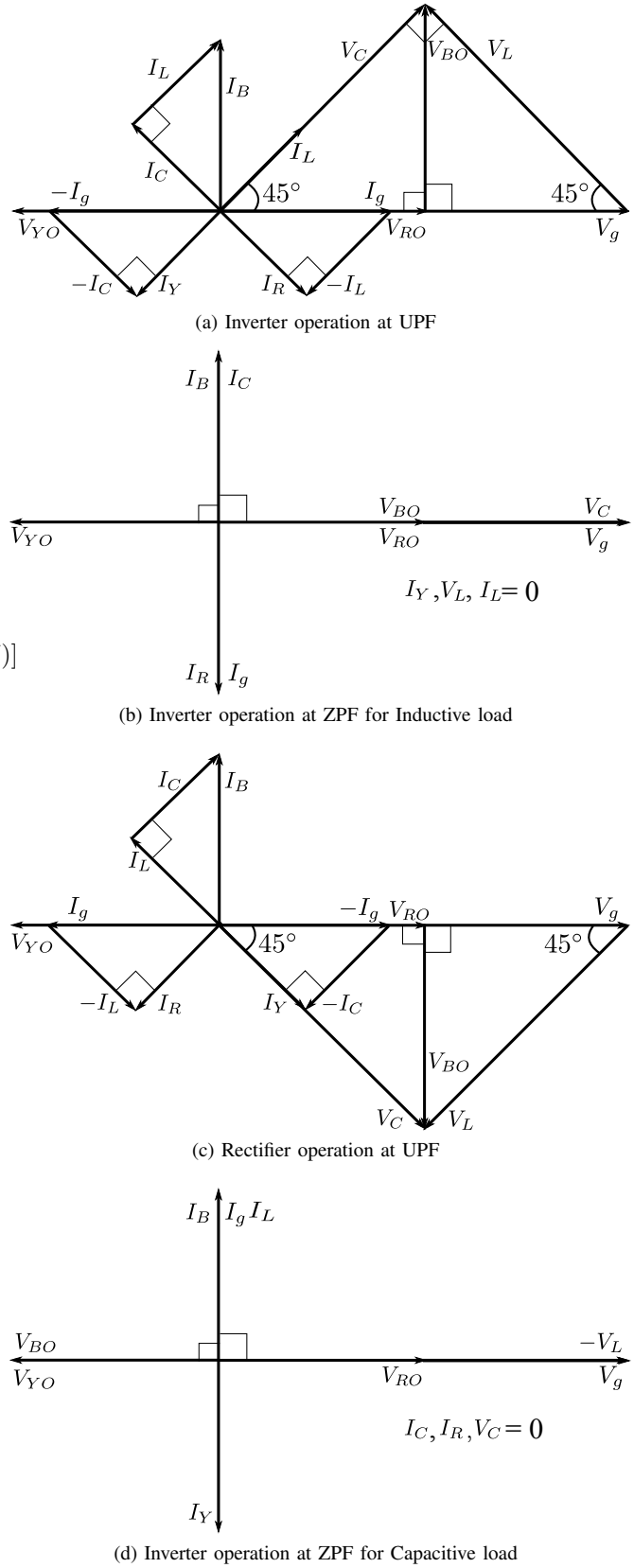
Using the above solution of V_{BO}, leg currents are obtained from the phasors for different loading conditions. The phasors are drawn with the current being pumped to the AC sink, which is the positive active power flow direction from DC to AC side.

The loading conditions considered are, full load for,

- Inverter UPF ($\alpha = 0$)
- Inverter ZPF for Inductive load ($\alpha = \pi/2$)
- Rectifier UPF ($\alpha = \pi$)
- Inverter ZPF for capacitive load ($\alpha = 3\pi/2$)

A. Individual case Analysis

For the rest of the analysis $|X_L|$ is considered as 1p.u., which is a design criteria.



(a) Inverter operation at UPF

(b) Inverter operation at ZPF for Inductive load

(c) Rectifier operation at UPF

(d) Inverter operation at ZPF for Capacitive load

Fig. 3. Phasor diagram at Full load condition

1) Inverter UPF operation at Full load: From equation (15) and (16),

$$|V_{BO}| = 0.5\ p.u.$$
$$\delta = \pi/2 - \alpha = \pi/2$$

Therefore, from fig. 3a,

$$\begin{aligned} V_C &= (\sqrt{2} * 0.5)\angle\frac{\pi}{4}\ p.u. \\ &= 0.707\angle\frac{\pi}{4}\ p.u. \\ V_L &= 0.707\angle\frac{3\pi}{4}\ p.u. \end{aligned}$$

Thus, with the assumption, $|X_L| = |X_C| = 1\ p.u.$,

$$\begin{aligned} I_C &= 0.707\angle\frac{3\pi}{4}\ p.u. \\ I_L &= 0.707\angle\frac{\pi}{4}\ p.u. \end{aligned}$$

Which gives the leg currents,

$$\begin{aligned} I_R &= I_g - I_L = 0.707\angle -\frac{\pi}{4}\ p.u. \\ I_Y &= -(I_g + I_C) = 0.707\angle -\frac{3\pi}{4}\ p.u. \\ I_B &= I_C + I_L = 1\angle\frac{\pi}{2}\ p.u. \end{aligned}$$

2) Inverter ZPF for Inductive load at Full load: From equation (15) and (16),

$$|V_{BO}| = 0.5\ p.u.$$
$$\delta = \pi/2 - \alpha = 0$$

Therefore, from fig. 3b,

$$\begin{aligned} V_C &= 1\angle 0\ p.u. \\ V_L &= 0\ p.u. \end{aligned}$$

Thus, with the assumption, $|X_L| = |X_C| = 1\ p.u.$,

$$\begin{aligned} I_C &= 1\angle\frac{\pi}{2}\ p.u. \\ I_L &= 0\ p.u. \end{aligned}$$

Resulting in the leg currents,

$$\begin{aligned} I_R &= I_g - I_L = 1\angle -\frac{\pi}{2}\ p.u. \\ I_Y &= -(I_g + I_C) = 0\ p.u. \\ I_B &= I_C + I_L = 1\angle\frac{\pi}{2}\ p.u. \end{aligned}$$

3) Inverter UPF operation at Full load: From equation (15) and (16),

$$|V_{BO}| = 0.5\ p.u.$$
$$\delta = \pi/2 - \alpha = -\pi/2$$

Therefore, with reference to fig. 3c, following the same procedure as in $Case\ 1$, leg currents are,

$$\begin{aligned} I_R &= I_g - I_L = 0.707\angle -\frac{3\pi}{4}\ p.u. \\ I_Y &= -(I_g + I_C) = 0.707\angle -\frac{\pi}{4}\ p.u. \\ I_B &= I_C + I_L = 1\angle\frac{\pi}{2}\ p.u. \end{aligned}$$

4) Inverter ZPF for Capacitive load at Full load: From equation (15) and (16),

$$|V_{BO}| = 0.5\ p.u.$$
$$\delta = \pi/2 - \alpha = 0$$

Therefore, from fig. 3d,

$$\begin{aligned} V_C &= 0\ p.u. \\ V_L &= 1\angle\pi\ p.u. \end{aligned}$$

Following the same process and with the same assumption as in $Case\ 2$, Resulting leg currents,

$$\begin{aligned} I_R &= I_g - I_L = 0\ p.u. \\ I_Y &= -(I_g + I_C) = 1\angle -\frac{\pi}{2}\ p.u. \\ I_B &= I_C + I_L = 1\angle\frac{\pi}{2}\ p.u. \end{aligned}$$

The above results are condensed in table I for the ease of comparison with the existing topology [12].

III. Comparison With Existing Topology

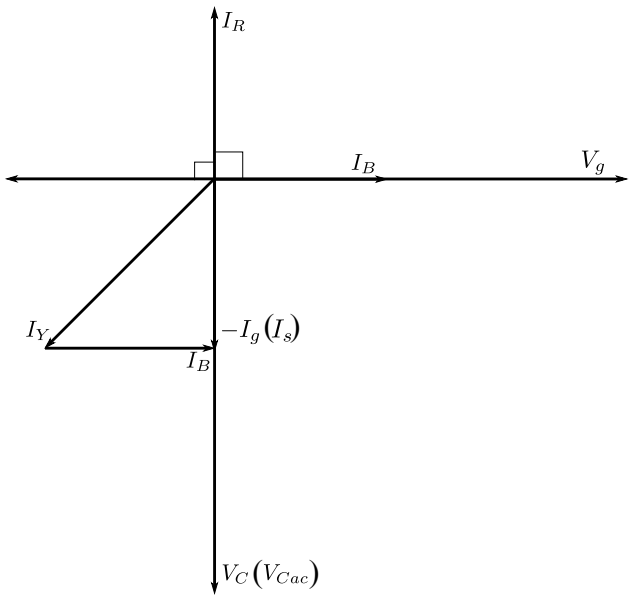


Fig. 4. Phasor diagram of STATCOM operation, $I_s(-I_g)$ lagging V_g by $\pi/2$ for topology [12]

With reference to the phasor diagram fig. 4 and the phasor diagrams presented in [12], the results of the existing topology are included in table I.

From table I, it can be seen that, the proposed topology has identical 30% current reduction in both the legs, which means lesser loss and temperature rise of the semiconductor switches. This reduced stress results in higher reliability of the switches. The improvement is even more for $\phi = -\pi/2$, where leg Y is 44% overstressed for the existing topology in [12].

The parameter K_{SF}, Stress Factor, has been defined as the ratio of 3 legged converter rating (APD compensated) and 3 legged converter rating (3^{rd} leg identical to uncompensated H bridge). From table I, it can be seen that, K_{SF} reduces by 15%

TABLE I
CONVERTER INSTALLED CAPACITY COMPARISON

PF condition		With only C storage [12]				With L & C storage			
		Leg Currents (in p.u.)			$K_{SF}{}^a$	Leg Currents (in p.u.)			$K_{SF}{}^a$
ϕ	α	$\|I_R\|$	$\|I_Y\|$	$\|I_B\|$		$\|I_R\|$	$\|I_Y\|$	$\|I_B\|$	
0	π	1	0.77	1	**0.92**	0.71	0.71	1	**0.8**
$\pi/2$	$\pi/2$	1	0	1	0.67	1	0	1	0.67
π	0	1	0.77	1	**0.92**	0.71	0.71	1	**0.8**
-$\pi/2$	-$\pi/2$	1	1.44	1	**1.13**	0	1	1	**0.67**

[a]Stress Factor = 3 legged converter rating (APD compensated) / 3 legged converter rating with 3^{rd} leg rated identical as H bridge(uncompensated)

under UPF and 70% for capacitive load when compared to [12] which indicates reduced stress on the converter switches.

It should be noted that in case of inductor being the only storage element instead of capacitor as in [11], the results will remain same under UPF operation, whereas, 70% reduction will be observed for inductive load instead of capacitive load.

IV. SIMULATION RESULTS

For verification of the proposed topology and effectiveness of the decoupling method, a system rated for 230V, 5A has been modelled and simulated. The system parameters are listed in table II.

TABLE II
SYSTEM PARAMETERS

AC Voltage, V_g	230V (50 Hz)
AC Current, I_g	5A (50 Hz)
DC bus Voltage, V_{DC}	400V
Switching Frequency, f_{sw}	20kHz
Filter Capacitor, C_{DC}	100μF
Filter Inductor, L_g	7.3mH
Storage Capacitor, C	68μF
Storage Inductor, L	146mH
Filter Inductor, L_C	2.2mH

The simulation results for inverter operating at UPF is presented in fig. 5, 6 and 7. From fig. 5 it can be observed that, the DC bus current ripple reduces to 0.2A with APD compensation compared to 5.8A under uncompensated scenario thus validating the effectiveness of the scheme. Figure 6 shows that under UPF operation, both capacitor and inductor shares the energy equally and the currents through them are 70% of the grid current. In fig. 7 leg currents of the converter are shown from which the current reduction in two legs to 70% of the rated current (7A peak) are clearly visible.

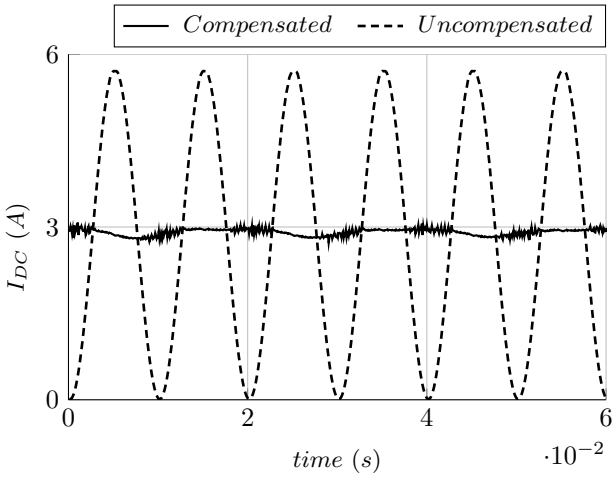


Fig. 5. DC bus current with and without APD compensation at steady state

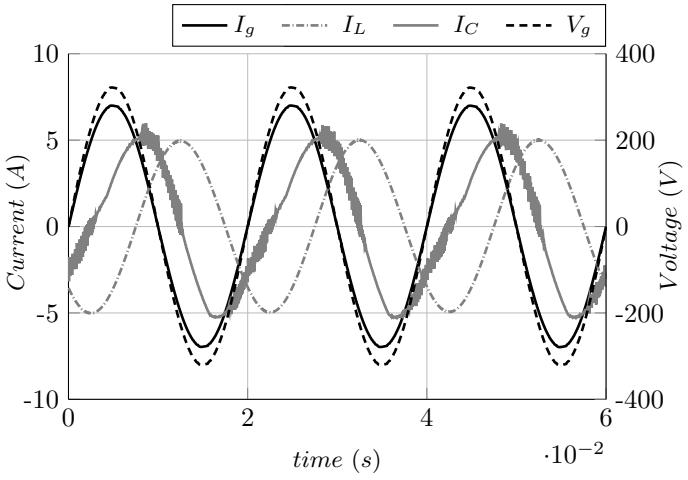


Fig. 6. Branch currents and grid voltage at steady state

V. CONCLUSION

In this paper, a novel topology is proposed to handle the single phase power ripple. Analysis of the topology is performed using power balance equation and the phasor diagrams. 30% reduction in current rating of the H-bridge inverter is achieved for UPF. And also the topology can handle all loading conditions with the maximum of 70% reduced stress compared to the existing topologies. The simulation results are presented for the validation of the same.

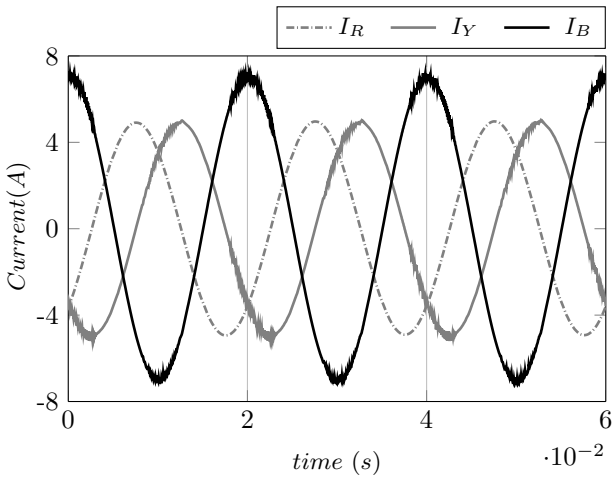


Fig. 7. Leg currents with APD compensation at steady state

APPENDIX
STEADY STATE INSTANTANEOUS POWER EQUATIONS DERIVATION

GRID POWER DERIVATION

Instantaneous power pumped into AC sink,
$p_g = v_g * i_g$
Substituting expression of v_g and i_g from equation (1) and (2), the above equation reduces to

$$\begin{aligned} &= \frac{V_{gm}I_{gm}}{2}[\cos\alpha - \cos(2\omega t - \alpha)] \\ &= V_g I_g[\cos\alpha - \cos(2\omega t - \alpha)] \end{aligned} \tag{17}$$

CAPACITOR POWER DERIVATION

Power stored in capacitor C,

$$p_C = v_C * i_C \tag{18}$$

On simplifying equation (18), using equation (3) and (4),

$$\begin{aligned} p_C &= V_{Cm}\sin(\omega t + \theta) * I_{Cm}\sin(\omega t + \theta + \frac{\pi}{2}) \\ &= -V_C I_C \cos(2\omega t + 2\theta + \frac{\pi}{2}) \\ &= V_C I_C \sin(2\omega t + 2\theta) \\ &= \frac{V_C^2}{|X_C|}(\sin 2\omega t\cos 2\theta + \cos 2\omega t \sin 2\theta) \\ &= \frac{1}{|X_C|}[\sin 2\omega t(V_C^2 - 2V_C^2\sin^2\theta) \\ &\quad + 2\cos 2\omega t(V_C\sin\theta V_C\cos\theta)] \end{aligned} \tag{19}$$

INDUCTOR POWER DERIVATION

Similarly, for inductor L, power stored is,

$$p_L = v_L * i_L \tag{20}$$

Solving equation (20) using equation (5) and (6), results in,

$$\begin{aligned} p_L &= V_{Lm}\sin(\omega t + \phi) * I_{Lm}\sin(\omega t + \phi - \frac{\pi}{2}) \\ &= V_L I_L[-\cos(2\omega t + 2\phi - \frac{\pi}{2})] \\ &= -\frac{V_L^2}{|X_L|}\sin(2\omega t + 2\phi) \\ &= -\frac{V_L^2}{|X_L|}(\sin 2\omega t\cos 2\phi + \cos 2\omega t\sin 2\phi) \\ &= -\frac{1}{|X_L|}[\sin 2\omega t(V_L^2 - 2V_L^2\sin^2\phi) \\ &\quad + 2\cos 2\omega t(V_L\sin\phi V_L\cos\phi)] \end{aligned} \tag{21}$$

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