

High Performance Modulation of High-Frequency AC Link Inverter

Abhijit Kulkarni and Vinod John
Department of Electrical Engineering, IISc Bangalore.
(abhijitk@ee.iisc.ernet.in, vjohn@ee.iisc.ernet.in)

Abstract—Inverters with high voltage conversion ratio are used in systems with sources such as batteries, photovoltaic (PV) modules or fuel cells. Transformers are often used in such inverters to provide the required voltage conversion ratio and isolation. In this paper, a compact high-frequency (HF) transformer interfaced AC link inverter with lossless snubber is discussed. A high performance synchronized modulation scheme is proposed for this inverter. This modulation addresses the issue of over-voltage spikes due to transformer leakage inductance and it is shown that the circuit can operate safely even when the turn-on delay, such as dead-time, is not used in the HF rectifier section. The problem of spurious turn-on in the HF inverter switches is also mitigated by the proposed modulation method. The circuit performance is validated experimentally with a 900W prototype inverter.

Index Terms—Photovoltaic systems, batteries, inverters, pulse width modulation.

I. INTRODUCTION

Inverters at a power level of the order of $1kW$ using batteries, photovoltaic modules (PV) or fuel cells normally have low input voltage, typically less than 100V. High voltage conversion ratio is necessary to convert the input dc to line voltage ac which is typically $230V_{rms}$, $50Hz$. To achieve the required voltage conversion ratio and to provide isolation, the inverter circuit topologies for such systems often use transformers [1]–[7].

High-frequency (HF) transformer interfaced AC link inverter is preferred in many applications due to compact size of the transformer. In this paper, HF AC link inverter topology shown in Fig. 1 is discussed. This topology has an HF inverter which converts the input dc to HF ac. The HF transformer steps up the voltage which is rectified by a high-frequency active rectifier. This topology needs a snubber to avoid the over-voltage spikes due to commutation with the transformer leakage inductance in the circuit [4]. Output of the rectifier contains a lossless snubber for efficiency improvement in place of the passive RC snubbers which are lossy [8]. The output stage consists of an H-bridge single-phase inverter. The output is shown to be grid connected in Fig. 1. It can also be used in stand-alone applications feeding local load.

The inverter topology must be modulated such that the over-voltage spikes are completely suppressed. This is achieved by the proposed high performance synchronized modulation

method. The proposed modulation results in ZVS turn-on of the HF inverter and rectifier switches. The snubber switch has ZVS turn-on and turn-off resulting in practically zero switching losses. This improves the overall system efficiency. The modulation also results in better dc voltage utilization compared to the quasi-square wave modulation. The quasi-square wave modulation intentionally introduces zero portions in the link voltage, hence reducing the average of the rectified AC link voltage.

Traditionally the switches of HF rectifier are provided with a turn-on delay, similar to the dead-time provided in an inverter [9]. It is shown in this paper, that such a turn-on delay along with the reverse recovery of the diodes can cause spurious turn-on of the devices in the HF inverter. This is an undesirable effect. The proposed modulation mitigates these spurious pulses, hence increasing the system reliability. The proposed modulation of the HF AC link inverter has been validated experimentally on a laboratory developed prototype.

This paper is organized as follows. Section II discusses the ideal operation of the inverter topology with the proposed modulation. The practical operation of the inverter and the problems of spurious turn-on of HF inverter devices due to the turn-on delay time (dead-time) is detailed in Section III. The effect of elimination of turn-on delay time in the HF rectifier to address the spurious turn-on problem is discussed in Section IV. The experimental results validating the proposed modulation on laboratory prototype are included in Section V. Conclusions are provided in Section VI.

II. IDEAL MODES OF OPERATION OF THE HF TRANSFORMER INTERFACED INVERTER

All the semiconductor devices in the inverter topology are assumed to be ideal. Thus the complementary devices are considered to be switched without any turn-on delay time. The proposed modulation for the ideal inverter includes the following synchronized switching.

- 1) The HF inverter and rectifier devices are switched in square wave mode in synchronism.
- 2) The output inverter is modulated using the conventional sine-triangle pulse width modulation (PWM) scheme.
- 3) The snubber device S is turned on during the active state (AS) of the output inverter. That is, whenever the diagonal switches of the output inverter are ON, S will be turned on. Thus, the switching frequency of S will be twice that of output inverter.

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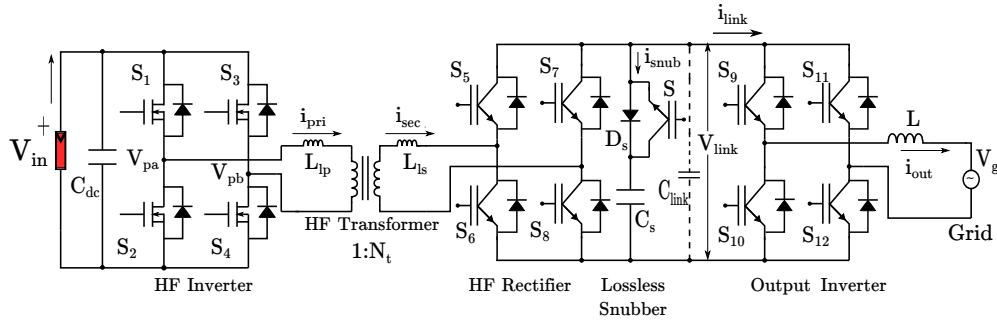


Fig. 1: HF transformer interfaced AC link inverter with a lossless snubber.

The modulation technique indicated in the three steps above, requires synchronization with appropriate phase shift of the carriers of HF inverter/rectifier and output inverter. The carriers used for the HF inverter, rectifier and output inverter are shown in Fig. 2(a) and (b). The time-relationship between output AS, zero-state (ZS) with link current, transformer primary voltage and current is shown in in Fig. 2(c) and (d).

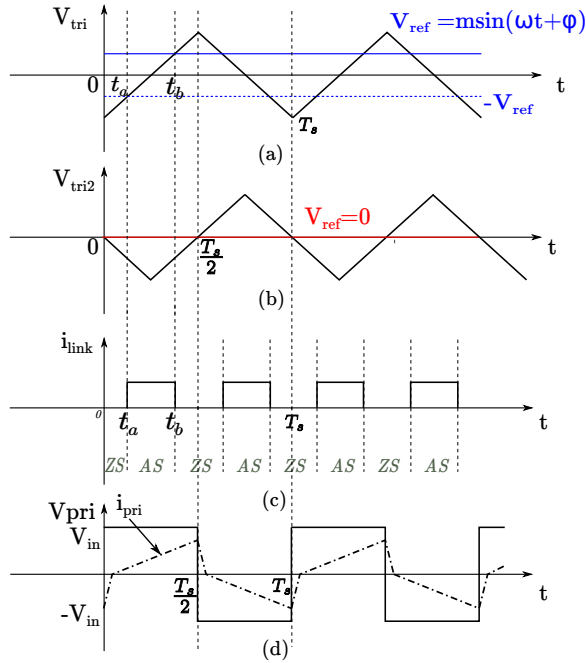


Fig. 2: (a) Triangular carrier for output inverter, (b) Triangular carrier for HF inverter and rectifier, (c) Link current indicating the active state and zero state and (d) Primary voltage and current.

The operation of the circuit, considering the different time intervals in a switching half-cycle, for the ideal condition is explained in the following subsections with reference to Fig. 2. The steps described in the following subsections will repeat in every switching half-cycle. The different modes of operation are described using equivalent circuit of the inverter topology. In the equivalent circuit, the devices $S_9, S_{10}, S_{11}, S_{12}$ and the output is replaced by a current source i_{link} . Each of the ideal modes of operation are detailed with an equivalent circuit which shows the conducting elements and gated-ON switches

in dark lines. The non-conducting elements and the gated-OFF switches are shown in light-shades.

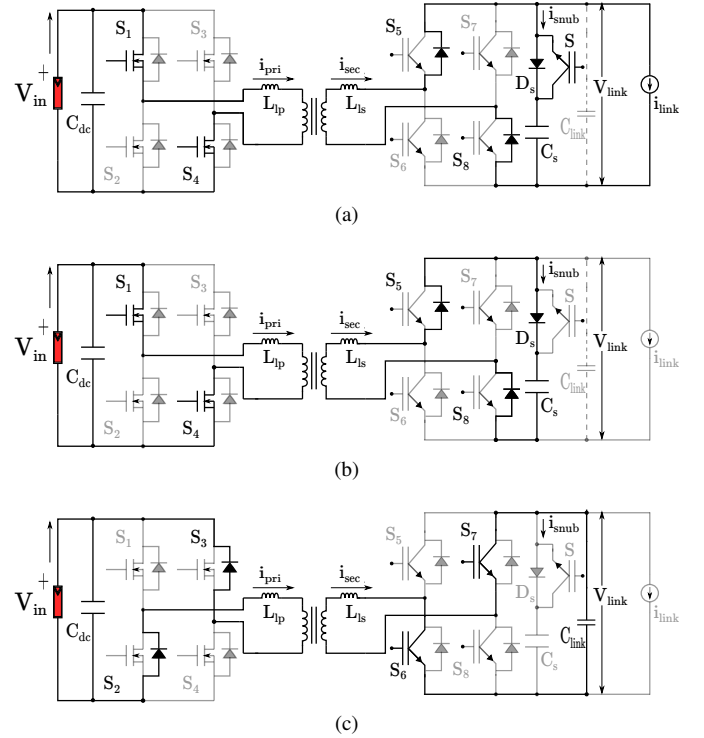


Fig. 3: Conducting devices for the ideal operation of the inverter in (a) Active state (AS), (b) Zero state (ZS), and (c) During primary voltage polarity reversal.

A. For $t_a \leq t < t_b$ (AS)

In AS, magnitude of i_{link} equals that of output current. S is turned on and hence C_s discharges through S to supply the necessary i_{link} . This prevents a large di/dt for transformer current. This means no voltage spike on the semiconductor devices. Primary and secondary currents (i_{pri}, i_{sec}) are building up in positive direction. The equivalent circuit in AS is shown in Fig. 3(a), indicating various conducting and non-conducting paths.

B. For $t_b \leq t < T_s/2$ (ZS)

i_{out} circulates between S_{12} and diode of S_{10} hence making $i_{link} = 0$. V_{pri} is positive and C_s is being charged via D_s .

Snubber switch S is off. The equivalent circuit during this mode is shown in Fig. 3(b).

C. For $t > T_s^+/2$ upto next AS

This interval includes the zerostate after the polarity reversal in the primary voltage, which occurs at $t = nT_s^+/2$ where n is any integer. i_{sec} starts flowing through S_6 , C_{stray} and S_7 since S_5 , S_8 are turned off, as shown in Fig. 3(c). The snubber switch and diode do not participate in the conduction of i_{sec} as S is off and D_s cannot conduct reverse current. Hence, i_{sec} discharges C_{stray} resetting the link voltage to zero. Secondary voltage V_{sec} also goes to zero during this reset.

Let I_{sec} be the value of secondary current when the link voltage reset happens. As the energy in leakage inductance is significantly higher than the energy stored in stray capacitance C_{link} , there will be practically negligible change in the value of I_{sec} . Thus the slope with which the link voltage gets reset is given by

$$\frac{dV_{link}}{dt} = \frac{I_{sec}}{C_{link}} \quad (1)$$

Then i_{sec} and i_{pri} , with value I_{sec} and nI_{sec} respectively, will decay to zero with the following slope.

$$\left| \frac{di}{dt} \right| = \frac{V_{in}}{L_{lk}} \quad (2)$$

In (2), L_{lk} is the effective leakage inductance referred to the primary side. The leakage inductances L_{lp} and L_{ls} in (3) below are indicated in Fig. 1. If $1 : N_t$ be the turns ratio of the transformer, then

$$L_{lk} = L_{lp} + \frac{L_{ls}}{N_t^2} \quad (3)$$

Note that the link voltage cannot become negative due to the presence of anti-parallel diodes in S_5 , S_6 , S_7 and S_8 . Thus, once reset to zero, link voltage stays at zero till the transformer current reaches zero. The resetting of link voltage and secondary voltage when the transformer primary voltage changes polarity is shown in Fig. 4. These waveforms are zoomed around the time instant when the polarity reversal of primary voltage happens. The gate to source voltages (V_{GS}) of primary side switches S_1 , S_2 and secondary side switches S_5 , S_6 are also shown in Fig. 4. The drain to source voltage (V_{DS}) of S_2 is also shown. The secondary voltage with its zero portion between t_1 and t_2 is shown. The polarity reversal in the primary voltage occurs at $t = t_1$ which is equal to nT_s/s as stated before. It can be seen that the falling and rising slopes of V_{sec} are unequal. This is because, the falling of V_{sec} occurs at a higher value of i_{sec} (or i_{pri}) while the rising occurs when the transformer currents are small. This is reflected in the link voltage also.

III. PRACTICAL OPERATION OF THE HF TRANSFORMER INTERFACED INVERTER

The proposed modulation is analysed for the practical implementation in this section. Normally, turn-on delay or dead-time is provided for all the complementary switching

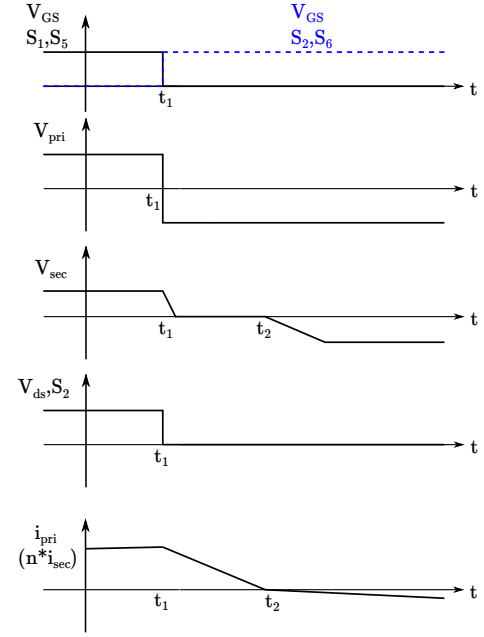


Fig. 4: Analytical waveforms for the ideal case zoomed around the instant of polarity reversal in the transformer primary voltage.

devices [9]. Fig. 5 shows the waveforms for the normal implementations with a turn-on delay time of t_d . This can be compared with the same set of waveforms in Fig. 4. The effect of diode reverse recovery is considered for the practical behaviour analysis. The various key waveforms are labelled in Fig. 5. The occurrence of false turn-on in primary voltage and V_{DS} of S_2 can be seen in the figure. This is explained in detail in the following subsections.

A. For $0 < t \leq t_1$

Switches S_1 , S_5 are on. V_{pri} , V_{sec} and i_{pri} , i_{sec} are positive. i_{pri} flows through S_1 and S_4 in the primary side and i_{sec} through the reverse diodes of S_5 and S_8 in the secondary side. This time interval corresponds to the zero state as just before the primary voltage polarity reversal, the output inverter is in zero state as can be seen from Fig. 2. Hence, the equivalent circuit for this time interval will be same as Fig. 3(b).

B. For $t_1 < t \leq t'_2$

This is an interval during dead-time. This circuit mode is absent in the ideal operation of the circuit. The equivalent circuit is shown in Fig. 6(a). S_1 , S_5 and their paired devices S_4 , S_8 are turned off. The i_{pri} starts to flow through the diodes of S_2 and $S_3 \Rightarrow$ hence reversing the primary voltage polarity. Secondary voltage continues to be positive because the diodes of S_5 and S_8 were conducting and the turn-off of their corresponding IGBTs will not have any impact. Due to the application of a large negative voltage across leakage inductance, the i_{pri} and i_{sec} start to fall linearly. The rate of fall is given by

$$\left| \frac{di}{dt} \right| = \frac{(V_{in} + |V_{link}|/N_t)}{L_{lk}} \quad (4)$$

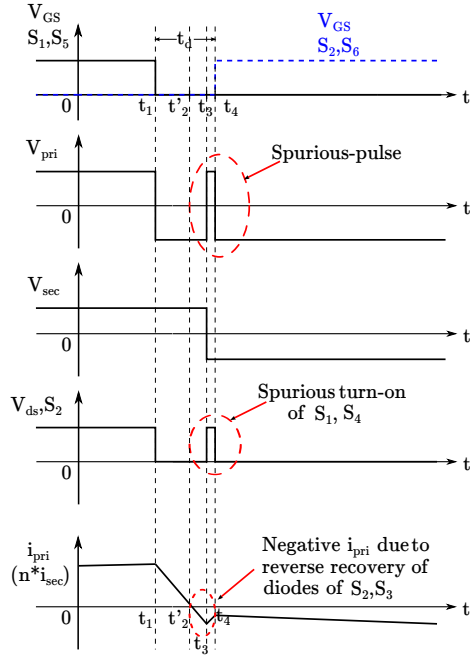


Fig. 5: Analytical waveforms zoomed around the instant of polarity reversal in the transformer primary voltage for the practical case with turn-on delay time t_d .

At time $t = t'_2$, the i_{pri} and i_{sec} go to zero.

C. For $t'_2 < t \leq t_3$

Ideally, the i_{pri} and i_{sec} should have remained clamped at zero. However, they go negative due to diode reverse recovery. At $t = t_3$, the diodes of S_2 , S_3 and S_5 , S_8 turnoff. The equivalent circuit for this case is same as Fig. 6(a) but with the polarities of i_{pri} and i_{sec} reversed. This is shown in Fig. 6(b) with the reversed current direction. Note that all the diodes, including the snubber diode D_s , are conducting negative current due to the diode reverse recovery.

D. For $t_3 < t \leq t_4$

The i_{pri} is now slightly negative but the dead-time duration is still persisting. As, i_{pri} cannot be interrupted suddenly, it flows through the diodes of S_1 , S_4 in the primary side. This gives rise to positive primary voltage spurious-pulse which is not expected from ideal waveforms. This spurious turn-on can be seen in the V_{DS} of S_2 and S_3 also.

The secondary current will be carried by the diodes of S_6 , S_7 resulting in V_{sec} becoming negative. Now the net positive voltage applied across leakage inductance, tries to increase the i_{pri} and i_{sec} . The equivalent circuit for this mode is shown in Fig. 6(c). It can be observed that the net voltage applied across the leakage inductance is positive now.

E. For $t > t_4$ till next AS

The dead-time ends at $t = t_4$. Thus the V_{pri} changes its polarity to the actual expected value and the currents will have the ideally expected slope. This is shown in the equivalent circuit in Fig. 6(d). The transformer voltages and currents are now negative.

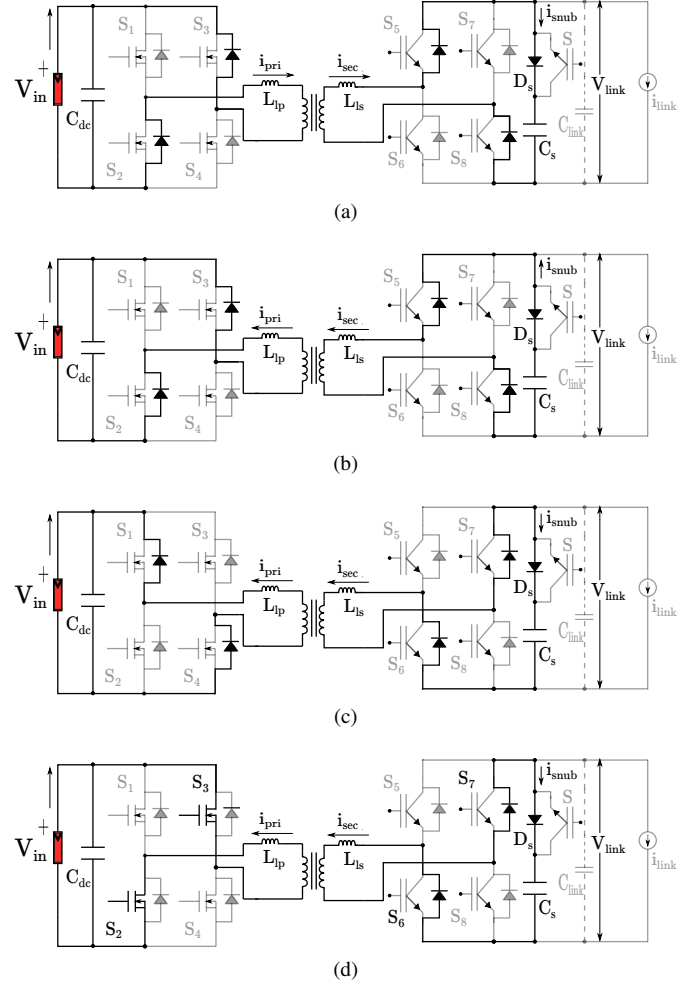


Fig. 6: Practical operation with dead-time. (a) During the dead-time with only diode conduction. (b) During dead-time with all the diodes conducting negative current due to reverse recovery. (c) During dead-time with spurious turn-on of diodes of S_1 and S_2 . (d) End of the dead-time with output inverter still in zero state.

The practical operation of the circuit can be explained similarly when the polarity reversal occurs from negative to positive in the primary voltage.

IV. ELIMINATION OF SPURIOUS TURN-ON IN THE HF-INVERTER SWITCHES

It was detailed in Section III that the turn-on delay time causes false turn-on pulses in the HF inverter switches. This problem can be solved if the turn-on delay time is eliminated in the HF rectifier switches namely S_5 , S_6 , S_7 and S_8 . It is also shown that this can be safely done without any shoot through issues in the circuit. The operation of the circuit when the turn-on delay time in HF rectifier is eliminated is explained as follows. The time intervals detailed below are with respect to Fig. 7.

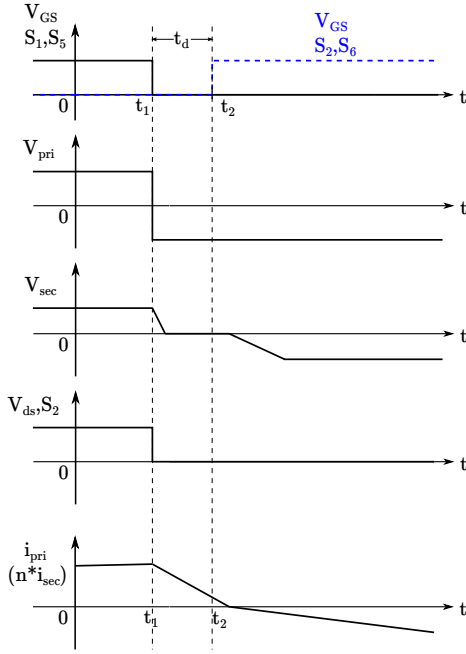


Fig. 7: Analytical waveforms zoomed around the instant of polarity reversal in the transformer primary voltage for the proposed modulation.

A. For $0 < t \leq t_1$

This is same as that for practical case explained in Section III. The equivalent circuit for this time interval will be same as Fig. 3(b).

B. For $t_1 < t \leq t_2$

This is an interval during dead-time in HF inverter. As in case of the operation in Section III, the primary side conduction is by the diodes of S_2 and S_3 . The input voltage polarity reverses just at the beginning of dead-time, as expected in ideal case.

The HF rectifier switches do not have a dead-time. Thus, S_5 , S_8 are turned off and their complementary devices S_6 and S_7 are turned-on simultaneously. There can be a switching overlap of the rectifier switches at this instant. The equivalent circuit during this time instant is shown in Fig. 8.

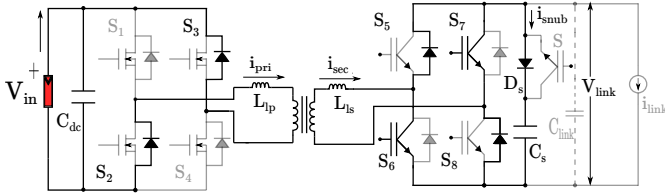


Fig. 8: The equivalent circuit with proposed modulation showing the commutation in the secondary side when the primary side switches have dead-time interval.

The diodes of S_5 and S_8 will turn-off completely during the dead-time period of the HF inverter, transferring the complete secondary current to S_6 and S_7 . The resulting current will discharge the link voltage to zero as it does not have a reverse-flow path due to D_s and the snubber IGBT S is OFF as the

commutation occurs in the ZS of the output inverter. The equivalent circuit for this time instant will be identical to Fig. 3(c).

The shorting of link voltage and application of negative primary voltage causes the transformer current to drop. The transformer currents start falling at a slope given in (2) which is the ideally expected value. The dead-time ends at $t = t_2$.

C. For $t > t_2$

The HF inverter switches S_2 and S_3 are turned on while their diodes are conducting. Hence it is a ZVS turn-on. The transformer currents continue to fall with the slope given in (2) and reach zero. Then the polarity of currents changes to negative and the diodes of S_6 and S_7 in HF rectifier begin to conduct.

The secondary current charges up the link voltage till it exceeds to forward bias the snubber diode. Then the link voltage equals the snubber capacitor voltage and the system continues in this state till the next active state begins. The equivalent circuit for this will be same as Fig. 6(d).

V. EXPERIMENTAL RESULTS

When there is turn-on delay present in both HF inverter and rectifier devices, there will be false turn-on as explained in Section III. This is shown in Fig. 9(a).

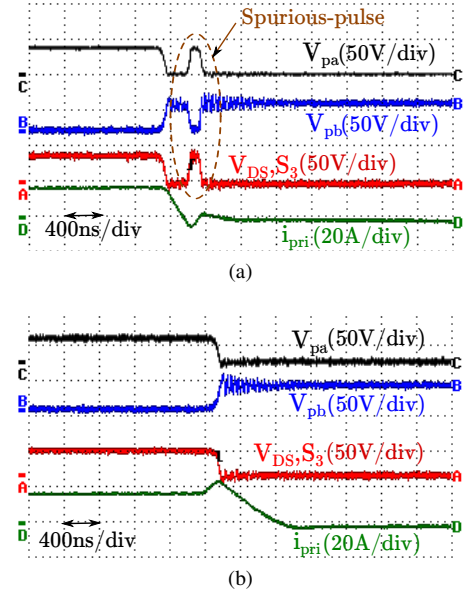


Fig. 9: (a) Spurious turn-on when turn-on delay is present in HF rectifier switches, (b) Improved performance with simultaneous switching in HF rectifier switches.

The voltages V_{pa} , V_{pb} are marked in Fig. 1 and their difference is the V_{pri} . The same set of waveforms are obtained with the proposed modulation in Fig. 9(b). Clearly, there is no spurious turn-on pulse with proposed modulation. The primary current is also shown in Fig. 9(a) and (b). Due to the link voltage reset, the di_{pri}/dt for the case with proposed modulation is lesser. This aids in the ZVS turn-on for the HF inverter switches.

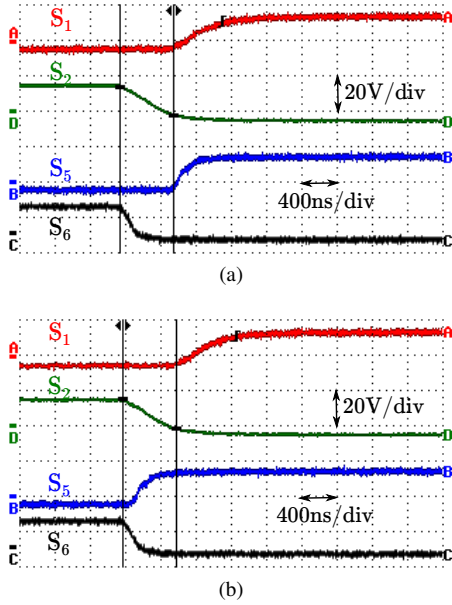


Fig. 10: V_{GS} signals for S_1 , S_2 , S_5 and S_6 – (a) With conventional turn-on delay, (b) Proposed simultaneous switching for HF rectifier switches (Shown for S_5 and S_6).

The gate-to-source voltages for S_1 , S_2 and S_5 , S_6 are shown in Fig. 10(a) and (b). It can be observed that in Fig. 10(a) there is a turn-on delay between both pairs of complementary devices which is as per the conventional implementation. In Fig. 10(b), the proposed simultaneous switching for HF rectifier switches S_5 and S_6 is shown.

The secondary voltage and current at a frequency of $20kHz$ are shown with the proposed modulation in Fig. 11(a). In Fig. 11(b), the output voltage and currents are shown. The system has been tested in stand-alone mode for upto $0.9kW$.

When the inverter was modulated with the traditional turn-on delay time in HF rectifier switches, the circuit behaviour was very noisy due to spurious pulses. It could be run without trip-signal from protection circuitry only upto an input voltage of $30V$ and a power level of $389W$. The losses were determined to be $57.8W$. At the same power level, with the proposed modulation, the losses were reduced to $52.4W$.

VI. CONCLUSION

In this paper, a high performance synchronized modulation is proposed for a HF AC link inverter with low input voltage for PV, battery or fuel cell input systems. This modulation addresses the over-voltage spikes in the circuit due to transformer leakage inductance. Practical operational issue of spurious turn-on is analyzed and solved by using the proposed simultaneous switching in the HF rectifier switches. It is shown that the turn-on delay time in HF rectifier section can be eliminated without causing any shoot-through problems. The HF inverter and rectifier switches can have soft switching with the proposed modulation. The performance of the circuit is validated experimentally with the proposed modulation.

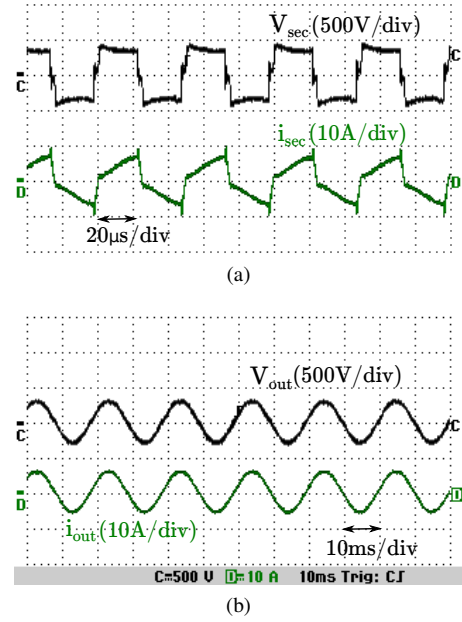


Fig. 11: (a) Transformer secondary voltage and current, (b) Output current and voltage at a power level of $0.9kW$.

REFERENCES

- [1] Z. Salam, S. Ayob, M. Ramli, and N. Azli, "An improved 'dc-dc type' high frequency transformer-link inverter by employing regenerative snubber circuit," in *Power Electronics and Drive Systems, 2007. PEDS '07. 7th International Conference on*, pp. 1081–1084, Nov 2007.
- [2] W. Li, L. Fan, Y. Zhao, X. He, D. Xu, and B. Wu, "High-step-up and high-efficiency fuel-cell power-generation system with active-clamp flyback-forward converter," *IEEE Transactions on Industrial Electronics*, vol. 59, pp. 599–610, Jan 2012.
- [3] A. Kulkarni and V. John, "Mitigation of lower order harmonics in a grid-connected single-phase pv inverter," *IEEE Transactions on Power Electronics*, vol. 28, pp. 5024–5037, Nov 2013.
- [4] T. Shimizu, K. Wada, and N. Nakamura, "Flyback-type single-phase utility interactive inverter with power pulsation decoupling on the dc input for an ac photovoltaic module system," *Power Electronics, IEEE Transactions on*, vol. 21, pp. 1264–1272, Sept 2006.
- [5] D. Martins and R. Demonti, "Grid connected pv system using two energy processing stages," in *Photovoltaic Specialists Conference, 2002. Conference Record of the Twenty-Ninth IEEE*, pp. 1649–1652, May 2002.
- [6] J. Mapurunga Caracas, G. De Carvalho Farias, L. Moreira Teixeira, and L. De Souza Ribeiro, "Implementation of a high-efficiency, high-lifetime, and low-cost converter for an autonomous photovoltaic water pumping system," *IEEE Transactions on Industry Applications*, vol. 50, pp. 631–641, Jan 2014.
- [7] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional dc – dc converter for high-frequency-link power-conversion system," *IEEE Transactions on Power Electronics*, vol. 29, pp. 4091–4106, Aug 2014.
- [8] D. De and V. Ramanarayanan, "A proportional + multiresonant controller for three-phase four-wire high-frequency link inverter," *IEEE Transactions on Power Electronics*, vol. 25, pp. 899–906, April 2010.
- [9] J.-W. Choi and S.-K. Sul, "Inverter output voltage synthesis using novel dead time compensation," *Power Electronics, IEEE Transactions on*, vol. 11, pp. 221–227, Mar 1996.