A Voltage Sensorless Control Method to Balance the Input Current of the Boost Rectifier Under Unbalanced Input Voltage Condition

Souvik Chattopadhyay, V. Ramanarayanan
Power Electronics Group
Department of Electrical Engineering,
Indian Institute of Science, Bangalore 560012, India
souvik@ee.iisc.ernet.in ,vram@ee.iisc.ernet.in

Abstract: **This paper proposes a control method that can balance the input current of the three phase, three wire, Boost rectifier under unbalanced input voltage condition. The control objective is to operate the rectifier in the high power factor mode under normal operating condition but to give overriding priority to the current balance function in case of unbalance in the input voltages. The inner loop implements resistor emulator type input current shaping strategy. The outer control loop performs magnitude scaling and phase shifting operations on current of one of the axis to make it balanced with respect to the current on the other axis . The coefficients of scaling and shifting functions are determined by two closed loop PI controllers. The control method is input voltage sensorless. In implementation Texas Instrument's DSP TMS320F240F is used as the digital controller.**

Index Terms - Power factor correction, High power factor rectifiers, Boost rectifier, Current-mode control, input voltage unbalance , input current unbalance.

I. INTRODUCTION

For three phase high power factor rectification Boost type PWM converters are very widely used. The control methods normally used for high power factor rectification are based either on regulation of active and reactive current components in the synchronously rotating reference frame or on direct control of active and reactive power components by hysteresis type of controllers . It is assumed in these methods that the input voltages both in terms of Thevenin equivalent voltages and output impedances are balanced . If the input voltages of such a three phase three wire system, as shown in Fig.1, are not balanced then that would cause abnormal even harmonics in the output dc voltage and odd harmonics in the input line currents [1].

A few methods have been proposed [2],[3],[4] to solve the problem of harmonics under unbalanced input voltage condition. In [2] the input voltages are decomposed into symmetrical components so that the detected negative sequence components can be added to the positive sequence control voltages for balancing the currents. This method performs well, however requires input voltage sensing and the current balance function is executed in the open loop. Another method proposed in [3] computes the second-order harmonics in the dc bus and generates three independent current references for cancellation of the even harmonics. The input currents need not be balanced in this method. It also needs input voltage sensing and the implementation is based on variable switching frequency operation. The method proposed in [4] is complex and achieves reduction of harmonics in the input current instead of elimination.

In this paper a closed loop input current balance scheme for three phase, three wire Boost rectifier is proposed. The control objective is to operate the rectifier in the high power factor mode under normal operating condition but to give overriding priority to the current balance function in case of unbalance in the input voltages. This control algorithm provides high performance with much simpler control structure than the methods mentioned above. It does not require sensing of input voltages and is based on constant switching frequency operation. The input impedances of the Boost rectifier need not be balanced as two independent closed loop PI controllers are used to balance the phase currents both in magnitude and in phase.

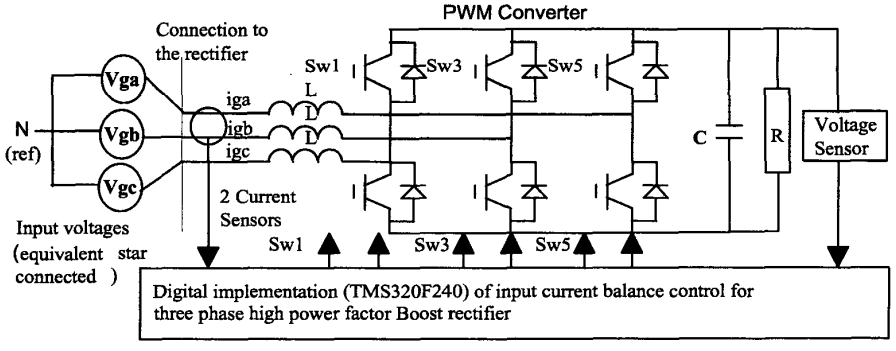


Fig. 1 Circuit schematic of the digitally controlled three phase high power factor Boost rectifier

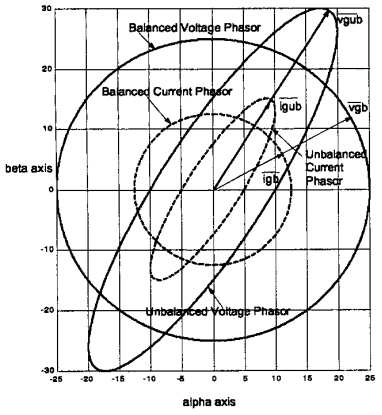


Fig.2 High power factor operation in α and β axis variables under balanced and unbalanced (chosen arbitrarily) input voltage conditions

II. HIGH POWER FACTOR AND VOLTAGE UNBALANCE

The control objective of a three phase, three wire, high power factor Boost rectifier, shown in Fig.1, is defined as

$$\overline{ig} = \frac{\overline{vg}}{Re} \tag{1}$$

where Re is the emulator resistance of the rectifier. Mathematically $\overline{vg}\,(= vga + jv_{g\beta})$, the phasor of the input phase voltages, and $\overline{ig}\,(= iga + ji_{g\beta})$, the phasor of the input phase currents, can be expressed as (2) and (3)

$$\overline{vg} = vga + v_{gb}e^{j\frac{2\pi}{3}} + vgce^{j\frac{4\pi}{3}} \tag{2}$$

$$\overline{ig} = \frac{2}{3}(iga + i_{gb}e^{j\frac{2\pi}{3}} + igce^{j\frac{4\pi}{3}}) \tag{3}$$

If we take components along α and β axes, which are stationary and orthogonal to each other, the control objective of (1) can be expressed in terms of two scalar equations (4) and (5). This is illustrated in Fig. 2.

$$iga = \frac{vga}{Re} \tag{4}$$

$$i_{g\beta} = \frac{v_{g\beta}}{Re} \tag{5}$$

If the phase voltages vga, v_{gb}, *and* vgc are balanced then their peak magnitudes are equal and they are phase shifted by 120°. For balanced phase voltages the components vga and $v_{g\beta}$, obtained from (2), are phase shifted by 90° and their peak magnitudes are also equal. The unbalance in the input voltages can either be in magnitude, or in phase, or in both magnitude and phase, and the summation of phase voltages may or may not be equal to zero. It can be seen from (4) and (5) that iga and $i_{g\beta}$ will not be balanced if the input voltages are unbalanced because the controller will make the input currents proportional to the input voltages in the (a,β) axis. It can also be noted that for a three phase three wire Boost rectifier the power factor correction objectives defined in (a,β) axes as in (4) and (5) can always be satisfied by the controller irrespective of the type of input voltage unbalance present in the system. This is because after the transformation of (2), the zero sequence component (v_{g0}), otherwise present in the phase voltages, gets canceled in v_{ga} and $v_{g\beta}$. However the input phase currents can be made proportional to the respective input phase voltages only if $vga + v_{gb} + vgc = 0$. This is because for a three phase three wire system $iga + i_{gb} + igc = 0$ is always true.

It is possible for a line current shaping controller to implement the input current balance function as its basic control objective under any kind of input voltage condition. However, then the controller will not be able to achieve high power factor operation in each phase, unless the unbalanced input voltages are balanced in phase i.e. phase shifted by 120°.

From the discussion above we can conclude the following

(1) We can always achieve unity power factor operation in the (a,β) axes by the resistor emulator type input current shaping controller irrespective of the input voltage unbalance. But for a three phase three wire system this would result into unity power factor operation in the phases if $vga + v_{gb} + vgc = 0$.

(2) A controller with the control objective of balancing the phase currents in a three phase three wire system can simultaneously achieve unity power factor operation if the unbalanced phase voltages are at least balanced in phases, i.e., phase shifted by 120°, in all other cases of unbalance unity power factor operation is not possible.

III. ALGORITHM FOR BALANCING THE INPUT CURRENT

The objective of this section is to describe a voltage sensorless, digital current mode control technique that would balance the input currents of a three phase three wire Boost rectifier whose input phase voltages are unbalanced. The input voltages are assumed to be sinusoidal. So

$$vga = V_{ma}\cos(\omega t) \tag{6}$$

$$v_{g\beta} = mV_{m\beta}\sin(\omega t + \varphi)\,,\ where\ (-\frac{\pi}{2} < \varphi < \frac{\pi}{2}) \tag{7}$$

m is +1 if the phase sequence is $A-B-C$ otherwise it is −1. φ is the phase difference between $v_{g\beta}$ and $mV_{m\beta}\sin(\omega t)$. Here we follow the convention that φ is positive if $v_{g\beta}$ leads $mV_{m\beta}\sin(\omega t)$. Since the phase voltages are

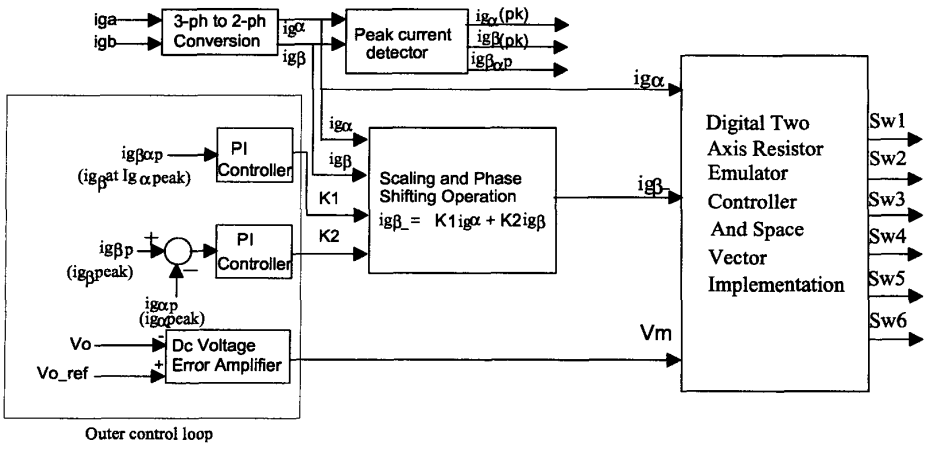


Fig.3 Block diagram of the closed loop input current balance controller

unbalanced , therefore in general , $V_{ma} \neq V_{m\beta}$, and $\varphi \neq 0$.

The control objective of the input current balance controller is to satisfy (8) and (9) simultaneously

$$i_{ga} = I_m \cos(\omega t) \tag{8}$$

$$i_{g\beta} = mI_m \sin(\omega t) \tag{9}$$

For balancing the input phase currents of the Boost rectifier the controller makes i_{ga} and a new variable $i_{g\beta\_}$, instead of $i_{g\beta}$, proportional to v_{ga} and $v_{g\beta}$ respectively. It is shown in (10) that $i_{g\beta\_}$ can be expressed as a linear combination of the sensed currents i_{ga} and $i_{g\beta}$. So under steady state when the rectifier dc output has reached its reference value and the input currents are balanced then

$$\begin{aligned} i_{g\beta\_} &= mI_{m\_} \sin(\omega t + \varphi) \\ &= mI_{m\_} \sin(\omega t)\cos(\varphi) + mI_{m\_} \cos(\omega t)\sin(\varphi) \\ &= K_2 i_{g\beta} + K_1 i_{ga} \end{aligned} \tag{10}$$

Where,

$$K_2 = \frac{I_{m\_}}{I_m}\cos(\varphi) \tag{11}$$

$$K_1 = \frac{mI_{m\_}}{I_m}\sin(\varphi) \tag{12}$$

It can be noted from (11) and (12) that K_2 is a positive constant whereas K_1 can either be positive or negative.

The structure given by (13) is used by the digital controller for configuring $i_{g\beta\_}$ from the currents $i_{ga}$and $i_{g\beta}$. For the n th switching period $i_{g\beta\_}[n]$ can therefore be expressed as

$$i_{g\beta\_}[n] = K_1 i_{ga}[n] + K_2 i_{g\beta}[n]. \tag{13}$$

In this implementation $K_1$and K_2 are obtained as outputs of two independent closed loop PI controllers as shown in the block diagram of the complete control scheme of Fig. 3. In [5], digital implementation of a voltage sensorless resistor emulator controller for three phase Boost rectifier has been described. We use the same carrier control technique here to make $i_{ga}[n]$and $i_{g\beta\_}[n]$ proportional to $v_{ga}[n]$ and $v_{g\beta}[n]$ respectively .

$$i_{ga}[n] = \frac{v_{ga}[n]}{Re} \tag{14}$$

$$i_{g\beta\_}[n] = \frac{v_{g\beta}[n]}{Re} \tag{15}$$

Our definition of voltage vectors and the corresponding sectors are shown in Fig.4. This is equivalent to control of two single phase Boost rectifiers, one in α axis and the other in β axis. The duty ratios $d_\alpha[n]$ and $d_\beta[n]$ need to satisfy (16) and (17) respectively

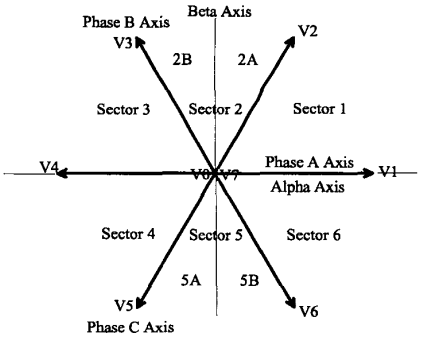


Fig.4 Voltage vectors produced by the the PWM converter of Fig.1 and the corresponding definition of '*Sector*'s.

$$igar[n] = \frac{Vo(1-da[n])}{Re} \quad (16)$$

$$i_{g\beta\_r}[n] = \frac{Vo(1-d_\beta[n])}{Re} \quad (17)$$

The modulators work on positive quantities, so based on the sector information, we generate $igar[n]$ and $i_{g\beta\_r}[n]$ as rectified current variables .

Vo is the regulated output of the two parallel connected single phase rectifiers. . After replacing $\frac{VoRs}{Re}$ by Vm in (16) and (17), where Rs is the current sense resistance, we can calculate the duty ratios $da[n]$ and $d_\beta[n]$ from

$$da[n] = (1 - \frac{igar[n]Rs}{Vm}) \quad (18)$$

$$d_\beta[n] = (1 - \frac{i_{g\beta\_r}[n]Rs}{Vm}) \quad (19)$$

From $iga[n]$and $ig_\beta[n]$, we can use (13) to get $i_{g\beta\_}[n]$.

We need to interpret the duty ratios requirements in terms of space vector PWM signals that would satisfy (18) and (19) simultaneously in every switching period. For that, from $da[n]$ and $d_\beta[n]$, we have to find out the time durations $T_1[n]$ and $T_2[n]$,for the two active vectors A_{v1} and A_{v2} to effectively produce the same volt-sec on each axis as demanded by the independent controllers. The remaining time $T_0[n]$ of the period should be used for the null vector A_0. If the active vectors $A_{v1}$and A_{v2} for s 1,3,4 and 6are identified as in TABLE I, then the corresponding time $T_1[n]$and $T_2[n]$, needed for synthesis of any vector (P, Q, R or S) with an angle θ with respect to the α axis of the segment, can be obtained by solving the following simultaneous equations.

$$(\frac{1}{2}).T_1[n] + T_2[n] = (1-da[n])Ts \quad (20)$$

$$(\frac{\sqrt{3}}{2})T_1[n] = (1-d_\beta[n])Ts \quad (21)$$

Similarly for *Sectors* $2A, 2B, 5A$and $5B$, TABLE II gives the selection of vectors. The following simultaneous equations can be used to solve for $T_1[n]$*and* $T_2[n]$.

$$(\frac{1}{2}).T_1[n] - (\frac{1}{2}).T_2[n] = (1-da[n])Ts \quad (22)$$

$$(\frac{\sqrt{3}}{2}).T_1[n] + (\frac{\sqrt{3}}{2}).T_2[n] = (1-d_\beta[n])Ts \quad (23)$$

Fig. 5 shows the generation of PWM signals for *Sector* 1 in the Event manager module of DSP TMS320F240.

This controller implements self-synchronization of the converter switching with respect to line voltage based on the following logic: as long as the sector selection is correct , the α and β axis modulators will produce duty ratios less

TABLE I

Sector	A_{v1}	A_{v2}
1	*V2*	*V1*
3	*V3*	*V4*
4	*V5*	*V4*
6	*V6*	*V1*

TABLE II

Sector	A_{v1}	A_{v2}
2A	*V2*	*V3*
2B	*V3*	*V2*
5A	*V5*	*V6*
5B	*V6*	*V5*

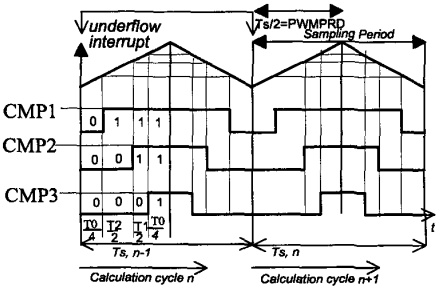


Fig. 5 Generation of symmetric PWM pulses in the Event manager module of DSP TMS320F240

than 1, i.e, $da[n] < 1$ *or* $d_\beta[n] < 1$. Similarly $T_2[n] > 0$ for the modulator to operate in the unsaturated region. When any one of these conditions are not satisfied , the next sector in sequence is chosen.

IV. DETERMINATION OF K_1,AND K_2

It can be seen from (13) that the constants K_1 and $K_2 > 0$ should be known for the computation of $i_{g\beta\_}[n]$. The conditions necessary for balancing iga and $i_{g\beta}$ are imposed on two independent closed loop controllers in order to determine $K_1$and K_2. This is shown in the block diagram of Fig. 3. Under balanced condition peak value of

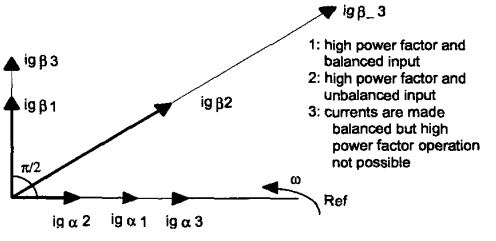
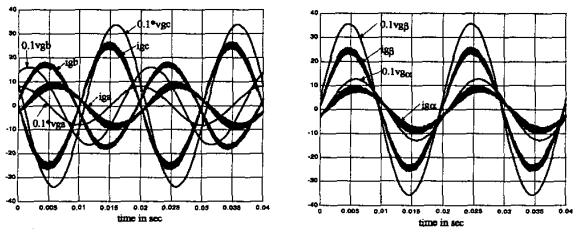
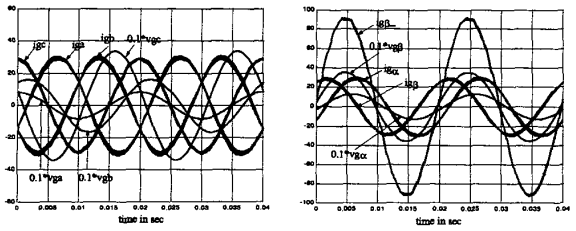


Fig. 6 Phasor diagram of the control variables ($iga, i_{g\beta}, i_{g\beta\_}$) under balanced and unbalanced input voltage conditions



(a) (b)

Fig. 7 Simulation result under unbalanced input voltage condition without input the current balance controller (a) Scaled v_{ga}, v_{gb}, v_{gc} and i_{ga}, i_{gb}, i_{gc} (b) Scaled $v_{ga}, v_{g\beta}$ and $i_{ga}, i_{g\beta}$



(a) (b)

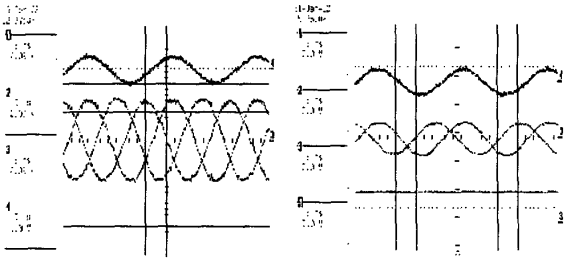
Fig. 8 Simulation result under unbalanced input voltage condition with the input current balance controller (a) Scaled v_{ga}, v_{gb}, v_{gc} and i_{ga}, i_{gb}, i_{gc} (b) Scaled $v_{ga}, v_{g\beta}$ and $i_{ga}, i_{g\beta}$

the α axis current , $i_{g\alpha p}$, over a line cycle, ($T = \frac{2\pi}{\omega}$), has to be equal to the peak value of the β axis current, $i_{g\beta p}$. This condition is imposed on one of the PI controllers in order to determine K_2 .

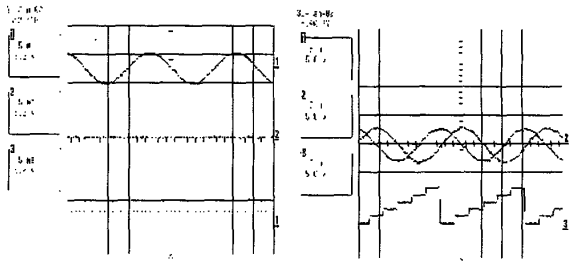
K_1 is obtained in a similar manner from the output of another PI controller that basically imposes the phase balance condition. The input to this PI controller is $i_{g\beta\alpha p}$, that is defined as the β axis current sampled at the instant when the α axis current is at its positive peak. Under steady state $i_{g\beta\alpha p}$ should be zero and this is defined as the zero phase condition for $i_{g\beta}$. Fig. 6 shows the time phasor diagrams of $i_{ga}, i_{g\beta}, and\ i_{g\beta\_}$ under balanced and unbalanced input voltage conditions.

V. Simulation Results

The proposed input current balance controller for a three phase three wire Boost rectifier is simulated on MATLAB-SIMULINK (version 5.3) platform. In the simulation, the unbalanced input voltages are chosen arbitrarily as $v_{ga} = 81.6\sin(\omega t), v_{gb} = 163.3\sin(\omega t - \frac{\pi}{6})$, $v_{gc} = 338.8\sin(\omega t - \frac{19\pi}{12})$. The operating parameters are: $V_O = 700V, L = 2mH, T_S = 100\mu S, R = 100\Omega$. Fig. 7 and



(a) (b)



(c) (d)

Fig.9 Experimental results with the current balance controller under normal input voltage condition (a) v_{gb} (Ch4 : 300V/div) and i_{ga}, i_{gb}, i_{gc} (Ch1,Ch2,Ch3: 3.2A/div) (b)v_{gb}(Ch4 :300V/div), $i_{ga}, i_{g\beta}$ (Ch1,Ch2: 8A/div) and V_O (Ch3: 270V/div) (c) v_{gb} (Ch1: 300V/div) and K_1, K_2 (Ch2,Ch3: 1/div) (d)$i_{ga}, i_{g\beta\_}$(Ch1,Ch2: 8A/div) and '*Sector*'(Ch3: 4/div)

Fig. 8 show the simulated input voltage and input current waveforms without and with the input current balance controller respectively.

VI. Experimental Results

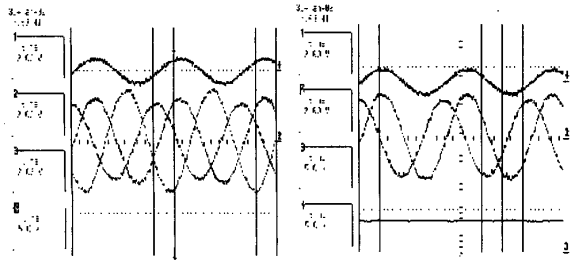
The control algorithm is implemented on DSP TMS320F240F based controller. The nominal operating point of the experimental Boost rectifier when the phase voltages are very nearly balanced is as follows:

$$Vga(phase) = 100V(rms) - star, V_O = 310V(dc - regulated),$$

$$L = 6mH, T_S = 100\mu Sec, R = 100\Omega$$

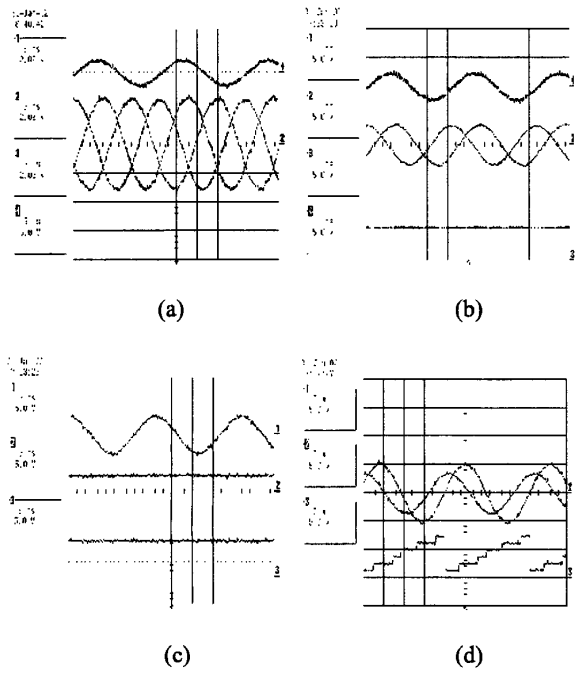
The experimental results of Fig. 9 (a),(b),(c) and (d) show balanced phase currents (i_{ga}, i_{gb}, i_{gc}), balanced (α, β) axis currents ($i_{ga}, i_{g\beta}$) , the output dc voltage V_O , the constants K_1, K_2 and the sequence of '*Sector*' change. From the measured $v_{gb}$and i_{gb} waveforms we can see that the power factor in phase B is nearly 1. These results demonstrate that the current balance controller does not interfere with the power factor correction objective under balanced input voltage condition.

The unbalance in the input phase voltages is created by changing the equivalent Thevenin impedance in one of the



(a) (b)

Fig. 10 Experimental results without the of the current balance controller under unbalanced input voltage condition (a) v_{gb} (Ch4 : 300V/div) and iga, i_{gb}, igc (Ch1,Ch2,Ch3: 3.2A/div) (b)v_{gb}(Ch4 :300V/div), $iga, i_{g\beta}$ (Ch1,Ch2: 3.2A/div) and V_O (Ch3: 270V/div)



(a) (b)

(c) (d)

Fig. 11 Experimental results with the current balance controller under unbalanced input voltage condition (a) v_{gb} (Ch4 : 300V/div) and iga, i_{gb}, igc (Ch1,Ch2,Ch3: 3.2A/div) (b)v_{gb}(Ch4 :300V/div), $iga, i_{g\beta}$ (Ch1,Ch2: 8A/div) and V_O (Ch3: 270V/div) (c) v_{gb} (Ch1: 300V/div) and K_1, K_2 (Ch2,Ch3: 1/div) (d)$iga, i_{g\beta\_}$(Ch1,Ch2: 8A/div) and $'Sector'$(Ch3: 4/div)

input source voltages. In this experimental unit we have added a series impedance consisting of $R_T = 8\Omega$ and $L_T = 22mH$ connected in series in the phase A supply line of the rectifier. Under such condition Fig. 10(a) and (b) show the unbalanced currents when current balance controller is not activated.

However when current balance control is used in the outer loop of the control structure the experimental results of Fig. 11 (a),(b),(c) and (d) show the balanced phase currents (iga, i_{gb}, igc), balanced (α, β) axis currents $(iga, i_{g\beta})$, the internal current variable $i_{g\beta\_}$, the output dc voltage V_O, the constants K_1, K_2 and the sequence of $'Sector'$ change. If we compare Fig. 10(a) with Fig. 11(a), the change in phase of i_{gb}due to the current balance control can be observed. However the power factor in each of the phases can not be adjusted to unity, as can be noted by observing $v_{gb}$and i_{gb}.

VII. CONCLUSION

This paper proposes a simple control method that can balance the input current of a three phase three wire Boost rectifier under unbalanced input voltage condition. The objective is to operate the rectifier in the high power factor mode under normal operating condition but to give overriding priority to the current balance function in case of unbalance in the input voltages., as a result of which high power factor operation in all the phases may not be possible. The control technique is input voltage sensorless and suitable for constant switching frequency digital implementation. It is computationally simple - the execution time of the control loop is less than $40\mu Sec$ on TMS320F240. Further this being a closed loop current balance method, is insensitive to the unbalance in the circuit component values - like per phase Boost inductance.

REFERENCES

[1] L. Moran, P.D. Ziogas, and G. Joos, " Design aspects of synchronous PWM rectifier-inverter system under unbalanced input voltage conditions," IEEE Transactions on Industry Applications, vol. 28,pp. 1286-1293, Nov/Dec. 1992.

[2] H. S. Kim, H. S. Mok, G. H. Choe, D. S. Hyun, S. Y. Choe "Design of current controller for 3-phase PWM converter with unbalanced input voltage" IEEE PESC Conference, 1998, pp503-509

[3] Ana Vladan Stankovic and Thomas A. Lipo, " A novel control method for input output harmonic elimination of the PWM Boost type rectifier under unbalanced operating conditions," in IEEE Transactions on Power Electronics, vol. 16, no. 5, Sept 2001, pp. 603-611.

[4] P.Rioual, H.Pouliquen and J.P.Louis, "Regulation of a PWM rectifier in the unbalanced network state," in Proc. IEEE-PESC Conference,1993,pp.641-647.

[5] Souvik Chattopadhyay and V. Ramanarayanan , "Digital implementation of a line current shaping algorithm for three phase high power factor Boost rectifier without input voltage sensing, " in APEC'01, pp. 592-600.