An Input Voltage Sensorless Input Current Shaping Method for Three Level Three Phase High Power Factor Boost Rectifier

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Abstract - **This paper proposes a simple digital control scheme to achieve high power factor operation for three level three phase boost rectifier. The controller uses resistor emulator concept in discrete domain to shape the input current like input voltage. It is based on fixed switching frequency, continuous conduction mode (CCM) operation of the converter. The control law is input voltage sensorless, as a result a Phase Locked Loop (PLL) is not required. Structurally it is different from vector control type of control scheme because the controller works in the stationary reference frame and inner loop current regulators are not required. The PWM generation is based on symmetric space vector method. In each control period only six devices (including three complementary) change states. The switching frequency can therefore be half compared to the two level switching rectifiers for the same quality input current waveform. The details of the digital control algorithm has been explained for the hardware platform of Texas Instruments's DSP based unit TMS320F240 EVM**.

Keywords-- Power factor correction, High power factor rectifier, Multilevel Converter, Boost rectifier, Three Level Diode Clamp Converter, Current mode control.

I. INTRODUCTION

Multilevel converters are being used for high voltage and high power applications. The multilevel inverters can synthesize the higher voltage levels using the power devices of lower voltage rating. There are several topologies of the multilevel inverters. Diode clamp power converter are most suitable configuration for the rectifier applications. Theoretically diode clamp inverters with any number of levels can be visualized. But some of the problems like unbalanced voltages, voltage clamping requirements, complexity of switching algorithms, circuit layouts and package constraints have limited the number of levels in practical multilevel converters to seven levels [1].

This paper employs three level diode clamp converter, also known as neutral point clamp converter for high power boost rectification. The three level diode clamp converter consists of two capacitor voltages in series and the center tap as the neutral. Each phase of the three level converter has two pairs of switching devices in series. The center of each pair is clamped to the neutral through clamping diodes [2].

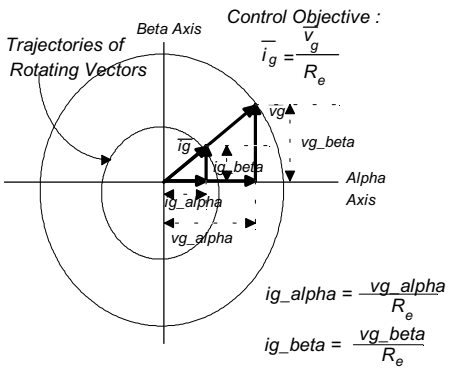

Fig. 1. The control objective of a three phase high power factor boost rectifier

A simple yet high performance control scheme is used in this work to achieve high power factor operation for three level three phase high power factor boost rectifier. The control objective is to operate the rectifier in the high power factor mode under normal operating conditions but to give overriding priority to the current balance function in case of unbalance in the input voltages [3],[4]. This control algorithm provides high performance with much simpler control structure than the conventional vector control method given in [5] -[7]. It does not require sensing of the input voltages and is based on constant switching frequency operation. The input impedance of the boost rectifier need not be balanced as two independent closed loop PI controllers are used to balance the phase currents both in magnitude and phase. The principle of the control algorithm is explained in section II.

This paper uses space vector PWM algorithm for three level power converters. Three level converters have 27 states, which represent 18 space vectors. Each of the vectors V1 to V6 can be synthesized by two inverters states. This property is made use to generate symmetrical PWM pulses. The selection of the switching states to synthesize the commanded vectors is explained in section II. Section III gives the simulation results of the proposed boost rectifier. The simulation results prove

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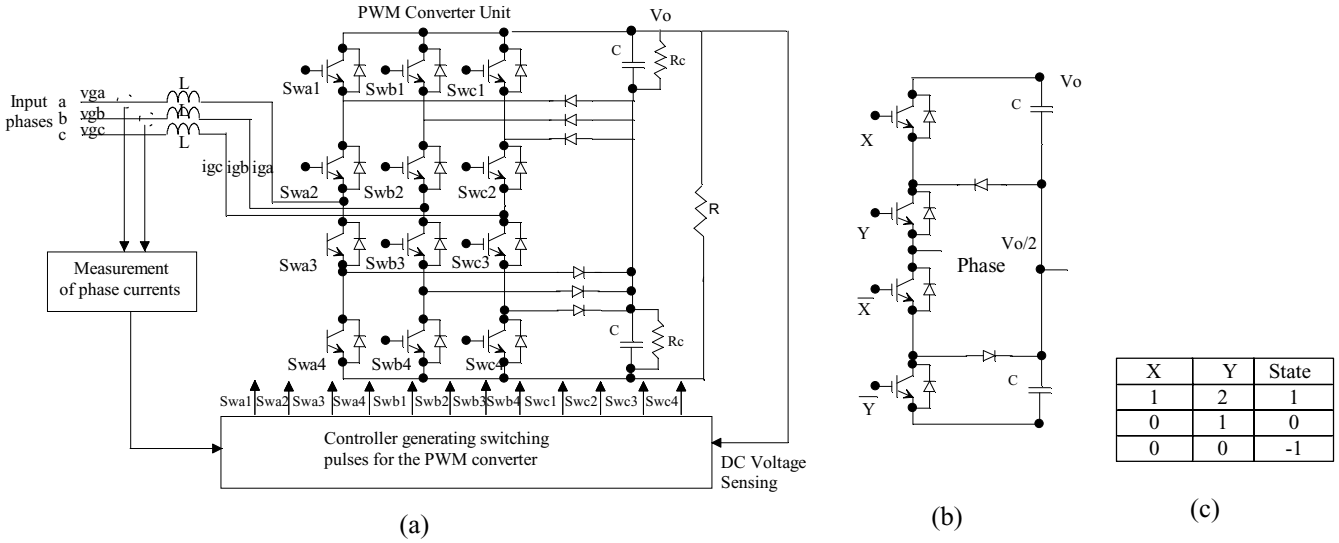


Fig. 2. (a) Three phase three level Boost rectifier circuit and control schematic. (b) Naming convention of switches in each phase. (c) The definition of 'State's based on the switch combination .

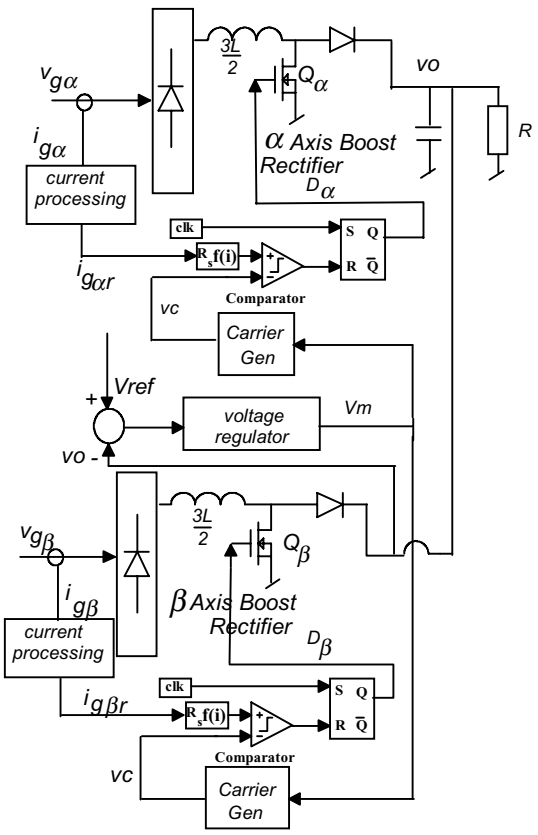


Fig. 3. Functional representation of three phase high power factor boost rectifier with two independent single phase rectifiers in current mode control structure.

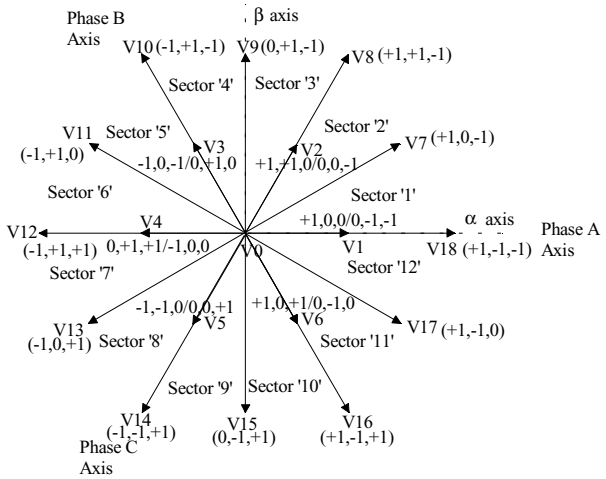


Fig. 4. Definition of voltage vectors and the corresponding sectors

the validity of the control algorithm. In general the present work offers a simple controller with cost effective three level three phase boost rectifier for high voltage applications.

II. CONTROLLER

We can define the control objective of a three phase high power factor Boost rectifier, as

$$\overline{i_g} = \frac{\overline{v_g}}{R_e} \tag{1}$$

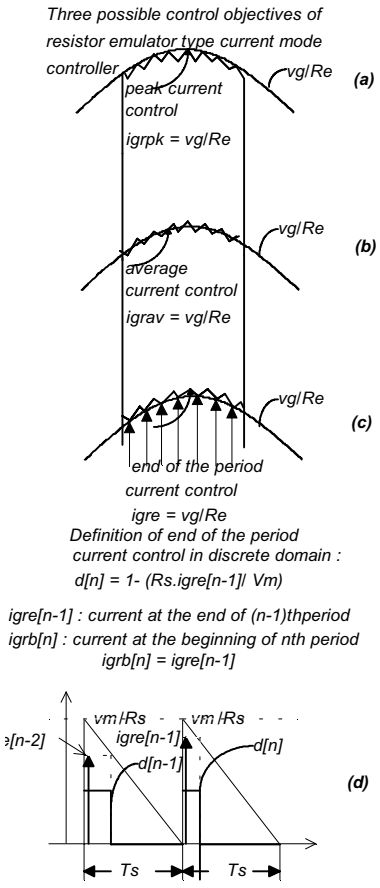


Fig. 5. Discrete version of resistance emulator type current mode controller

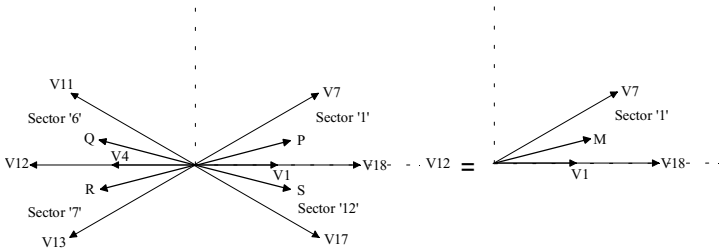


Fig. 6. Mapping of P,Q,R,S vectors into M of Sector 1 for solution of T_1 and T_2 (refer table I)

TABLE I
Vectors in sectors 1,6,7 and 12

Sector	A_{v1}	A_{v2}	A_{vm}
1	*V*7	*V*18	*V*1
6	*V*11	*V*12	*V*4
7	*V*13	*V*12	*V*4
12	*V*17	*V*18	*V*1

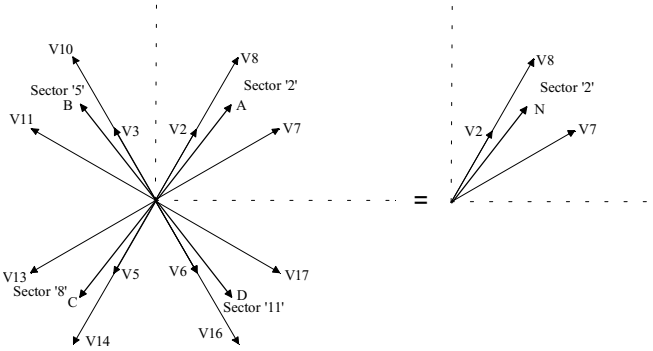


Fig. 7. Mapping of A,B,C,D vectors into N of Sector 2 for solution of T_1 and T_2 (refer table II)

TABLE II
Vectors in sectors 2,5,8 and 11

Sector	A_{v1}	A_{v2}	A_{vm}
2	*V*7	*V*8	*V*2
5	*V*11	*V*10	*V*3
8	*V*13	*V*14	*V*5
11	*V*17	*V*16	*V*6

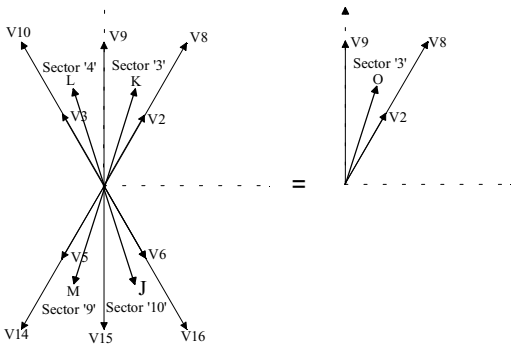


Fig. 8. Mapping of K,L,M,J vectors into N of Sector 2 for solution of T_1 and T_2 (refer table III)

TABLE III
Vectors in sectors 3,4,9 and 10

Sector	A_{v1}	A_{v2}	A_{vm}
3	*V*9	*V*8	*V*2
4	*V*9	*V*10	*V*3
9	*V*15	*V*14	*V*5
10	*V*15	*V*16	*V*6

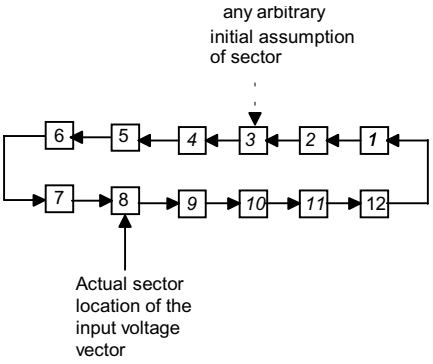


Fig. 9. Sequence of sector change to be followed to eventually synchronize with the location of the input voltage vector.

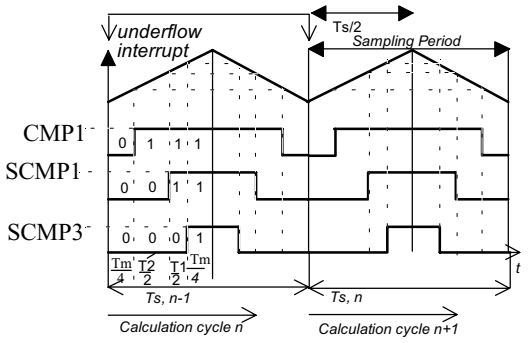


Fig.10 Symmetric PWM generation in the Event manager module of DSP TMS320F240. In each sector out of six independent PWM signals only three signals switch. For example in Sector 1 XA (CMP1), YB (SCMP1) and YC(SCMP3) change states and YA(high),XB(low) and XC(low) remain clamped throughout the period T_s .

, where R_e is the emulated resistance of the rectifier. The $(\bar{\ })$ above a variable indicates a space phasor. This control objective is shown in Fig. 1.

If we take components along α and β axes, which are stationary and orthogonal to each other, the control objective can be expressed in terms of two scalar equations

$$i_{g\alpha} = \frac{v_{g\alpha}}{R_e} \tag{2}$$

$$i_{g\beta} = \frac{v_{g\beta}}{R_e} \tag{3}$$

as shown in Fig. 1. This is equivalent to control of two single phase Boost rectifiers, one in α axis and the other in β axis, as shown in Fig.3. Let us assume here that the duty ratios d_α and d_β of these two switches Q_α and Q_β can be independently controlled. So, we can write,

$$i_{g\alpha r} = \frac{V_o(1-d_\alpha)}{R_e} \tag{4}$$

$$i_{g\beta r} = \frac{V_o(1-d_\beta)}{R_e} \tag{5}$$

V_o is the regulated output of the overall rectifier. i_{gar} and $i_{g\beta r}$ are obtained by rectifying $i_{g\alpha}$. and $i_{g\beta}$ respectively. Conceptually this is eqivalent to two current sources charging the same capacitor for voltage output. The control structure is also shown in Fig.3. In continuous time domain, $i_{gar}$and $i_{g\beta r}$ can be made to represent peak current, average current , or end of the period current of the inductor in every switching period T_s. This is shown in Fig. 5(a) ,5(b) and 5(c) respectively. Fig.2 (a) gives the circuit and control schematic of three phase three level boost rectifier. The naming convention of the switches in each phase are according to Fig.2(b) and Fig.2(c) gives the definition of 'State's based on the valid switch combination. Our definition of voltage vectors and the corresponding sectors are shown in Fig.4. However, in discrete implementation, current is sampled only once in a switching period. So, unless the sampling instant in a period is varied [4], the control objectives shown in Fig.5(a) or 5(b) can not be implemented. In contrast, Fig.5(c) is ideal for digital implementation, because the sampling instant can be kept fixed at the beginning of every switching period. We can calculate the duty ratios $d_\alpha[n]$ and $d_\beta[n]$ from expressions

$$d_\alpha[n] = (1 - \frac{i_{gare}[n-1]R_s}{V_m}) = (1 - \frac{i_{gar}[n]R_s}{V_m}) \tag{6}$$

$$d_\beta[n] = (1 - \frac{i_{g\beta re}[n-1]R_s}{V_m}) = (1 - \frac{i_{g\beta r}[n]R_s}{V_m}) \tag{7}$$

after replacing $\frac{V_o R_s}{R_e}$ by V_m in (4) and (5). The suffix $'e'$ indicates that the current is sampled at the end of the period. It should be noted that the current at the end of period $[n-1]$ is same as the current at the beginning of period $[n]$. This is shown in Fig.5(d). Here, R_s is the current sensing resistance. However, we need to satisfy (6) and (7) simultaneously in every switching period. So, from $d_\alpha[n]$ and $d_\beta[n]$, we have to determine the time duration $T_1[n]$ and $T_2[n]$, for the two active vectors $A_{v1}$and A_{v2} respectively, to effectively produce the same volt-sec on each axis as demanded by the independent controllers. The remaining time $T_o[n]$ of the period should be used for the null vector A_{vo} . From Fig.6, it can be noted that if the active vectors $A_{v1}$and A_{v2} for sectors $1, 6, 7$ and 12 are identified as in Table I, then the corresponding time $T_1[n]$ and $T_2[n]$, needed for synthesis of any vector (P, Q, R or S) with an angle θ with respect to the α axis of the segment, can be obtained by solving the following simultaneous equations.

$$(\frac{\sqrt{3}}{2}).\frac{\sqrt{3}}{2}T_1[n] + T_2[n] = (1 - d_\alpha[n])T_s \tag{8}$$

$$(\frac{\sqrt{3}}{2})\frac{1}{2}T_1[n] = (1 - d_\beta[n])T_s \tag{9}$$

TABLE IV

$i_{g\alpha}$. and $i_{g\beta}$ in each sector

Sector	$i_{gar}[n]$	$i_{g\beta r}[n]$
1	$i_{g\alpha}[n]$	$i_{g\beta}[n]$
2	$i_{g\alpha}[n]$	$i_{g\beta}[n]$
3	$i_{g\alpha}[n]$	$i_{g\beta}[n]$
4	$i_{g\alpha}[n]$	$i_{g\beta}[n]$
5	$-i_{g\alpha}[n]$	$i_{g\beta}[n]$
6	$-i_{g\alpha}[n]$	$_{g\beta}[n]$
7	$-i_{g\alpha}[n]$	$-i_{g\beta}[n]$
8	$-i_{g\alpha}[n]$	$-i_{g\beta}[n]$
9	$-i_{g\alpha}[n]$	$-i_{g\beta}[n]$
10	$i_{g\alpha}[n]$	$-i_{g\beta}[n]$
11	$i_{g\alpha}[n]$	$-i_{g\beta}[n]$
12	$i_{g\alpha}[n]$	$-i_{g\beta}[n]$

For sectors $2, 5, 8$ and 11, as shown in Fig.7, Table II gives the selection of vectors. The following simultaneous equations can be used to solve for $T_1[n]$ and $T_2[n]$.

$$(\frac{\sqrt{3}}{2}).\frac{\sqrt{3}}{2}T_1[n] + (\frac{1}{2}).T_2[n] = (1-d_\alpha[n])T_s \quad (10)$$

$$(\frac{\sqrt{3}}{2}).\frac{1}{2}T_1[n] + (\frac{\sqrt{3}}{2}).T_2[n] = (1-d_\beta[n])T_s \quad (11)$$

For sectors $3, 4, 9$ and 10 ,as shown in Fig.8, Table III gives the selection of vectors. The following simultaneous equations can be used to solve for $T_1[n]$ *and* $T_2[n]$.

$$\frac{1}{2}T_2[n] = (1-d_\alpha[n])T_s \quad (12)$$

$$(\frac{\sqrt{3}}{2}).T_1[n] + (\frac{\sqrt{3}}{2}).T_2[n] = (1-d_\beta[n])T_s \quad (13)$$

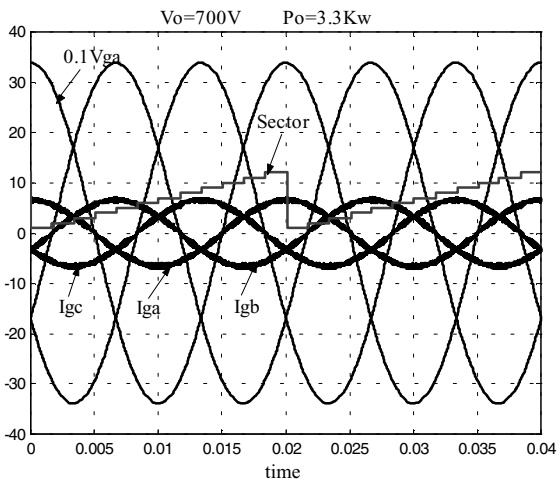
It can be seen that input voltage need not be sensed for computation of $T_1[n]$ and $T_2[n]$. However the sector information should be known for appropriate selection of active vectors. This controller implements self-synchronization of the converter switching with respect to line voltage based on the following logic: as long as the sector selection is correct , the α and β axis modulators will produce duty ratios less than 1, i.e, $d_\alpha[n] < 1$ *or* $d_\beta[n] < 1$. Similarly $T_1 > 0$ *and* $T_2[n] > 0$ have to be satisfied for the modulator to operate in the unsaturated region. When any one of these conditions are violated , the next sector in sequence is chosen, as shown in Fig.9. This sector change can take place in the same switching cycle in which it had saturated because of incorrect selection of vectors. After that the modulator will recalculate the duty ratios, which won't saturate now as the sector selection is correct. In this implementation of the three level switching we will not use any zero vector , instead the

TABLE V
Full compare unit of TMS320F240

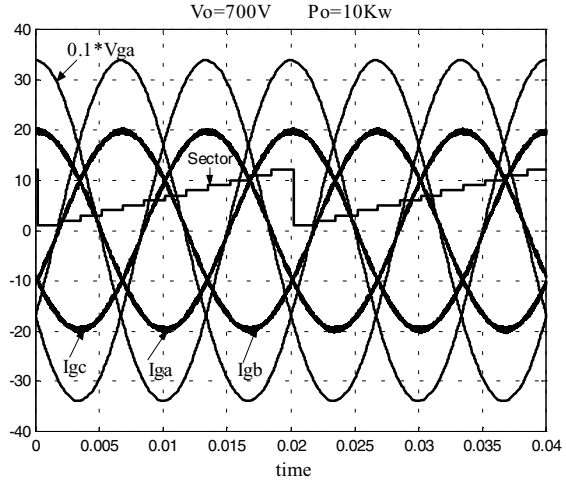
sector	*CMP*1 for signal Xa	*CMP*2 for signal Ya	*CMP*3 for signal Xb
1	$T_x = (T_s - T_1 - T_2')/4$	0	$T_s/2$
2	$T_x = (T_s - T_1 - T_2')/4$	0	$T_x + T_1/2$
3	$T_x + T_1/2$	0	$T_x = (T_s - T_1 - T_2')/4$
4	$T_s/2$	$T_x + T_2'/2$	$T_x = (T_s - T_1 - T_2')/4$
5	$T_s/2$	$T_x + T_1/2 + T_2'/2$	$T_x = (T_s - T_1 - T_2')/4$
6	$T_s/2$	$T_x + T_2'/2 + T_1/2$	$T_x = (T_s - T_1 - T_2')/4$
7	$T_s/2$	$T_x + T_2'/2 + T_1/2$	$T_x + T_1/2$
8	$T_s/2$	$T_x + T_2'/2 + T_1/2$	$T_s/2$
9	$T_s/2$	$T_x + T_2'/2$	$T_s/2$
10	$T_x + T_1/2$	0	$T_s/2$
11	$T_x = (T_s - T_1 - T_2')/4$	0	$T_s/2$
12	$T_x = (T_s - T_1 - T_2')/4$	0	$T_s/2$

TABLE VI
Simple compare unit of TMS320F240

sector	*SCMP*1 for signal Yb	*SCMP*2 for signal Xc	*SCMP*3 for signal Yc
1	$T_x + T_2'/2$	$T_s/2$	$T_x + T_1/2 + T_2'/2$
2	0	$T_s/2$	$T_x + T_1/2 + T_2'/2$
3	0	$T_s/2$	$T_x + T_1/2 + T_2'/2$
4	0	$T_s/2$	$T_x + T_1/2 + T_2'/2$
5	0	$T_s/2$	$T_x + T_2'/2$
6	0	$T_x + T_1/2$	0
7	0	$T_x = (T_s - T_1 - T_2')/4$	0
8	$T_x + T_2'/2$	$T_x = (T_s - T_1 - T_2')/4$	0
9	$T_x + T_1/2 + T_2'/2$	$T_x = (T_s - T_1 - T_2')/4$	0
10	$T_x + T_1/2 + T_2'/2$	$T_x = (T_s - T_1 - T_2')/4$	0
11	$T_x + T_1/2 + T_2'/2$	$T_x + T_1/2$	0
12	$T_x + T_1/2 + T_2'/2$	$T_s/2$	$T_x + T_2'/2$



(a)



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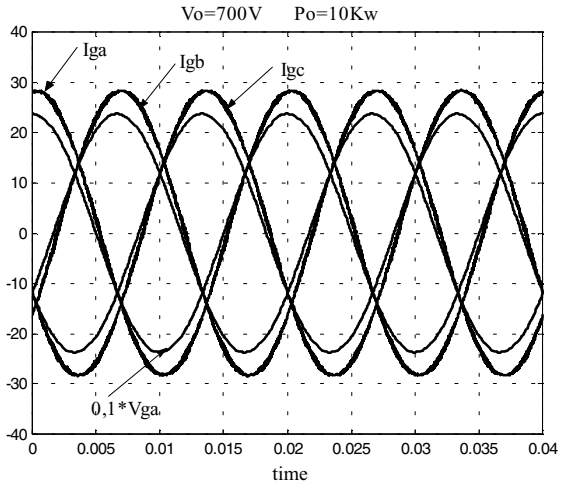

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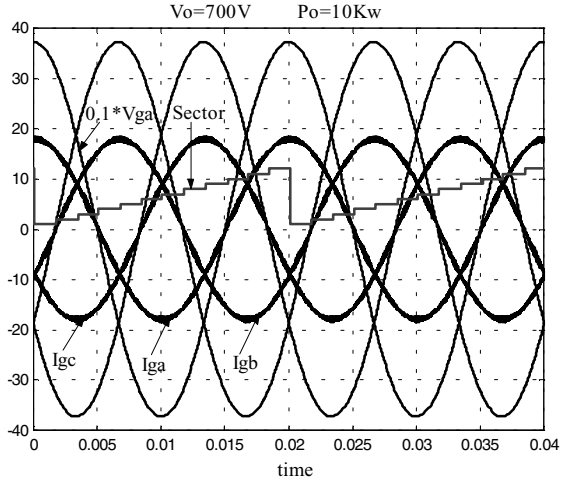
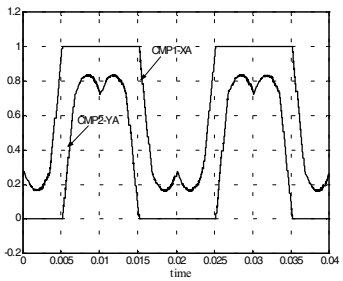
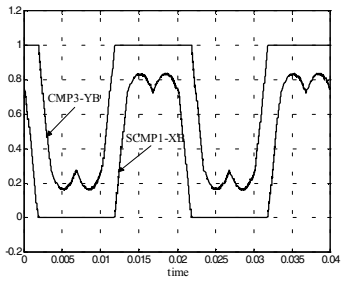


(d)

Fig. 11 (a) and(b) show input phase voltages and currents at load 3.3*Kw* and 10*Kw* respectively**.** The sector change sequence is also shown. (c) and (d) show input phase voltages and currents at 70% and 110% of the rated input voltage for 10*Kw* load.



(a)



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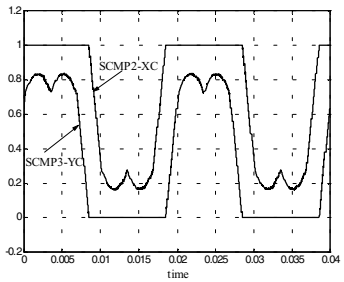

(c)

Fig.12 (a),(b), and (c) show the normalized profile ($\frac{T_s}{2}$ *is equivalent to* 1) of the compare register entries for the switches XA,YA,XB,YB,XC and YC as listed in Table VI over the line cycle.

effective volt-sec will be synthesized by A_{v2} , now switched for duration $T_2^{'}$, and A_{vm} , switched for duration

$$T_m = (T_s - T_1 - T_2^{'})$$

$$T_2^{'} = 2T_2 - T_s + T_1 \quad (14)$$

$$T_m = 2(T_s - T_1 - T_2) \quad (15)$$

In each sector of Fig. 4, A_{vm} can be identified as the middle level vector , as specified in Table I, II and III. It can be produced by two alternative combinations of switching states . It will be shown in later part of this discussion that by effectively using this property of the middle level vector we can generate symmetric PWM pulses from the event manager module of the DSP TMS320F240.

Here we should explain the current processing function of the modulator. First, the two phase currents $i_{ga}[n]$and $i_{gb}[n]$ are sensed and converted to $i_{ga}[n]$ and $i_{g\beta}[n]$ by standard three phase to two phase transformation. However, the modulators work on DC quantities, so based on the sector information, we generate $i_{gar}[n]$ and $i_{g\beta r}[n]$, as shown in Table 1V, and use them for calculation of duty ratios.

In any phase of the converter, if we do not consider the effect of dead time in the switching signals, then it can be seen from Fig.2(b) that only two of the four switching signals have to be independently controlled. The switching states produced by the combination of signals for these switches ,(1=ON,0=OFF), are defined in Table 1. So, in each switching period, the TMS320F240 based digital controller has to generate six independent PWM signals corresponding to the previously computed $T_1, T_2^{'}$ and T_m values. The 'Event Manager Module' of TMS320F240 has two 'Compare Unit's , each consisting of three compare registers , that are loaded with values given by Table V and Table VI. Each compare unit is clocked by the internal timer circuit, Timer 1 in this case, at the required frequency. In this implementation the timer is configured to work in 'continuous up-down' counting mode. Each cycle of control calculations are initiated by the timer 'underflow interrupt'. It can be observed from Table V and Table VI that only three of the six signals change states in a control period. The symmetrical PWM generation procedure for sector 1 is shown in Fig 10 as an example.

III. SIMULATION RESULTS

The proposed controller is simulated on MATLAB-SIMULINK (version 5.3) software platform. The nominal rating of the three phase Boost rectifier is chosen to be $10Kw, 415Vac, 700Vdc$ .The inductance/phase is $3mH$. The control loop period is $T_s = 100\mu Sec$, so the switching frequency of the semiconductor devices is $2.5KHz$. Under rated input voltage condition and at regulated $700V$ output, Fig. 11 (a) and(b) show input phase voltages and currents at load $3.3Kw$ and $10Kw$ respectively. The sector change sequence is also shown. Fig.11 (c) and (d) show input phase voltages and currents at 70% and 110% of the rated input voltage for $10Kw$ load. Fig.12 (a),(b), and (c) show the normalized profile ($\frac{T_s}{2}$ *is equivalent to* 1) of the compare register entries as listed in Table V and Table V1 over a line cycle for the switches XA,YA,XB,YB,XC and YC.

IV. CONCLUSION

This paper describes a discrete current mode control algorithm that can performs high power factor operation for a three phase three level Boost rectifier. The salient features of this controller are : (1) No input voltage sensing is required, as switching pulses get self-synchronized with the line frequency, (2) No need to use PLL, as the controller works in stationary reference frame, (3) Two decoupled fixed frequency current mode controllers are used to generate the equivalent ON and OFF durations for shaping currents in two orthogonal axes , (4) A combined switching strategy is developed in the form of space vectors to simultaneously satisfy the timing requirements of both the current mode controllers in a control period. (5) The PWM signals are symmetric , requires only three switches (also the complementary devices) to change states in a control period and can be implemented in a general purpose DSP like TMS320F240. The switching frequency therefore can be half compared to the two level rectifiers for the same quality of input current wave form. In conclusion, it can be said that, this method of control of three phase three level high power factor boost rectifier provides comparable or better performance over existing methods with a much simpler control structure.

REFERENCES

[1] Jih-Sheng Lai and Fang Zheng Peng, "Multilevel Converters -A new breed of power converters," *IEEE Transactions on Industry Applications,* vol .32, no .3, pp 509-517, May/June 1996.

[2] Akira Nabae, I. Takahashi and H. Akagi, "A new neutral point clamped PWM inverterrs," *IEEE Transactions on Industry Applications*, vol.7, no. 5, pp 518 -523, Sept/Oct 1981.

[3] Souvik Chattopadhyay and V. Ramanarayanan , "Digital implementation of a line current shaping algorithm for three phase high power factor Boost rectifier without input voltage sensing,," *Proc. of APEC'01*, pp. 592-600, 2001

[4] S.Buso,P.Mattavelli, L.Rossetto and G.Splazzi, " Simple Digital Control Improving Dynamic Performance of Power Factor Preregulators," *IEEE Transactions on Power Electronics* , Vol. 13, No. 5, Sept 1998.

[5] H. S. Kim, H. S. Mok, G. H. Choe, D. S. Hyun and S. Y. Choe "Design of Current Controller for 3-Phase PWM Converter with unbalanced input Voltage," *Proc. of IEEE PESC Conference, 1998*, pp503-509, 1998

[6] Ana Vladan Stankovic and Thomas A. Lipo, " A novel control method for input output harmonic elimination of the PWM Boost type rectifier under unbalanced operating conditions," *IEEE Transactions on Power Electronics*, vol. 16, no. 5, pp. 603-611, Sept. 2001.

[7] P.Rioual, H.Pouliquen and J.P.Louis, "Regulation of a PWM rectifier in the unbalanced network state," *Proc. IEEE-PESC Conference,* pp.641-649 , 1993.

[8] TMS320C24x DSP Controllers Peripheral Library and Specific Devices - Reference Set - Volume 2, Literature Number : SPRU161B December 1997.