Space Vector Based Synchronized PWM Algorithm for Three Level Voltage Source Inverters: Principles and Application to *V/f* Drives

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Abstract- This paper describes the synchronized PWM techniques based on space vector approach for three level voltage source inverters. The objective is to improve the output waveform of the inverters used in high power applications, where the switching frequency is very low. This is achieved by maintaining the synchronization and half wave symmetry, quarter wave symmetry, three-phase symmetry in the PWM waveforms. The principles of achieving synchronization and symmetries are presented. The proposed algorithm is implemented on TMS320F240 based digital controller and applied to *V/f* drive. The experimental waveforms of the inverter output voltage and motor no load current for different operating eonditions of the drive are presented. The V_{WTHD} of the line voltage and I_{THD} of the no load current of the motor are computed from the experimental data. The performance measure in terms of the V_{WTHD} of the line voltage is computed for the entire operating region of the drive for the proposed algorithm and the synchronized SPWM technique. The comparative results show that the proposed method has improved THD over SPWM method. Another significant feature of the proposed algorithm is that the symmetry and synchronization leads to self-halancing of the D.C. bus capacitor voltages.

I. INTRODUCTION

Three level inverters are preferred for high power applications since they can achieve double the voltage rating; hence double the power capacity with the semiconductor switches of similar rating as that of two level inverters. Switching frequency (f_{sw}) of these inverters is limited to low values (350 Hz to 1KHz) to reduce the switching losses. Hence the ratio of f_{sw} to the fundamental frequency f_1 or the pulse number ($p = f_{sw}/f_1$) is low. Under such circumstances, the output voltage of the inverter will he rich in harmonics. The output voltage must he synchronized with its fundamental component in order to eliminate sub harmonics. In the case of two level inverters, it is shown that in addition to synchronization, preserving half wave symmetry (HWS), quarter wave symmetry (QWS) and three phase symmetry (TPS) in the output voltage will improve the performance of the inverter compared to the PWM methods which do not preserve symmetries [1].

Practical three level inverters employ sine triangle PWM (SPWM) technique because of its simplicity. However the space vector PWM (SVPWM) gives a better D.C. utilization and greater flexibility in selecting the switching states. The purpose of the present work is to develop a simple SVPWM technique, which will result in synchronous PWM waveforms with QWS, HWS and TPS. Hence the output voltages will have improved waveform with reduced harmonics. An important feature of this technique is that this method is simple to implement on digital controllers and has reduced computational requirements compared to the conventional SVPWM technique. The basic principle of the space vector approach to synchronization and symmetry is detailed in section II.

Another major contribution of the proposed PWM technique is that the synchronization and symmetry in the output waveforms ensures that the D.C. link capacitor voltages are balanced over every cycle of the fundamental. This will help in reducing the D.C. link capacitor requirements.

The proposed PWM technique is implemented on TMS320F240 fixed point DSP controller. This technique is applied to *V/f* drive on experimental prototype consisting of 400V, 10HP, Induction Motor powered from 10KVA,IGBT based three level diode clamp inverter. The experimental results are presented in section III. The performance of the proposed technique is studied over the entire operating range of the drive. A comparison in terms of the weighted total harmonic distortion factor of the output line voltage (V_{WTHD}) is given for the proposed technique and SPWM technique. The comparative results reveal the superiority of the present method over SPWM technique in terms of the THD.

II. PRINCIPLES

Fig.1 shows the circuit diagram of three level diode clamp inverter. The space vectors associated with the three level inverters on $\alpha - \beta$ plane are shown in fig.2. The states are defined in Table I. In space vector approach to PWM the reference vector $\bar{V}_r$ is sampled at regular intervals T_s. The sampled reference vector is approximated by time averaging the nearest three vectors $\bar{V}_x, \bar{V}_y$ and $\bar{V}_z$ according to (1)

$$\bar{V}_r T_S = \bar{V}_x T_x + \bar{V}_y T_y + \bar{V}_z T_z, \qquad (1)$$

where, T_x, T_y and T_z are the intervals of $\bar{V}_x, \bar{V}_y$ and $\bar{V}_z$ respectively and $T_s = T_x + T_y + T_z$

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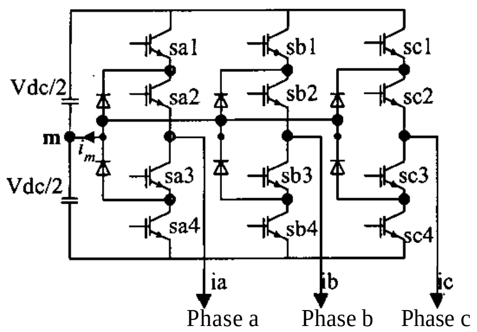


Fig. 1 Circuit digram of three level diode clamp inverter

TABLE I
DEFNITION OF INVERTER STATES

State	Switch Position	Pole voltage with respect to V_m
1	sa1=ON, sa2=ON sa3=OFF , sa4=OFF	Vdc/2
0	sa1=OFF, sa2=ON sa3=ON ,sa4=OFF	0
-1	sa1=OFF, sa2=OFF sa3=ON , sa4=ON	-Vdc/2

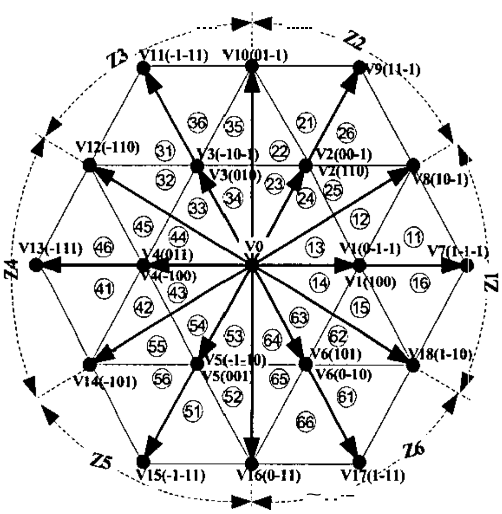
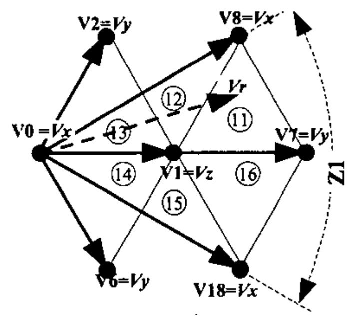
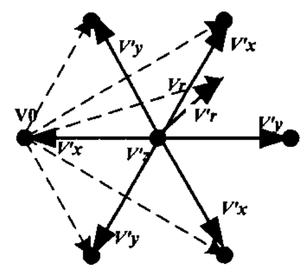


Fig.2. Space vectors of three level inerter.

In order to simplify the above equation, a novel approach is adopted. The space vector plane is divided in to six sectors, each of sixty degrees interval as shown in fig.1. Each sector Z, where $Z = 1, 2, ...6$, is associated with one pivot vector $\bar{V}_Z$ and six other vectors. The pivot vector $\bar{V}_1$ and other six vectors of sector 1 are redrawn in fig.3 **(a).** The vectors of the other sectors are phase displaced by



(a)



(b)

Fig.3.(a) Space vectors associated with sector 1. (b) Mapping of the vectors of sector Ito fictitious vectors.

TABLE II
PIVOT VECTORS AND THEIR STATES

Sector Z	Pivot Vector $\bar{V}_z$	$\bar{V}_{zx}$	$\bar{V}_{zy}$
1	$\bar{V}_1$	100	0-1-1
2	$\bar{V}_2$	110	00-1
3	$\bar{V}_3$	010	-10-1
4	$\bar{V}_4$	011	-100
5	$\bar{V}_5$	001	-1-10
6	$\bar{V}_6$	101	0-10

$(Z-1)\pi/3$ radians. All the six sectors exhibit symmetry and this property is exploited to reduce the computation complexity of the time intervals. All the vectors of a given sector can be mapped to seven vectors, with pivot vector as the origin according to (2).

$$\bar{V}_r^1 = \bar{V}_r e^{j(Z-1)\pi/3} - \bar{V}_1,$$
$$\bar{V}_x^1 = \bar{V}_x e^{j(Z-1)\pi/3} - \bar{V}_1,$$
$$\bar{V}_y^1 = \bar{V}_y e^{j(Z-1)\pi/3} - \bar{V}_1 \text{ and}$$
$$\bar{V}_z^1 = \bar{V}_z e^{j(Z-1)\pi/3} - \bar{V}_1 = 0. \quad (2)$$

The mapping of the all the seven vectors of sector I to fictitious vectors is illustrated in fig. 3(b). The equation 1 will have only two unknowns as in (3).

$$\overline{V}_r^1 T_s = \overline{V}_x^1 T_x + \overline{V}_y^1 T_y \qquad (3)$$

The T_x, T_y and T_z are computed using (4),(5) and (6).

$$V_r^1\alpha T_s = \overline{V}_x^1\alpha T_x + \overline{V}_y^1\alpha T_y \qquad (4)$$

$$\overline{V}_r^1\beta T_s = \overline{V}_x^1\beta T_x + \overline{V}_y^1\beta T_y \qquad (5)$$

$$T_z = T_s - T_x - T_y \qquad (6).$$

A. *Space Vector Approach to Synchronization and Symmetry*

The pivot vectors can he synthesized by two inverter states, $\overline{V}_{zx}$ and $\overline{V}_{zy}$ as given in Table II. Switching sequence using all the four space vectors, $\overline{V}_{zx} \Leftrightarrow \overline{V}_x \Leftrightarrow \overline{V}_y \Leftrightarrow \overline{V}_{zy}$ can he generated, where T_z interval **is** equally split between $\overline{V}_{zx}$ and $\overline{V}_{zy}$. **In** order to maintain minimum switching frequency the sequences must satisfy following two conditions.

- Condition 1: Only one switch is switched during state transition. That is transition from state 1 to state -1 and vice versa is not allowed.
- Condition 2: The final state of present sample will he the initial state of next sample.

At low switching frequencies, it **is** necessary to maintain perfect synchronization of inverter output voltage with respect to its own fundamental to avoid sub harmonics. The three-phase symmetry will ensure that all the harmonics and the fundamental of all the three phases will he perfectly balanced. So the triplen harmonics will he cancelled from the line voltage. The half wave symmetry will ensure elimination of even harmonics from the output voltage. The conditions of waveform symmetry for a given sample ***k*,** are given in first row of the Table III. The necessary and sufficient conditions in terms of the inverter states to achieve synchronization and symmetry at the line and pole voltages are given in the second row of Table III. In table III, θ is any arbitrary angle measured from the ***a*** axis and the states $S_a^1 S_b^1 S_c^1$ indicate the complementary states of $S_a S_b S_c$ (Complementary state of 1 is state -1 and vice versa and complementary state of 0 is state 0). The consideration of symmetry demands that there should he integral number of samples N, in each sector of 60 degrees duration and these samples should he positioned at identical intervals at each sector. If N is odd, then the N^{th} sample will be on the sector boundary and all other *N-1* samples are placed at an interval of $\Delta\theta = \frac{\pi/3}{N}$ in a sector. All the samples except the sample during sector change over will have the sequence $\overline{V}_{zx} \rightarrow \overline{V}_x \rightarrow \overline{V}_y \rightarrow \overline{V}_{zy}$ or $\overline{V}_{zy} \rightarrow \overline{V}_y \rightarrow \overline{V}_x \rightarrow \overline{V}_{zx}$ alternatively.

TABLE III.
CONDITIONS FOR HWS, TPS AND SYNCHRONIZATION

	θ	$\theta \pm 360$ (Synchronization)	$\theta \pm 180$ HWS	$\theta + 120$ TPS	$\theta + 240$ TPS
1	***va***	***va***	***-va***	***vc***	***vb***
	vb	***vb***	***-vb***	***va***	***vc***
	vc	***vc***	***-vc***	***vb***	***vo***
2	Sa	Sa	S^1a	SC	Sb
	Sh	Sh	S^1b	Sa	s c

During sector change over, the pivot vector $\overline{V}_z$ has to he changed accordingly. If N is odd, the N^{th} sample will have sequences $\overline{V}_{zx} \Leftrightarrow \overline{V}_x \Leftrightarrow \overline{V}_y \Leftrightarrow \overline{V}_{zy} \Leftrightarrow \overline{V}_y$ or $\overline{V}_{zx} \Leftrightarrow \overline{V}_x \Leftrightarrow \overline{V}_y$. The former will result in pulse number of $p = (3N+1)/2$ and the latter will result in $p = (3N-1)/2$. So for odd values of *N=1,3,5...*, ***p*** will take values 2,5,8... or 1,4,7.... If N is even then there will not he sample on sector boundary and the first and last sample in a sector will have the sequences $\overline{V}_{zx} \Leftrightarrow \overline{V}_x \Leftrightarrow \overline{V}_y \Leftrightarrow \overline{V}_x$. For even values of N, p is given by $p = (3N)/2$. So for *N*= 2,4,6..., ***p*** will take values 3, 6, 9, ... Hence for any integer value of pulse number ***p*,** synchronization and QWS, HWS and TPS will he maintained. So the switching frequency variation in variable frequency drives is small and will result in smooth operation of the drive. This is a significant improvement over synchronized SPWM, where ***p*** must be odd multiple of 3 to avoid odd harmonics and triplen harmonics from the line voltage.

B. *Implementation*

The reference vector is sampled at $T_s = 1/(f_1 * 6 * N)$ and it decides the sector *Z*. Once *Z* is known then the sample can be mapped to $\overline{V}_r^1$ as explained above. Also the *Z* will decide the starting vector $\overline{V}_z$. The information on N (*N* is odd or even) will decide the sequence. An interesting feature of this PWM technique is that the output waveforms will have QWS, that is, $v_a(\theta_a + \theta) = v_a(\theta_a - \theta)$ $v_b(\theta_b + \theta) = v_b(\theta_b - \theta)$ and $v_c(\theta_c + \theta) = v_c(\theta_c - \theta)$, where θ_a, θ_b and θ_c are the angles for which the phase voltages v_a, v_b and v_c are at peak values. This is because the switching sequences satisfy the following condition of QWS, $S_a(\theta_a + \theta) = S_a(\theta_a - \theta)$, $S_b(\theta_b + \theta) = S_b(\theta_b - \theta)$ and $S_c(\theta_c + \theta) = S_c(\theta_c - \theta)$.

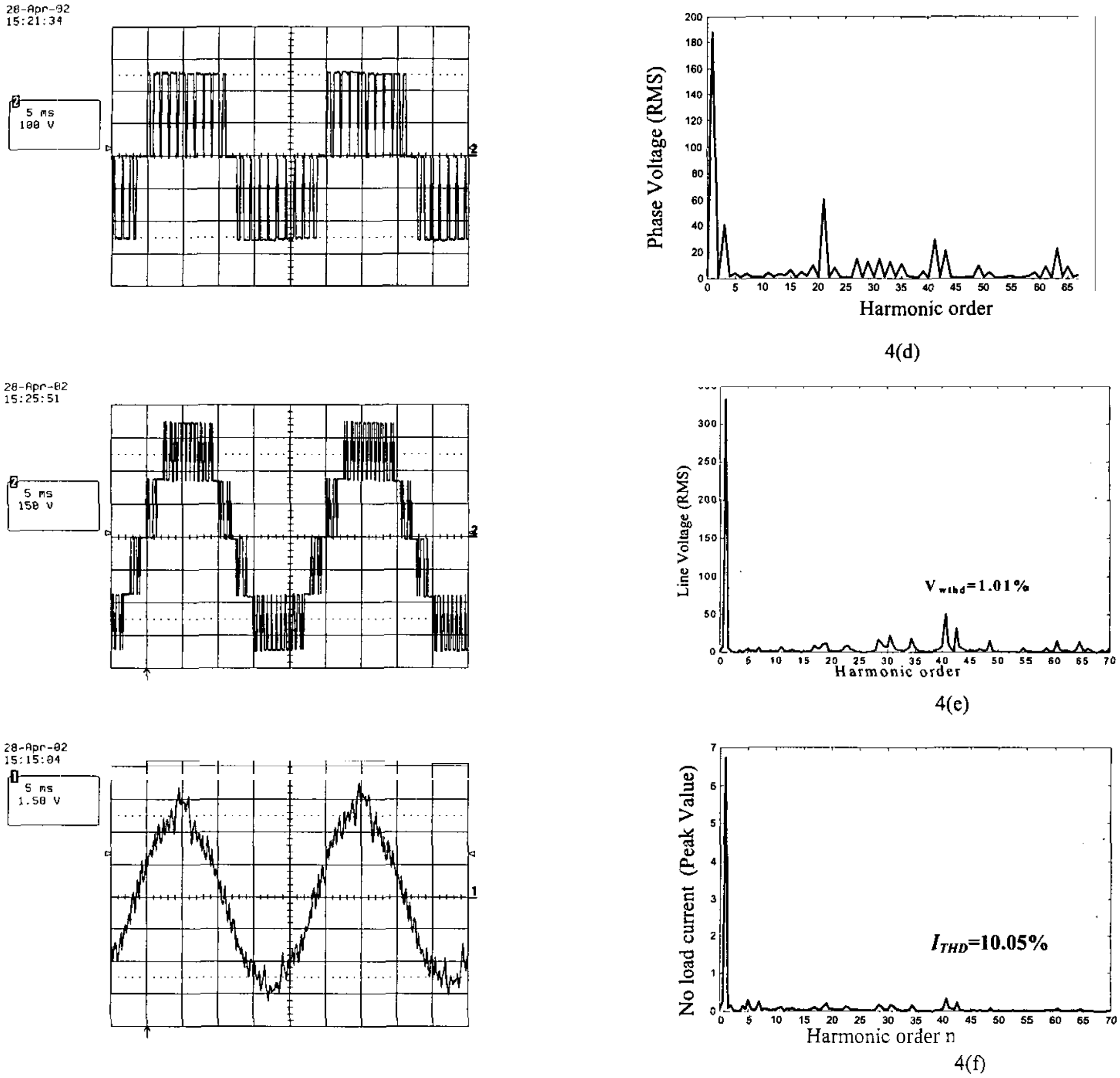


Fig .4. Experimental waveforms: f_1=40Hz, N=7, p=10, f_{sw}=400Hz. V_1 = 320V (a) Pole Voltage (b) Line Voltage (c) No load current of the motor. (Scale: 1V=2.5A) (d) Frequency Spectra of Phase voltage, (e) Frequency Spectra of line voltage and (f) Frequency spectra of no load current of the motor

C. *Self Balancing of D.C. Bus Capacitor Voltages*

Fig. 1 shows the power circuit of three level diode clamp inverter. The D.C. link mid point voltage (v_m) imbalance is decided by the mid point bus current i_m [3][4]. Every sample except the N^{th} sample will switch $\overline{V}_{zx}$ and $\overline{V}_{zy}$ for equal duration of $Tz/2$ seconds. The i_m due to $\overline{V}_{zx}$ is equal and opposite of that of $\overline{V}_{zy}$. So the D.C. link mid point current is cancelled to some extent in every sub cycles. For a given sample k where $k=1,2..N$, the time intervals $T_x(k)$, $T_y(k)$ and $T_z(k)$ of all the sectors will be identical. So the D.C. Link capacitor voltages *are* perfectly balanced over every cycle of the fundamental. It can also be shown that under unity power

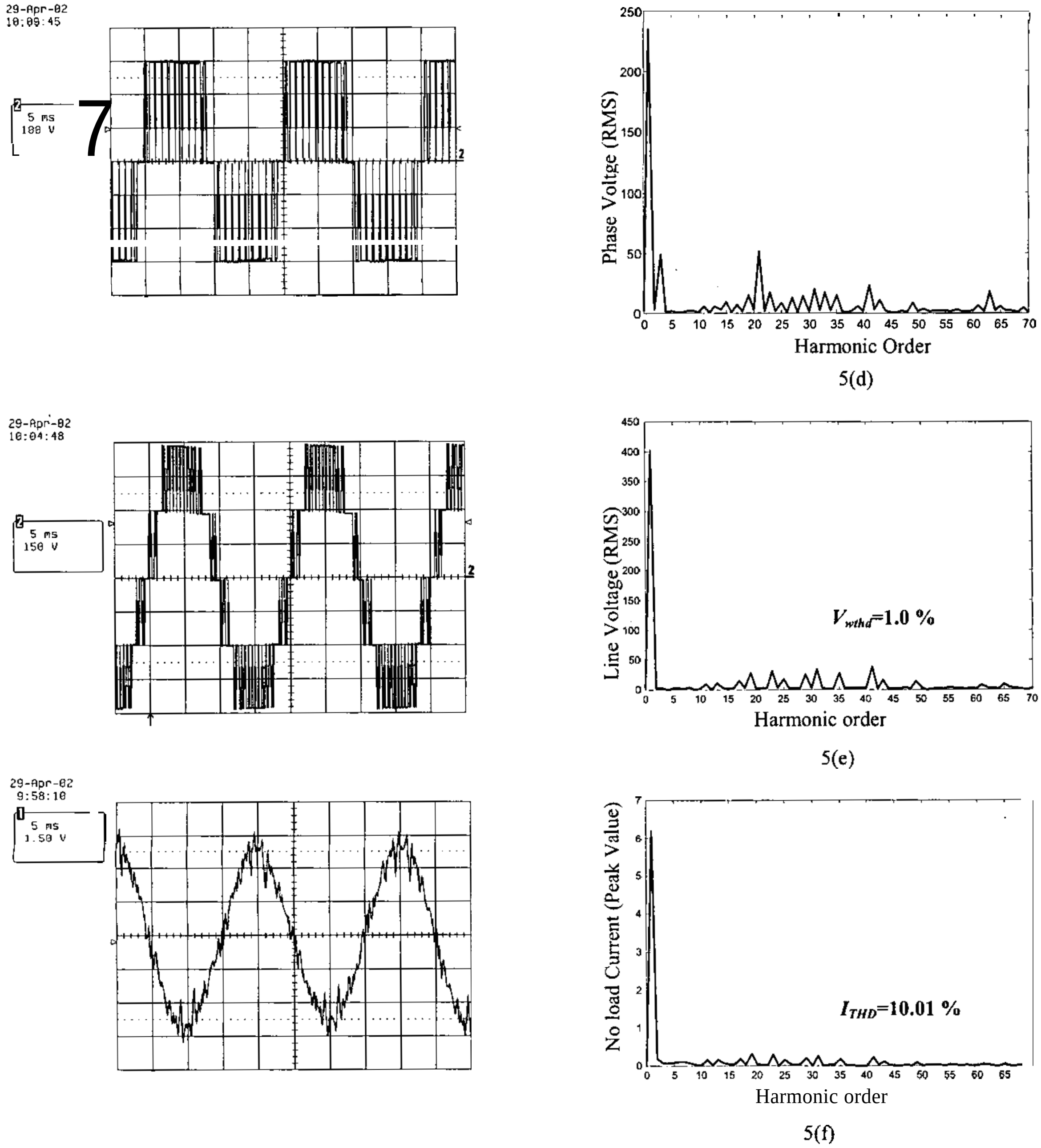


Fig. **5** Experimental Waveforms: f_l=50Hz, N=7, p=10, f_{sw}=500Hz, V_l=400V **(a)** Pole Voltage, **(b)** Line Voltage (c) No load current of the motor (Scale: 1V=2.5A) (d) Frequency spectra of phase voltage (e) Frequency spectra of line voltage (f) Frequency spectra of the no load current of the motor

factor conditions, the D.C. link capacitor voltages are perfectly balanced on every $(1/6)^{th}$ cycle of the fundamental. Hence the D.C. link capacitor voltage balancing is built in to the algorithm and does not require any additional computation as given in [3]. The D.C. link capacitor requirements can be reduced

III. EXPERIMENTAL RESULTS

The proposed algorithm is implemented on TMS 320 F240 fixed point DSP controller. The algorithm is applied to V/f drive consisting of 400V, 10HP induction motor, powered

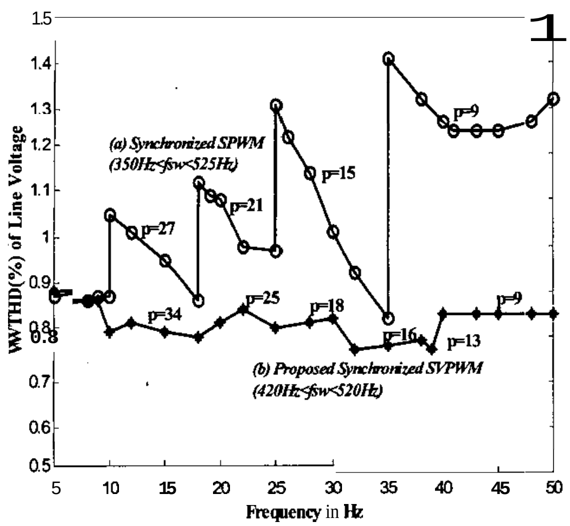


Fig. 6 . V_{wthd} V/S f_l plot.

from a 30KVA, IGBT based three level diode clamp inverter. The D.C. link voltage is maintained at 500V for the linear range of the modulator. The maximum frequency for which the modulator remains in linear range corresponds to f_l = 43.3 Hz. For 50Hz, the D.C. link voltage is maintained at 575V, which will result in fundamental voltage (V_l) of 400V, which corresponds to the highest modulation with linear range. The pole voltage, line voltage and the no load current for f_l=40Hz and 50Hz and their frequency spectra are given in fig. 4 and fig.5 respectively. The I_{THD} is computad from the experimental data and is 10.05% and 10.01% for f_l=40Hz and 50Hz respectively. Similarly the V_{WTHD}, computad from the experimental data for these two conditions is 1.01% and 1.0% respectively. The frequency spectra of the line voltage and current demonstrate the absence of sub-harmonics, even harmonics and triplen harmonics for any integer value of pulse number, *p*.

IV. PERFORMANCE ANALYSIS

In high power drives the total harmonic distortion of the no load current (I_{THD}) of the motor, which is a function of voltage spectra and motor parameters is a suitable performance index at low switching frequencies [1]. I_{THD} is givenhy $I_{THD} = \frac{\sqrt{\Sigma I_n^2}}{I_1}, n \neq 1$, where I_n is the rms value of n[th] harmonic and I_1 is the RMS value of the fundamental component of the no load current of the motor. .Another equivalent quantity, which is a measure of I_{THD} , function of voltage spectra only and independent of load is the V_{WTHD} given by $V_{WTHD} = \frac{\sqrt{\Sigma (Vn/n)^2}}{V_1}, n \neq 1$ [1],[7]. In this paper the proposed synchronized PWM technique and the synchronized SPWM are evaluated in terms of the V_{WTHD}.

The V_{WTHD} is computed from the simulation results for the entire range off, for the proposed method and SPWM. In the case of SPWM synchronization is maintained and pulse number, *p* is odd integral multiple of 3. The plot of V_{WTHD} v/s f_l is given in fig. 6. The proposed method has improved V_{WTHD} compared to that of SPWM for the entire region. This demonstrates the superiority of the proposed method over the SPWM technique in terms of V_{WTHD}.

V. CONCLUSIONS

The theory of the space vector based synchronized PWM method with HWS, QWS and TPS is explained. The experimental results are presented. The proposed algorithm is simple to implement on digital controllers and does not add to any computational complexity. It is shown that the proposed PWM technique will result in balanced D.C. link capacitor voltages. The performance results show that the V_{WTHD} of the proposed method is better compared to that of SPWM technique. The experimental waveforms show QWS, HWS and TPS for any integer value of pulse number. The absence of triplen harmonics from the line voltage shows that the inverter output voltages have three-phase symmetry. Even though the focus is on low switching frequency applications, the proposed technique can be used for high switching frequency applications also.

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