# A Grid Simulator to Evaluate Control Performance of Grid-Connected Inverters

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***Abstract*—Grid simulators are used to test the control performance of grid-connected inverters under a wide range of grid disturbance conditions. In the present work, a three-phase back-to-back connected inverter sharing a common dc bus has been programmed as a grid simulator. Three phase balanced disturbance voltages applied to three-phase balanced loads has been considered in the present work. The developed grid simulator can generate three phase balanced voltage sags, voltage swells, frequency deviations and phase jumps. The grid simulator uses a novel disturbance generation algorithm. The algorithm allows the user to reference the disturbance to any of the three phases at any desired phase angle. Further, the exit of the disturbance condition can be referenced to the desired phase angle of any phase by adjusting the duration of the disturbance. The grid simulator hardware has been tested with different loads – a linear purely resistive load, a non-linear diode-bridge load and a grid-connected inverter load.**

***Index Terms*—grid simulator, power-quality, STATCOM, fault ride-through, programmable voltage source**

## I. Introduction

In recent years, the number and power rating of the converters integrated to the grid are on the rise. This can be attributed to the increasing use of distributed generation units and power quality converters. Both these applications invariably use a grid-connected inverter as an interface to the grid. With the power levels of wind and solar generation units having reached a few MWs and with high power inverters being used to maintain the power quality, a sudden disconnection of these converters due to short time grid disturbances such as voltage sags and voltage swells can cause instability in the grid. To avoid this, additional controls are usually implemented in grid-connected inverters to stay connected to the grid during prescribed depths and durations of voltage sags and voltage swells. To test these controls before commissioning, it is required to re-create short time disturbances like voltage sags and voltage swells in the laboratory. A hardware grid simulator is used for this [1]–[4]. Grid simulators can also help in testing the control performance of other control loops of grid-connected inverters such as the phase-locked loop, current control loop and voltage control loop.

The simulation of grid disturbances in a laboratory environment has been of interest for a long time. However, till very recent times, the interest has primarily been to test for EMI compliance as per the IEC standard IEC 61000-4-34 [5] for electrical equipment connected to the grid. Since the mentioned standards require testing under voltage sags only, most earlier literature limit their focus to voltage sags. All these earlier works use mostly simple passive components [2], [6], [7] to create voltage sags with the exception of [3] which uses a series-injected inverter for the same purpose.

With the distributed generation gaining pace and their power levels reaching a few MWs, research work on grid simulators have become more generic in recent years [1], [4], [7]–[10] and includes generation of a wide range of grid disturbance conditions besides voltage sags. The need to generate a wide range of disturbance conditions has prompted researchers to use IGBT based inverters as the hardware for grid simulators. The topology usually has an active front-end converter that charges the dc bus and an inverter at the output side to generate the required grid disturbances. The bi-directional power flow capability of this topology makes it possible to generate a wide range of grid disturbance conditions in the laboratory. The various methods available in literature [1], [4], [7]–[10] differ primarily in the topology of the front-end converter and the output inverter.

In the present work also, the grid simulator uses an IGBT based three-phase 4-wire voltage source inverter. The topology of the grid simulator has been explored widely in available literature. So, the focus of the present work has been on the disturbance generation algorithm. A novel disturbance generation algorithm has been proposed for the grid simulator. The algorithm allows the user to reference the disturbance to any of the three phases at any desired phase angle. Further, the exit of the disturbance condition can be referenced to the desired phase angle of any phase by adjusting the duration of the disturbance. This helps in testing the equipment under test at any desired point of fault condition. The algorithm has been developed, analysed and implemented using a Finite State Machine (FSM). A Moore Model has been used for the FSM. Three phase balanced disturbances applied to three phase balanced loads has been considered. The grid simulator is capable of simulating three phase balanced voltage sags, voltage swells, frequency deviations and phase jumps. The hardware has been tested with different loads - a linear purely resistive load, a non-linear diode-bridge load and a grid-

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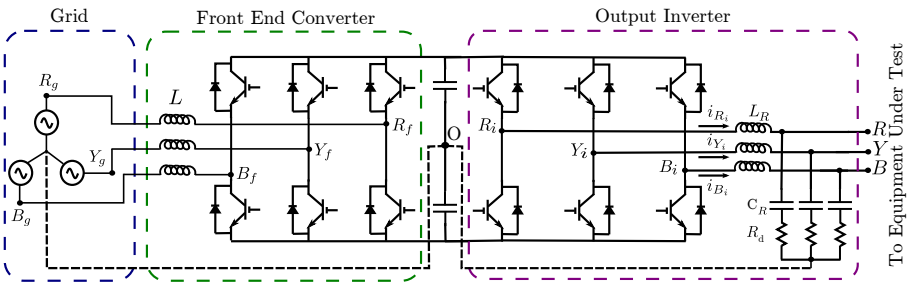


Fig. 1: Topology of the grid simulator.

connected inverter load.

## II. Topology of the Grid Simulator

The grid simulator uses a back-to-back connected inverter topology with a shared dc bus as shown in Fig. 1. The front-end uses a simple inductor as filter while the output uses a LC filter. Both the front-end converter and the output inverter can have a 3-wire configuration shown in solid lines or a 4-wire configuration shown in dashed lines. In the present work, a single-phase configuration has been used in the front-end by utilising only two of the three legs and the output is a three-phase 3-wire configuration. The LC resonance at the output inverter is damped through passive means using 2Ω ($R_d$) resistors connected in series with the output capacitors. The dc bus is maintained at 500 V to produce an output per phase voltage of 120V (rms). The front-end converter ensures a fixed voltage at the common dc bus by drawing real power from the grid while the output inverter is programmed to generate a wide range of grid disturbance conditions. The in-house built hardware is rated at 50kVA for the front-end and output three-phase inverters when operated at a dc bus voltage of 800V with a switching frequency of 10 kHz. However, the converter is operated at a lower power for the present work. The inverter parameters used in the present work have been shown in Table I.

Only three-phase balanced disturbance voltages applied to three-phase balanced loads has been considered in the present work. Hence, the front-end is operated in a single-phase configuration by using two legs of the three-phase front-end converter. The output inverter uses a 3-wire configuration as unbalance conditions has not been considered in this work. The focus of the work has been on the disturbance generation algorithm and hence these simplifications. However, by operating the hardware in three-phase 4-wire configuration in the front-end converter and output inverter sides, the disturbance algorithm algorithm developed in this work can be used for unbalance cases also.

TABLE I: Grid Simulator Ratings

| **Parameter** | **Value** |
|---|---|
| Output Voltage | 120V/phase (rms) |
| Switching Frequency | 10kHz |
| DC Bus | 500V |
| Output Filter Inductor | 5mH |
| Output Filter Capacitance | 3$\mu$F |
| Output Filter Damping Resistance | 2Ω |

## III. Grid Simulator Controls

### A. Front-End Converter(FEC) Control

The FEC locks to the grid using a Synchronous Reference Frame based Phase-Locked Loop (SRF-PLL) [11]. The SRF-PLL requires transformation of the input grid voltage from the stationary reference frame to the synchronous rotating dq frame. For a three-phase configuration, Clarke's and Park's transformations are used to convert the grid voltages to dq frame [12]. For a single-phase configuration, a Second Order Generalised Integrator (SOGI) [13] replaces the Clarke's transformation. The SOGI is used to convert the single phase input grid voltage into orthogonal components to be used for Park's dq transformation. Fig. 2 shows the SRF-PLL control block diagram for the single-phase FEC used in the present work.

Once locked to the grid, the FEC uses an inner current control loop to draw near unity power factor current from the grid. An outer dc bus voltage control loop maintains the dc bus at the required reference voltage. The current loop uses a proportional-resonant (PR) controller in the stationary reference frame for its control. The voltage loop uses a proportional-integral (PI) controller. Fig. 2 shows the FEC inner current control and outer dc bus voltage control block diagrams. The FEC uses sine-triangle modulation at a switching frequency of 10kHz.

In case unbalanced disturbance voltage conditions are to be simulated using a three-phase 4-wire inverter at the grid

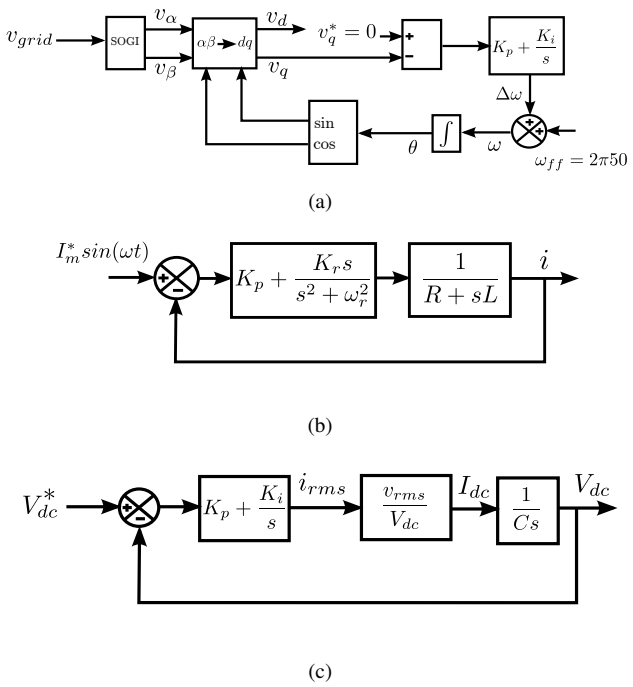


Fig. 2: FEC Controls. (a) Synchronous Reference Frame Phase Locked Loop (SRF-PLL) for single-phase FEC. (b) Inner current loop structure. PR controller is used. It acts directly on the ac current reference. L, R are the filter inductance and the resistance associated with the filter. $\omega_r = 2.\pi.50$ (c) Outer voltage loop structure. PI controller is used. $v_{rms}$ is the rms grid voltage.

simualator output, a single-phase FEC cannot be used. The unbalance condition causes voltage variations between the top and bottom dc bus capacitors. To handle this, a three-phase 4-wire FEC configuration is required. An additional control loop will be required to equalize the capacitor voltages.

### *B. Output Inverter Control*

The output inverter is controlled as an open loop voltage source. The pulse-width modulation signals are generated from the three-phase nominal and disturbance voltage references using sine-triangle modulation at a switching frequency of 10kHz. The disturbance voltage references are generated using the disturbance voltage generation algorithm explained in Section V.

## IV. Grid Simulator Operation

A proper start-up sequence is required to ensure that the grid simulator reaches a steady operation smoothly. The disturbance generation at the output inverter also requires a well-defined sequence of operation. Section IV-A and Section IV-B explain the sequence of operation of the grid simulator and the different modes involved in the generation of voltage disturbance.

### *A. Start-Up Sequence of Grid Simulator*

The following is the start-up sequence of operation of the grid simulator once the input power is switched on:

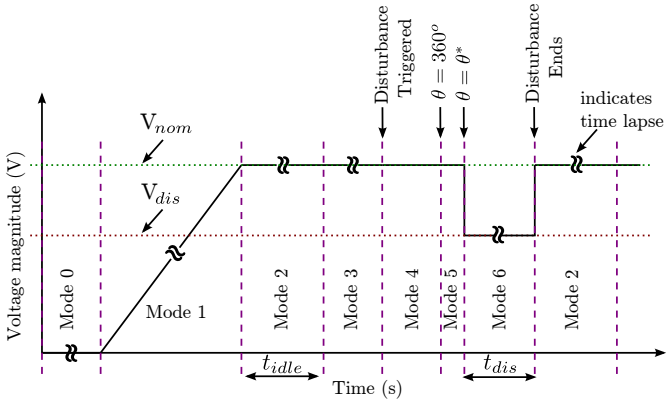


Fig. 3: Grid Simulator modes during voltage disturbance generation. $t_{idle}$ is the duration of idle state between successive disturbances, $t_{dis}$ is the time duration of the voltage disturbance. $V_{nom}$, $V_{dis}$ indicate the nominal and disturbance voltage magnitudes.

1) The anti-parallel diodes in the FEC act as a single phase diode bridge rectifier and charge the dc bus capacitor towards voltage $V_1$. $V_1$ corresponds to the single-phase diode bridge output voltage. A resistor is connected in series with the filter inductor L when the dc bus starts to charge. A contactor shorts out the resistor as the dc bus reaches $V_1$. This ensures that the there are no current spikes due to sudden charging of dc bus capacitor. The current control, dc bus voltage control and the output inverter controls are not activated during this period. The gate pulses to both the inverters are withheld through software.
2) When the anti-parallel diodes are charging the dc bus capacitor, the PLL control starts and locks the inverter to the grid frequency and phase.
3) Once the dc bus is charged to $V_1$, a toggle switch is used to start the current and voltage loops of the FEC. The toggle switch action can be automated. The output inverter controls still remain deactivated. The FEC controls boost the voltage from $V_1$ to the set reference voltage, $V_{dc}^*$.
4) Once the dc bus voltage stabilises at $V_{dc}^*$, the output inverter control is activated using a press button switch. This slowly ramps up the voltage at the ac terminals of the output inverter to the nominal value. This ensures that there are no current spikes or oscillations due to sudden charging of the output LC filter.

### *B. Modes during Disturbance Generation*

Fig. 3 shows the different modes involved in the disturbance voltage generation at the ac terminals of the output inverter including the start-up voltage ramp-up. The voltage magnitude versus time plot has been drawn assuming the disturbance is a three-phase balanced voltage sag. However, the different modes shown are equally applicable to the other types of disturbances also. The different modes are as follows:

**Mode 0: No output voltage**

During this mode, the input power to the grid simulator has been switched on and the grid simulator is going through its start-up sequence to boost the dc bus voltage to the set reference, $V_{dc}^{*}$. The grid simulator output voltage is withheld during this mode as explained in Section IV-A.

**Mode 1: Voltage ramp-up**

This mode is entered by activating a press button switch after ensuring that the dc bus voltage has stabilised at $V_{dc}^{*}$. On pressing the switch, the output voltage of the grid simulator ramps up slowly to the nominal value. The ramp up time is programmable.

**Mode 2: Wait state between disturbances**

This mode is entered once the output voltage is ramped up to the nominal value. The grid simulator enters into a wait state for a set interval of time. During the wait state, the disturbance event cannot be triggered. The grid simulator has been programmed to re-create a disturbance any number of times to allow the user to repeat the test to study different control behaviour of the equipment under test without having to restart the grid simulator. Since the same press button switch is used to create the disturbance several times, a wait time is provided between successive disturbances so as to avoid false triggers.

**Mode 3: Ready state**

This mode is entered once the wait time between successive faults elapses. The output voltage remains at the nominal value. The grid simulator is ready to service any disturbance trigger input. The ready state is exited on triggering a disturbance using the press button switch.

**Mode 4: Wait state for end of current cycle of reference phase**

This mode is entered on receiving the trigger to start the disturbance. The algorithm waits for the end of the current cycle of the reference phase so that the disturbance can be started at the required phase angle in the new cycle. The output ac voltage is at its nominal value during this mode.

**Mode 5: Wait state for desired phase angle in new cycle**

This mode is entered on the completion of the current cycle of the reference phase after the disturbance is triggered using the press button switch. The algorithm monitors the phase angle of the reference phase during this mode. The mode ends when the desired phase angle, $\theta^{*}$ is reached. The output ac voltage is at its nominal value during this mode.

**Mode 6: Disturbance state**

This mode is entered on the phase angle of the reference phase reaching the desired value. The disturbance voltage appears at the output ac terminals during this mode. The three phase disturbance voltage magnitude, frequency and starting phase are programmable. Magnitude setting helps create a sag or swell, frequency deviations are created by adjusting the frequency setting, starting phase can be used to create phase jumps. A combination of different settings can help create a wide range of disturbance conditions. The duration of this mode is programmable. By adjusting the duration of the disturbance, the user can choose to reference the disturbance exit to the required phase angle of any desired phase. At the end of this mode, the ac output voltage returns to the nominal value. The initial phase angle after exit of the disturbance is programmable. This helps set any end point of fault conditions. The disturbance algorithm can include unbalance conditions also as the individual phase magnitudes, frequency and phase angles are programmable. However, in the present work only balanced conditions have been considered as the focus of the work is primarily on the disturbance generation algorithm rather than the disturbances that can be created.

## V. Voltage Disturbance Generation Algorithm

TABLE II: Description of States of the FSM

| State | Description | Corresponding Mode |
|---|---|---|
| State 1 (S1) | Grid simulator output voltage is at its nominal value and awaits a disturbance trigger input. | Mode 3 |
| State 2 (S2) | Grid simulator waits for the current cycle of the reference phase to end ($\theta = 360^{o}$). | Mode 4 |
| State 3 (S3) | Grid simulator waits for the desired phase angle ($\theta = \theta^{*}$) to be reached for the reference phase. | Mode 5 |
| State 4 (S4) | Disturbance voltage is created at the output. | Mode 6 |
| State 5 (S5) | Grid simulator is idle. No disturbance can be triggered. | Mode 2 |

Fig. 4 shows the Moore Model based Finite State Machine (FSM) [14] of the voltage disturbance generation algorithm for a chosen reference phase. In a FSM, 'states' describe 'events'. Different 'inputs' act as 'triggers' and cause control to be tranferred from one state to another. The control transfer is called a 'transition'. The different states involved in the disturbance generation algorithm are listed in Table II and the various input triggers are listed in Table III. A physical press button switch acts as one trigger input (A) and the phase angle of the reference phase acts as another trigger input (BC). In Fig. 4, combinations 000 to 111 indicate the value of 'ABC'. In some states, the time durations ($t_{dis}$, $t_{idle}$) are also used as triggers for transition to a different state. The FSM is the same for any referenced phase. Only the combination 'BC' in Table III varies with the referenced phase.

The FSM conveys the same idea as Fig. 3 but brings better clarity into implementation of the algorithm. The use of input trigger ensures that the algorithm is tested for all possible combination of triggers, thus avoiding any mal-operation due to unexpected input conditions. The FSM can be understood by

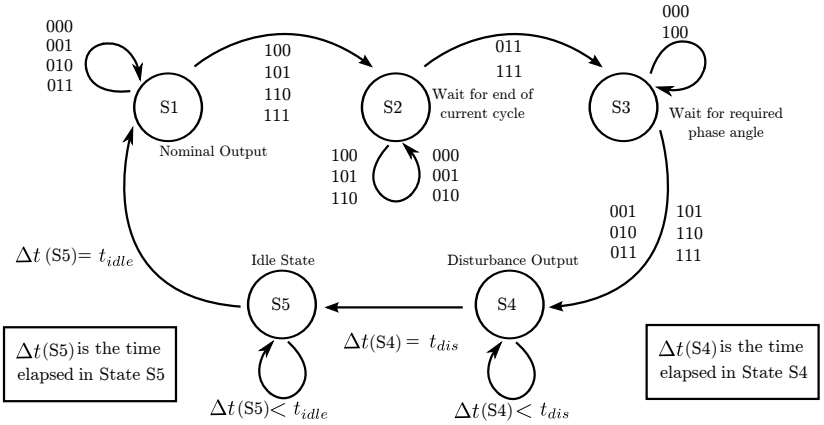


Fig. 4: Moore model based finite state machine for the voltage disturbance generation algorithm. The FSM assumes that the voltage disturbance has already been referenced to a chosen phase.

TABLE III: Trigger Inputs used for Initiating Emulation of Grid Disturbance Voltage

| **Press Button Switch Status** | |
|---|---|
| **Combination (A)** | **Status** |
| 0 | The press button switch has not been pressed |
| 1 | The press button switch has been pressed |
| **Phase angle of reference phase** | |
| **Combination (BC)** | **Status** |
| 00 | $0^o < \theta < \theta^*$ |
| 01 | $\theta = \theta^*$ |
| 10 | $\theta^* < \theta < 360^o$ |
| 11 | $\theta \geq 360^o$ |
| **Time duration of disturbance** | |
| $t_{dis}$ | Indicates the duration of disturbance. |
| **Time duration of idle state** | |
| $t_{idle}$ | Indicates the duration of idle state between successive disturbances. |

comparing the different states with Modes 2 to 6 discussed in the previous section. The modes corresponding to the different states are listed in Table II. The FSM has been drawn assuming a reference phase to have been chosen already. For different selections of reference phase, only the phase angle used for generating trigger combinations 'BC' will change.

## VI. Experimental Results

Fig. 5 shows the response of a non-linear three-phase diode-bridge rectifier load to a voltage sag disturbance. The R-phase voltage and current has been shown. The 470$\mu$F output filter capacitor used in the diode-bridge rectifier can be observed to cause zero current at the start of the disturbance. It also causes a peaky current at the exit of the disturbance condition as shown.

Fig. 6 shows the response of the PLL to a step change in grid frequency. The PLL tracks the frequency in less than 50ms as expected by the PLL design. The disturbance frequency has been intentionally set high for the purpose of clarity.

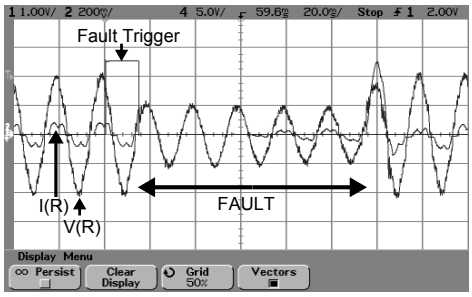


Fig. 5: Response of a three-phase diode bridge rectifier to a 50% voltage sag for 5 cycles. Voltage: 80V/div, Current: 5A/div.

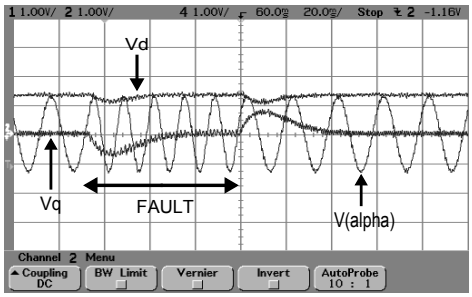


Fig. 6: Step response of synchronous reference frame PLL of a grid-connected inverter to a change in frequency from 50 Hz to 75 Hz. $v_d$, $v_q$, $v_\alpha$: 200V/div.

Fig. 7 captures the current loop response of a grid-connected STATCOM. The reference current can be observed to be tracked within a quarter of a cycle. The saturation of the control voltage can also be observed. This shows that the available control voltage limits the controller response.

Fig. 8 shows the fault ride through of a STATCOM under a 15 cycle voltage sag referenced to R-phase at $30^o$. The ability of the grid simulator to produce sags and handle an inverter load has been shown.

Fig. 9 shows a more severe fault ride through of a STATCOM under a 15 cycle voltage sag referenced to R-phase at $30^o$. At very low voltages the PLL of the STATCOM

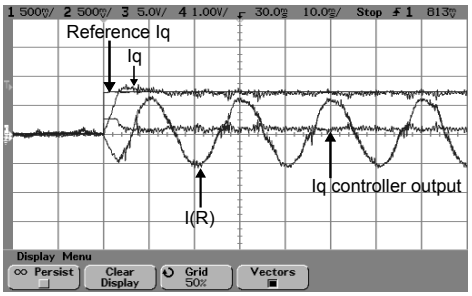


Fig. 7: Step response of STATCOM current loop. The control has been implemented in the synchronous (dq) reference frame. Control Voltage: 200V/div, Current: 6A/div.

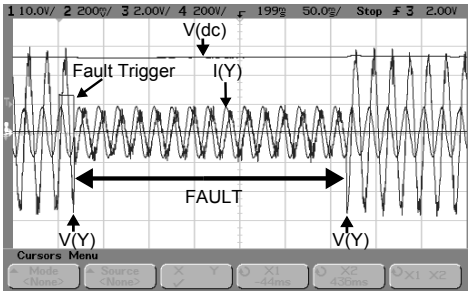


Fig. 8: Voltage sag ride-through of a STATCOM for a $80\%$ voltage sag. The STATCOM control has been implemented in the synchronous (dq) reference frame. $V_Y$: 80V/div, $i_Y$: 10A/div, $V(dc)$ is dc bus of STATCOM: 200V/div.

fails and leads to distortion in the fundamental frequency of the current produced by the STATCOM. The dc bus of the STATCOM starts reducing as a result. This eventually leads to a current trip in the STATCOM when nominal voltages have been restored by the grid simulator. The grid simulator robustness to handle test inverter failure is demonstrated.

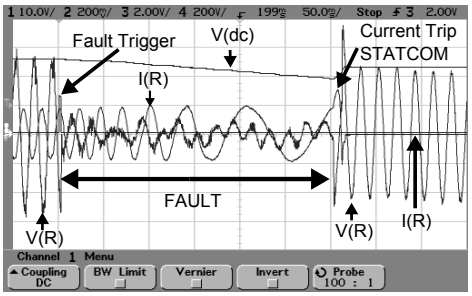


Fig. 9: Voltage sag ride-through of a STATCOM for a $90\%$ voltage sag. The STATCOM control has been implemented in the synchronous (dq) reference frame. $V_R$: 80V/div, $i_R$: 10A/div, $V(dc)$ is dc bus of STATCOM: 200V/div.

The experimental results show the usefulness of the grid simulator to evaluate the control performance of grid-connected inverters. It also demonstrates some of the features of the grid simulator like producing grid disturbances and determining the boundary conditions where the test inverter functionality is lost.

## VII. Conclusion

A grid simulator is designed to test the control performance of grid-connected inverters under different balanced grid disturbance conditions. The grid simulator uses a back-to-back inverter topology to generate voltage sags, voltage swells, frequency deviations and phase jumps. A novel command generation algorithm based on Finite State Machine model has been proposed to generate the disturbances. The algorithm helps provide reference for the disturbance voltage to be created with respect to any phase angle of desired phase at both the entry and exit of the disturbance voltage condition. Experimental results on linear, non-linear and inverter loads have been provided to substantiate the operation of the grid simulator using the developed algorithm.

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