Study on the Effect of Dead Time and its Compensation for Bus-Clamping PWM Techniques

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***Abstract*—Dead-time is provided in between the gating signals of the top and bottom semiconductor switches in an inverter leg to prevent the shorting of DC bus. Due to this dead time, there is a significant unwanted change in the output voltage of the inverter. The effect is different for different pulse width modulation (PWM) methodologies. The effect of dead-time on the output fundamental voltage is studied theoretically as well as experimentally for bus-clamping PWM methodologies. Further, experimental observations on the effectiveness of dead-time compensation are presented.**

***Keywords*— Bus-clamping PWM, discontinuous PWM, dead-time, dead-time compensation, fundamental error voltage, pulse width modulation, voltage source inverter.**

I. INTRODUCTION

Now a days, voltage source inverters (VSIs) are very popular and are used extensively in the fields of AC motor drives, uninterrupted power supplies (UPS), electric vehicles, induction heating and active power filters [1], [2], [3]. A three-phase VSI is shown in Fig. 1.

Pulse width modulated inverters switch at frequencies much higher than the modulation frequency to produce the desired output voltage. Due to non-ideal nature of power semiconductor devices, dead-time is provided between the gating signals of top and bottom switches in each leg to prevent shorting of DC bus. But this has a negative effect on the quality of the output voltage waveform [4]-[8].

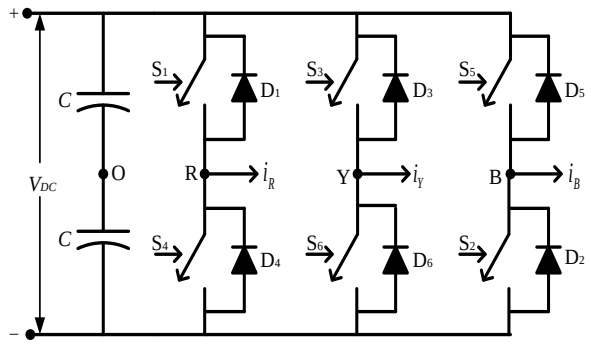


Fig. 1. Three –phase voltage source inverter.

In literature, the effect of dead-time has been studied primarily for continuous pulse width modulation (PWM) schemes such as sine-triangle PWM scheme (STPWM) and conventional space vector PWM scheme (CSVPWM) [4], [5], [6]. Limited theoretical study has been presented for a few other PWM schemes like bus-clamping PWM and advanced bus-clamping PWM schemes [7], [8], [9].

This paper presents a detailed study of dead-time effect on the inverter output voltage for bus-clamping PWM (BCPWM) schemes theoretically as well as experimentally. The BCPWM methods are compared with CSVPWM in terms of their dead-time effects. The experimental results are presented on a 1kVA MOSFET-based inverter. Further, experimental results are presented, demonstrating the effectiveness of a dead-time compensation circuit based on pulse-by-pulse correction.

II. DEAD TIME EFFECT FOR CSVPWM SCHEME

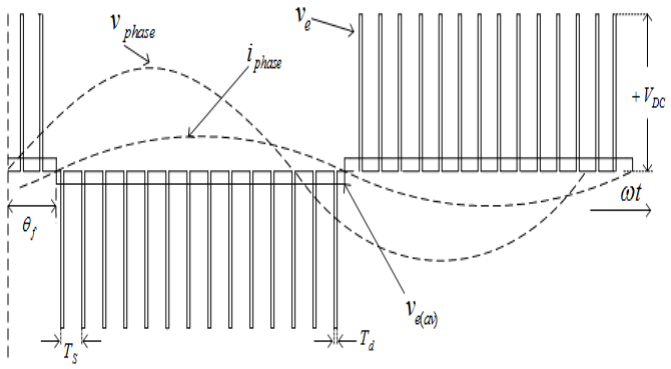
Dead-time (T_d) is provided at each rising edge of gate pulses. During the dead-time, the gate signals of both power devices (S_1, S_4 for R-phase; S_3, S_6 for Y-phase; and S_5, S_2 for B-phase in Fig. 1) in an inverter leg are low. Hence the load current (i_R for R-phase; i_Y for Y-phase; and i_B for B-phase in Fig.1) is conducted by an anti-parallel diode (D_1 or D_4 for R-phase; D_3 or D_6 for Y-phase; and D_5 or D_2 for B-phase in Fig. 1). As a result, there is certain amount of voltage loss/gain in each carrier period (T_s) [4]-[8].

It is observed that the effect of dead time depends on the load current polarity. When the load current is positive, the effect of dead time is negative, and *vice versa* [4]-[12]. The dead-time effect over a line cycle for CSVPWM is shown in Fig. 2(a). The error voltage (v_e) is found by subtracting the ideal pole voltage from the actual pole voltage. The average error voltage ($v_{e(av)}$) is a square wave over the line cycle, which is shown in Fig. 2(b). The fundamental current waveform is also shown in the same figure. The amplitude (h) of this square wave is given by (1a), where V_{DC} is the DC bus voltage and f_c is the carrier frequency. The R.M.S. value of the fundamental component of the square wave (V_{e1}) can be expressed as shown in (1b). This error voltage (V_{e1}) gets added phasorially to the ideal phase voltage (V_p) as illustrated in Fig. 2(c). The RMS value of the resultant (actual) phase voltage is given by (1c). The amplitude of fundamental error voltage is independent of load power factor angle (θ_f) as seen from (1b). However, the amplitude of the resultant phase voltage depends on the load power factor angle (θ_f) as seen from (1c) and Fig. 2(c).

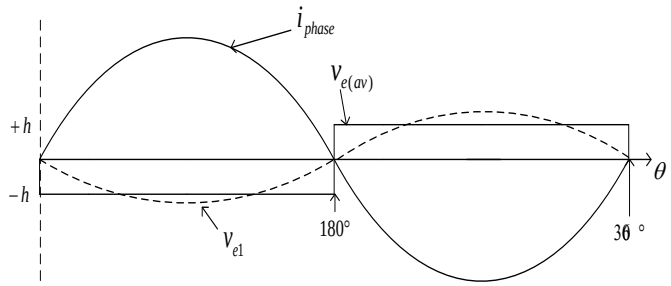
$$h = V_{DC}\frac{T_d}{T_S} = V_{DC}\,T_d\,f_{sw} \quad (1a)$$

$$V_{e1} = \frac{2\sqrt{2}h}{\pi} \quad (1b)$$

$$V_{PDT} = \sqrt{V_p^{\,2} + V_{e1}^{\,2} + 2V_p V_{e1}\cos(180^0 - \theta_f)} \quad (1c)$$



(a)



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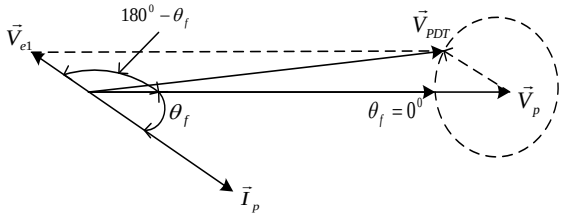
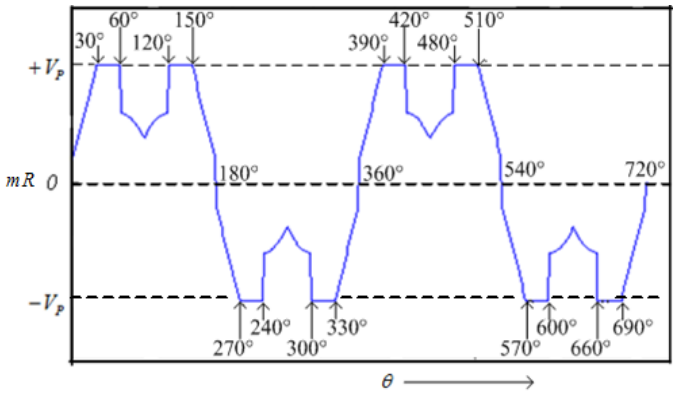


(c)

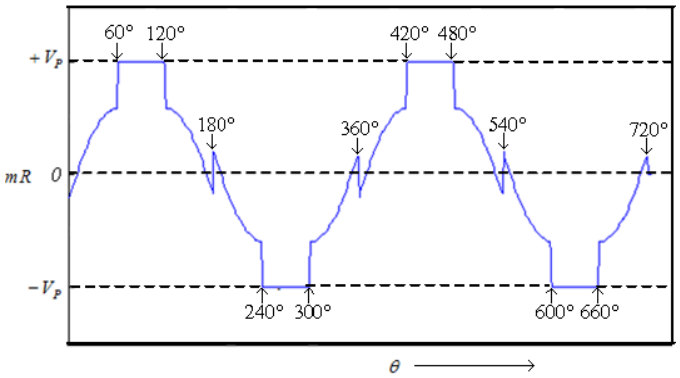
Fig. 2. (a) Dead-time effect over a line cycle, (b) average error voltage with respect to the fundamental current waveform, (c) phasor diagram illustrating dead-time effect for CSVPWM scheme.

III. Dead-Time Effect for Bus-Clamping PWM Schemes

The modulating signals corresponding to two BCPWM schemes, namely 30° bus-clamping PWM (30°BCPWM) and 60° bus-clamping PWM (60°BCPWM), are presented in Fig. 3(a) and 3(b), respectively. The two methods are studied in terms of their dead-time effects.



(a)

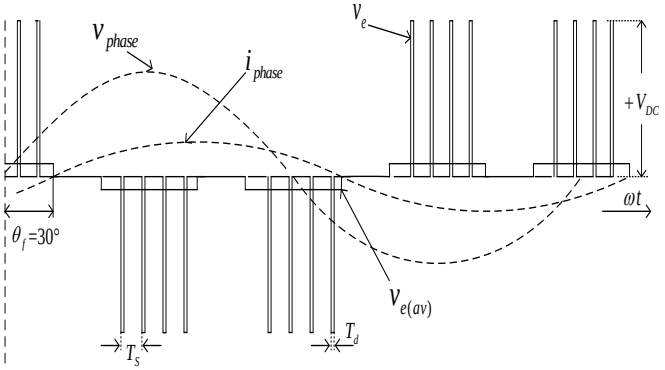


(b)

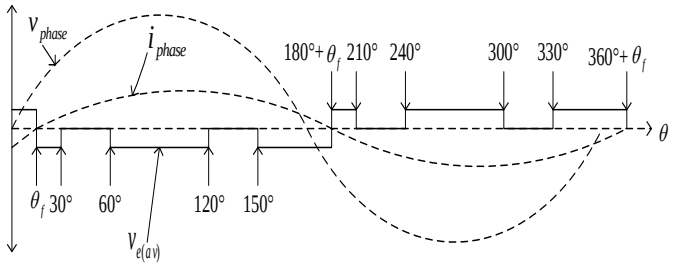
Fig. 3. R-phase modulating signals (*mR*) for (a) 30°BCPWM and (b)60°BCPWM schemes.

A. *30° Bus-clamping PWM scheme (30°BCPWM)*

In 30°BCPWM scheme, each phase of VSI is clamped to one of the DC bus terminals in the middle 30° duration of each quarter of the fundamental cycle [7], [8], [9]. In the duration of the clamping, there is no switching of power devices in the given leg. Hence dead-time effect is zero during the clamping duration. The average error voltage is also zero in the clamping intervals. In the other intervals, this is equal to $+h$ for negative current, and $-h$ for positive current. Fig. 4(a) illustrates the instantaneous and average error voltages (v_e and $v_{e(av)}$) over a line cycle for power factor 0.866 lagging. As the power factor changes, the waveshape of average error voltage also changes.



(a)



(b)

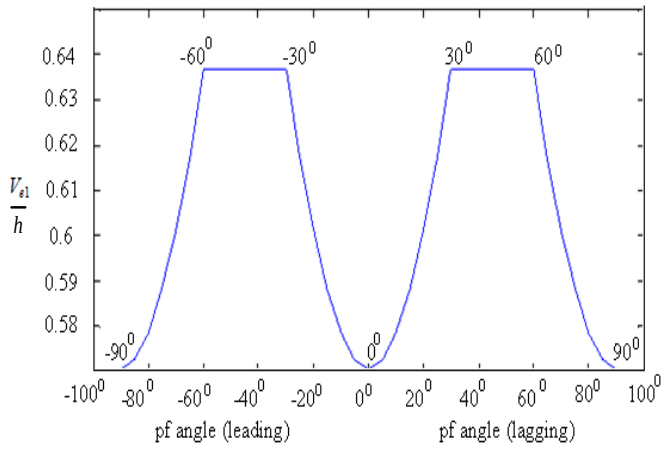
Fig. 4. (a) Instantaneous error voltage for θ_f=30° and (b) average error voltage for 0° ≤ θ_f ≤ 30° with 30°BCPWM.

The average error voltage for a power factor angle between 0° and 30° (lagging) is illustrated in Fig. 4(b). The amplitude (RMS value) and the phase of the fundamental error voltage for this waveform can be expressed as-

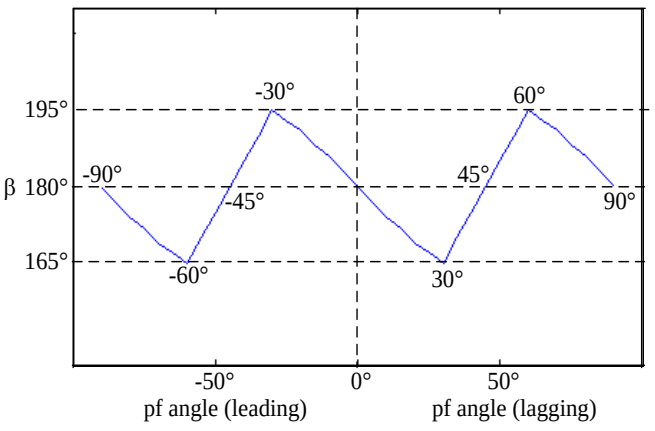
$$V_{e1} = \frac{\sqrt{2}h}{\pi}[\sqrt{4.535 - 2.928\cos\theta_f}] \qquad (2a)$$

$$\beta = 180^0 - \tan^{-1}[\frac{0.366\sin\theta_f}{1-0.366\cos\theta_f}] \qquad (2b)$$

It may be noted that the phase β is measured with respect to the fundamental current.



(a)



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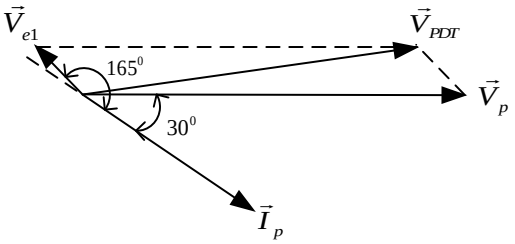


(c)

Fig. 5. (a) Magnitude and (b) phase of fundamental error voltage for different ranges of power factor angles (c) Phasor diagram illustrating dead time effect for 30°BCPWM (V_{e1}=0.6365V, β=165°)

For other ranges of power factor angle V_{e1} and β are evaluated in similar fashion. The RMS value (normalized with respect to h) and the phase of the fundamental error voltage vary with power factor (pf) as shown plotted in the Fig. 5(a) and 5(b), respectively. V_{e1} remains constant for power factor angles between 30° and 60° as seen from Fig. 5(a). As shown by Fig. 5(b), the phase β varies around 180° , while β is always equal to 180° in case of CSVPWM scheme.

The magnitude and phase of the phase voltage get modified due to the dead time effect as seen from the phasor diagram in Fig. 5(c).

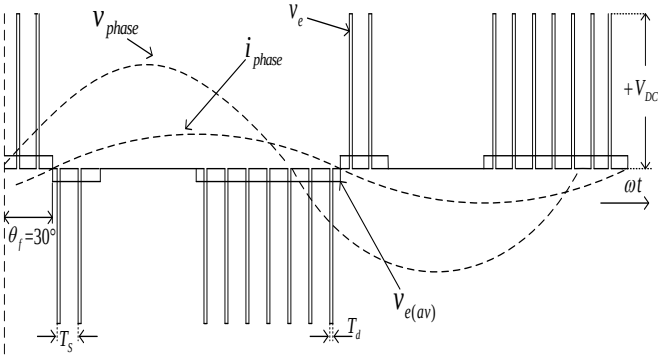
B. *60° Bus-clamping PWM scheme (60°BCPWM)*

In case of 60°BCPWM scheme, each phase is clamped to one of the DC bus terminals during the middle 60°duration of each half cycle of its fundamental voltage [7], [8], [9]. Dead-time effect in case of 60°BCPWM can be analysed in a fashion similar to that of 30°BCPWM.

The instantaneous and average error voltages are shown in Fig. 6(a). Fig. 6(b) shows the average error voltage for a power factor angle between 0° and 60° lagging. The RMS value and phase of the fundamental error voltage of this waveform are evaluated in the same manner as those for 30°BCPWM. These expressions are given in 3(a) and 3(b) , respectively.

$$V_{e1} = \frac{\sqrt{2}h}{\pi}[\sqrt{5 - 4\cos\theta_f}] \qquad (3a)$$

$$\beta = 180^0 - \tan^{-1}[\frac{\sin\theta_f}{2-\cos\theta_f}] \qquad (3b)$$



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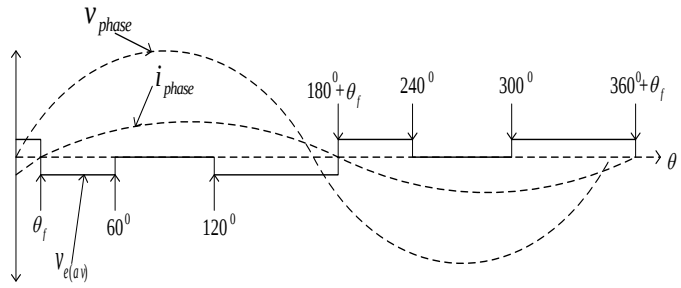
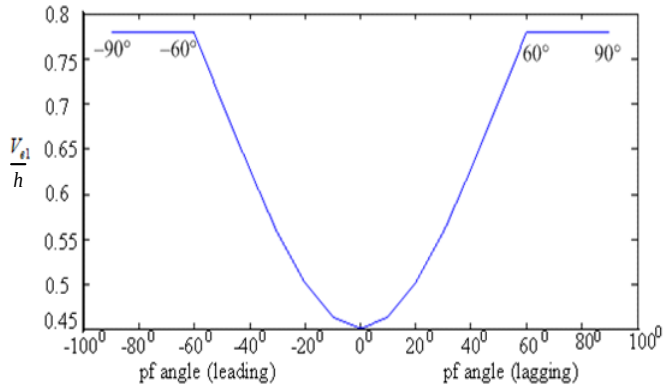


(b)

Fig. 6. (a) Instantaneous error voltage for θ_f=30° and (b) average error voltage for 0° ≤ θ_f ≤ 60° with 60°BCPWM.

The expressions for RMS value and phase of fundamental error voltage (i.e. V_{e1} and β) for other ranges of power factor angle are evaluated in similar way. Fig. 7(a) shows the variation of RMS value (normalized with respect to *h*) of fundamental error voltage with power factor angle. The RMS error voltage remains constant for power factor angles in between 60° and 90° as seen from this figure. The variation of phase angle β with power factor angle is shown in Fig. 7(b). Similar to 30°BCPWM, the phase β varies around 180° over the whole power factor range. The phasor diagram illustrating the dead-time effect on the fundamental phase voltage for 0.866 lagging power factor is shown in Fig. 7(c). The observations are similar to those in case of 30°BCPWM.



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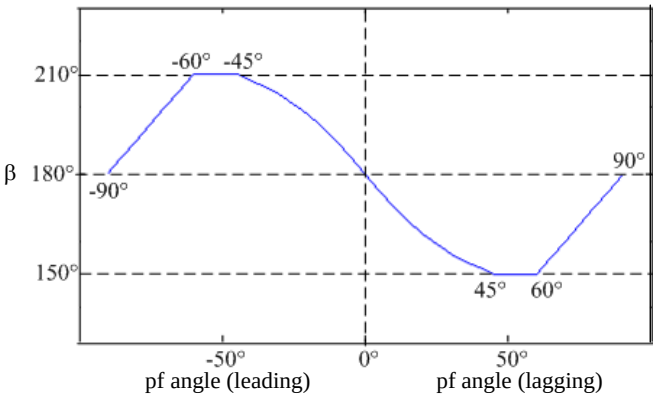

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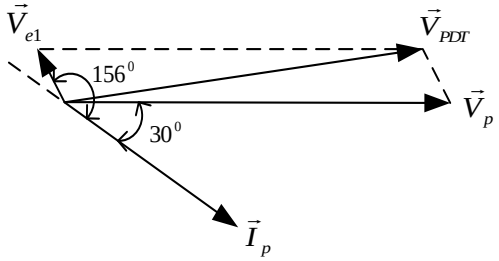


Fig. 7. (a) Magnitude and (b) phase of fundamental error voltage for different ranges of power factor angle (c) Phasor diagram of dead time effect for 60°BCPWM (V_{e1} =0.5578V, β=156°).

C. *Comparison of CSVPWM and BCPWM*

Fig. 8 shows that the normalized R.M.S. fundamental error voltage is independent of power factor angle for CSVPWM scheme. Fig. 5(a) and 7(a) are reproduced here for comparison with CSVPWM. The three methods are compared at the same carrier frequency.

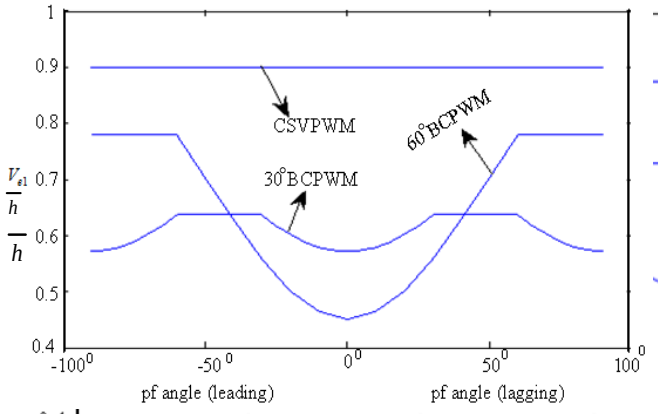


Fig. 8. Comparison of dead- time effect between BCPWM and CSVPWM schemes.

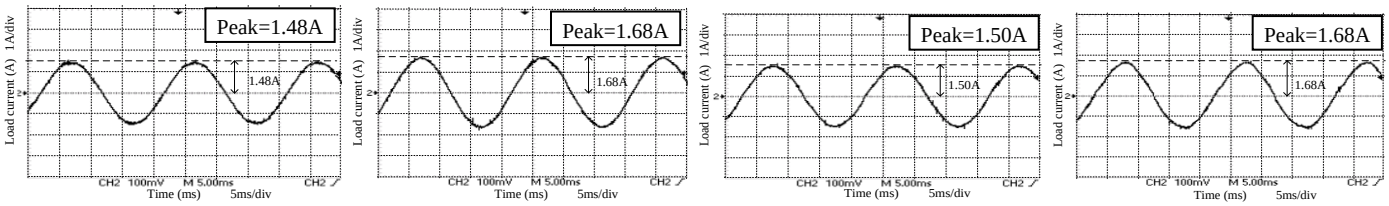
From Fig. 8. it can be concluded that the effect of dead-time is lower in case of BCPWM scheme than in case of CSVPWM scheme at a given carrier frequency. Further, for high power factor loads, the 60°BCPWM scheme is better than 30°BCPWM scheme.

IV. Experimental Results

This section presents experimental results, validating the analysis in the previous section.

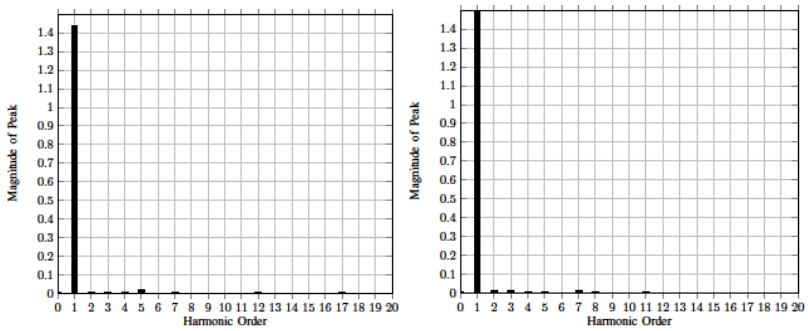
A. *Experimental Set-up*

A 1kVA MOSFET based three-phase two-level VSI is designed, developed and tested successfully to carry out the experimental validation of dead-time effect. The input to the inverter is a single-phase diode bridge rectifier with an inductive AC-side filter and a capacitive DC-side filter. The DC bus to the inverter acts as output capacitive filter to the rectifier. The PWM pulses are generated by DSP processor TMS320LF2407. The control board takes the PWM signals



(a) (b) (c) (d)

Fig. 9. Measured load current - (a) without and (b) with dead-time compensation for 30°BCPWM. (c) without and (d) with dead-time compensation for 60°BCPWM.



(a) (b)

Fig. 10. Harmonic spectra of measured load current - (a) without and (b) with dead-time compensation for 30°BCPWM.

and provides the dead-time before feeding to the power board. The load is considered as R-L type.

Experimental results are presented without and with dead-time compensation. The compensation circuit for dead-time effect is as presented in [10]. It works on the principle of pulse-by-pulse correction. While this compensation circuit is used for sine-triangle PWM in [10], the same is employed for BCPWM methods here.

B. *Measured Current Waveforms*

The load current is measured for an R-L load (R=26.5Ω, L=41mH, resulting in a power factor of 0.9) at a modulation index m=1.0, with V_{DC}=124V, and T_d=3.2μs. The carrier frequency f_c=30 kHz, and the average switching frequency, f_{sw}=20 kHz.

The measured load current waveforms without and with dead-time compensation circuit for 30°BCPWM scheme are shown in Fig. 9(a) and (b), respectively. Since the switching frequency is quite high (20 kHz), the ripple component is negligible in the current waveforms. Further, dead-time compensation improves the distortion around zero-crossing. Also, there is a clear improvement in the peak value of load current.

For 60°BCPWM scheme, the experimental conditions are the same as those for 30°BCPWM scheme as mentioned above. Fig. 9(c) and 9(d) show the measured load current waveforms without and with dead time compensation respectively, for 60°BCPWM scheme. The observations are also similar to those for 30°BCPWM scheme. The fundamental current increases with dead-time compensation as seen from Fig. 9(c) and 9(d).

Fig. 10(a) and 10(b) present the measured harmonic spectra of load current corresponding to 30°BCPWM scheme without and with dead-time compensation, respectively. These spectra confirm the increase in fundamental current with dead-time compensation.

C. *Measured Fundamental Current*

The values of fundamental load current are measured for CSVPWM as well as BCPWM schemes without and with dead-time compensation. The experimental conditions under which the PWM methods are compared are same as those in earlier section except for load and switching frequency. Here the load considered is R=50Ω and L=20mH. The average switching frequencies considered are 3.6, 7, 9, 12, and 15 kHz. The carrier frequency f_c is same as the average switching frequency f_{sw} for CSVPWM and is 1.5 times that of f_{sw} for BCPWM methods.

The theoretical values of R.M.S. fundamental current for CSVPWM, 30°BCPWM and 60°BCPWM are shown plotted in Fig. 11(a). As seen the fundamental current is reduced on account of dead-time (compared to the ideal values) for all PWM schemes. However, such reduction is lower in case of two bus-clamping PWM methods than CSVPWM. Experimental results, corresponding to the theoretical results in Fig. 11(a), are shown plotted in Fig. 11(b). These measured values agree with the theoretical values. Compared to the theoretical values, the experimental values of RMS fundamental current are found to be lower. This is due to the voltage drops in the switches, which are not considered in the theoretical analysis. However, both theoretical and experimental results show that the fundamental current reduces with increase in switching frequency on account of

dead-time. The compensation circuit works reasonably well for all PWM schemes as seen from Fig. 11(c). Again the difference between the ideal load current and compensated load current could be attributed to the voltage drops in the power semiconductor devices.

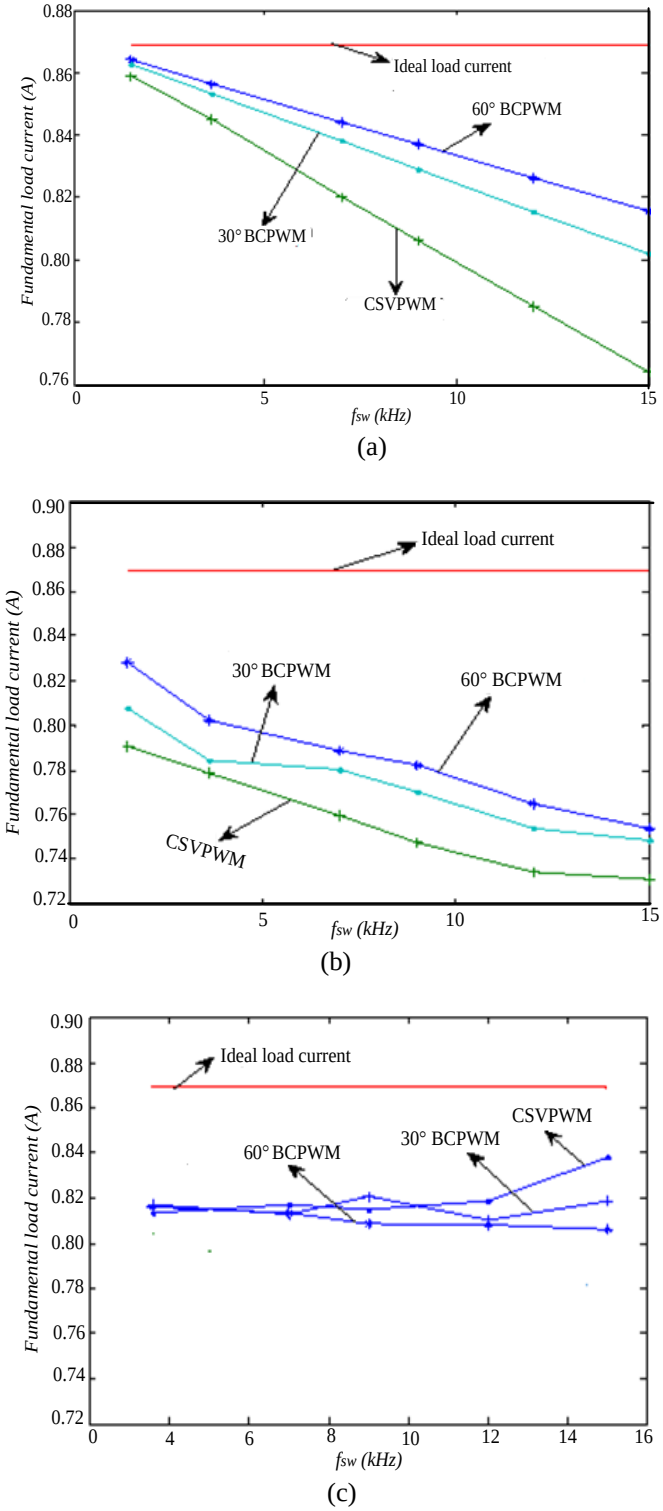


Fig. 11. Comparison of CSVPWM and BCPWM schemes (a) theoretical values of fundamental load current (b) experimental values of fundamental load current (c) experimental values of fundamental load current with dead-time compensation.

V. Conclusions

This paper analyses the effect of dead-time on the inverter output voltage for bus-clamping PWM schemes. The error voltage amplitude is expressed as a function of dead-time duration, carrier cycle, DC voltage and power factor angle. The analytical study is validated experimentally. The analytical and experimental results show that the effect of dead-time on fundamental voltage is lower in case of bus-clamping PWM than CSVPWM scheme at high power factors. Dead-time compensation circuit is found to significantly reduce the adverse effect of dead-time on fundamental output voltage for bus-clamping PWM schemes.

References

[1] M. Jones, D. Dujic, and E. Levi, "A Four-Motor Drive Supplied from a Triple Three-Phase Voltage Source Inverter," *Proc. Int. Power Electronics and Motion Control Conference, EPE-PEMC2010, pp. 194-200, Sept. 2010.*

[2] O. Vodyakho and C. C. Mi, "Three-Level Inverter-Based Shunt Active Filter in Three-Phase Three-Wire and Four-Wire Systems," *IEEE Transactions On Power Electronics, Vol. 24, No. 5, pp-1350-1363, May 2009.*

[3] B. Sarrazin, N. Rouger, J.P. Ferrievx, and J.C. Crebier, " Cascaded Inverters for Electric Vehicles: Towards a better Management of Traction Chain from the Battery to the Motor?," *Proc. IEEE Int. Sympo., Industrial Electronics (ISIE), pp. 153-158, June 2011.*

[4] S. G. Jeong and M. H. Park, "The Analysis and Compensation of Dead-Time Effects in PWM Inverters," *IEEE Trans. on Industrial Electronics*, Vol. 38, No. 2, pp-108-114, April 1991.

[5] V. M. Cardenas G., S. M. Horta, R. S. Echararria, "Eliminations of Dead Time Effects in Three-Phase Inverters," *Proc.* Inter. *Power Electronics Congress, pp-258-262, 1996.*

[6] L. B. Brahim, "The Analysis and Compensation Dead-Time Effects in Three-Phase PWM Inverters," *IEEE-IECON, 1998, Vol.2. pp-792-797.*

[7] X. Mao, R. Ayyanar and A. K. Jain, "Dead Time Effect in Two-Level Space Vector PWM Voltage Source Inverters with Large Current Ripple," *IEEE Applied Power Electronics Conference And Exposition (APEC), 2011, pp-679-684.*

[8] B. A. Welchko, S. E. Schulz, S. Hiti, " Effects and Compensation of Dead-Time and Minimum Pulse-Width Limitations in Two-Level Voltage Source Inverters," *Proc. Industry Applications Conference 2006, Vol. 2, pp. 889-896.*

[9] V.S.S.P.K. Hari and G. Narayanan, "Space-Vector-Based Hybrid Pulse Width Modulation Technique to Reduce Line Current Distortion in Induction Motor Drives," *IET Power Electronics, Vol.-5, No-8, pp-1463-1471, Sept. 2012.*

[10] M. Raghava Krishna And G. Narayanan, "A Dead Time Compensation Circuit For Voltage Source Inverters," *Proc. National Power Electronics Coference (NPEC), Roorkiee 2010.*

[11] D. Leggate and RJ Kerkman, " Pulse-based dead time compensator for PWM voltage inverters,"- *IEEE Trans. on Industrial Electronic,s Vol. 44, No-2, pp-191-197, April 1997.*

[12] J. L. Lin, "A New Approach of Dead-Time Compensation for PWM Voltage Inverters," *Proc. IEEE Transactions on Circuits and Systems, Vol. 49, No. 4, pp-476-483, April 2002.*