Experimental Study on Dead-Time Induced Oscillations in a 100-kW Open-Loop Induction Motor Drive

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***Abstract*—This paper reports instability and oscillations in the stator current under light-load conditions in a practical 100-kW induction motor drive. Dead-time is shown to be a cause for such oscillations. This paper shows experimentally that these oscillations could be mitigated significantly with the help of a simple dead-time compensation scheme.**

***Index Terms*—Induction motor drive, pulse width modulated inverter, dead-time, light-load instability, dead-time compensation.**

I. Introduction

OPEN-loop volts-per-hertz (V/f) control of an induction motor fed from IGBT-based voltage source inverter (VSI) is widely employed in high-power applications including fans and pumps. These drives operate over a wide range of speeds, carrying load torque ranging anywhere between no load and rated load. This paper reports instability phenomenon and its mitigation in a practical 100-kW induction motor drive, shown schematically in Fig. 1, at low speeds under light load. The operation of V/f drives at low speeds and light-load conditions is significant from the perspective of fan-type loads (where torque demand is low at low speeds).

The setup consists of a 100-kW squirrel-cage induction motor, coupled to a wound-rotor machine (not shown in Fig.1) through a rigid coupling (and not a flexible one) as required for a certain application. The wound-rotor machine is not loaded and just adds to the inertia of the system. The squirrel-cage induction motor is fed from an IGBT-based pulse-width-modulated (PWM) VSI. The inverter, in turn, is fed from a diode-bridge rectifier for testing the drive under light loads.

Oscillations of high amplitude were observed in the motor current at low fundamental frequencies under no load (see Fig. 2). Significant oscillations were also observed in the dc bus voltage (not shown). Further, the acoustic noise was of high intensity with a clearly audible sub-harmonic component.

The possible reasons for the oscillations could be mechanical, magnetic and/or electrical in nature. Initially, problems due to alignment and coupling were suspected, particularly since the coupling is rigid. But the mechanical system was smooth to be rotated by hand. Further the spatial harmonics

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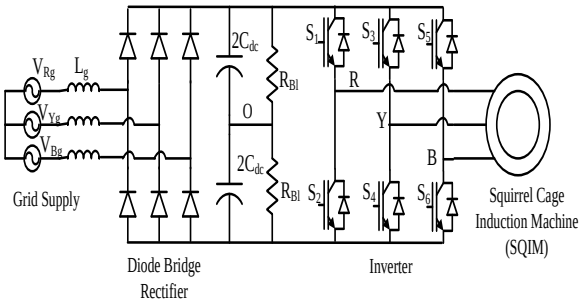


Fig. 1. Diode rectifier - inverter fed open loop induction motor drive.

on account of the winding distribution were also found to be negligible to cause any significant impact on the motor performance. Interestingly, the V/f ratio was found to have a significant impact on the oscillations as discussed below.

While it is common to provide a voltage boost at low modulation frequencies less than 5 Hz [1], even V/f ratios lower than 1 pu (e.g. 0.8 or 0.9 pu) were observed to result in inverter trip. In fact, the measured stator current waveform, shown in Fig. 2, is at a reduced V/f ratio of 0.63 pu and a steady frequency command of 10 Hz. As seen from the figure, the peak-to-peak current varies from fundamental cycle to cycle; the amplitude has a sub-harmonic envelope of frequency 1 Hz roughly.

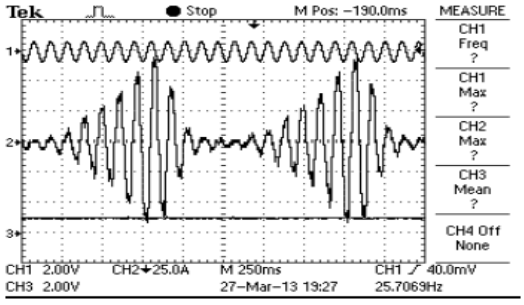


Fig. 2. Repetitive oscillations observed in the stator current waveform at an applied fundamental frequency of 10 Hz in a 100-kW squirrel induction motor at no load. Trace 1: modulating signal (2 V/div), Trace 2: stator current (25 A/div), Trace 3: frequency command (20 Hz/div).

The stability of an induction motor and the influence of various motor parameters on the same have been studied [2]–[7]. High values of stator resistance have been shown to cause light-load instability [4], [5]. In inverter-fed motor drives,

the effect of inverter dead-time could be seen as increase in stator resistance [5], [6]. Such an increase in the effective stator resistance and consequent oscillatory behaviour is more pronounced in case of high-power motors than low-power motors [8]. Hence it is hypothesized here that dead-time is a probable cause for the oscillations observed (Fig. 2) in the drive at low speeds.

Inverter dead-time is a short delay introduced between the gating signals of complementary switches in an inverter leg, to avoid a shoot through fault during commutation. The effect of dead-time on the inverter output voltage [9]–[11] is reviewed briefly in section II. It is shown that the dead-time effect can be modelled as an increase in stator resistance. Further, based on small-signal analysis, instability of the 100-kW induction motor is shown to increase with increase in the stator resistance. A simple dead-time compensation scheme is introduced in section III. Experimental results, demonstrating the reduction in the stator current oscillations with dead-time compensation, are presented in section IV.

II. Effect of dead-time in a VSI fed motor drive

The effects of inverter dead-time on the inverter output voltage and on the small-signal stability of the motor are studied in this section.

A. Instantaneous error voltage

An inverter leg consists of two complementary switches as shown by Fig. 3. The voltage at the mid-point of the leg,

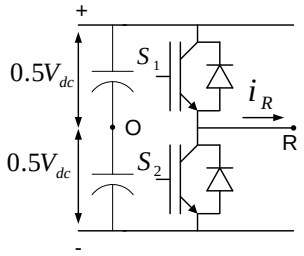


Fig. 3. One leg of a three-phase voltage source inverter.

measured with respect to the dc mid-point O, is defined as the pole voltage v_{RO}.

The ideal pole voltage $v_{RO,id}$, corresponding to the ideal gating signals S_1 and S_2 of the top and bottom switches, respectively, is shown in Fig. 4. However, for the purpose of device protection, the leading edges of S_1 and S_2 are delayed by dead-time t_d to obtain the actual gating signals S_{1d} and S_{2d} as shown in the figure. Since both the gating signals are low during dead-time, neither of the IGBT's can conduct. For the positive direction of load current i_R indicated in Fig. 3, the bottom anti-parallel diode conducts. Hence, during dead-time intervals, pole voltage is always $-\frac{V_{dc}}{2}$ for $i_R > 0$. The actual pole voltage $v_{RO,act}$ deviates from the ideal pole voltage $v_{RO,id}$ during diode-to-IGBT transitions (i.e whenever the IGBT should come into conduction), while there is no such deviation during the IGBT-to-diode transitions. This deviation is seen as an error voltage pulse of negative polarity for positive current as illustrated in Fig. 4. For $i_R < 0$, the top diode conducts during t_d. Hence the pole voltage

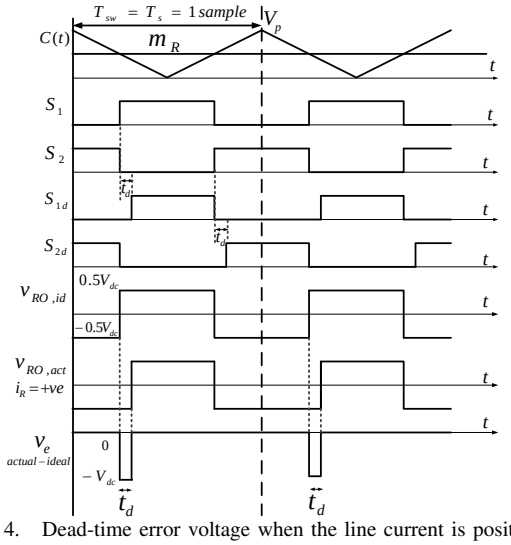


Fig. 4. Dead-time error voltage when the line current is positive.

is $\frac{V_{dc}}{2}$; therefore, the error voltage pulse is positive. Thus, the instantaneous error voltage v_e, on account of dead-time, depends on the current polarity as shown by (1), where V_{dc} is the dc bus voltage [9]–[11].

$$v_e = v_{RO,act} - v_{RO,id} = -sign(i_R)V_{dc} \tag{1}$$

The error voltage is seen as a train of negative pulses of width t_d during the positive half cycle of the current, and *vice-versa*, as shown by Fig.5. The width of the pulses are shown exaggerated for clarity.

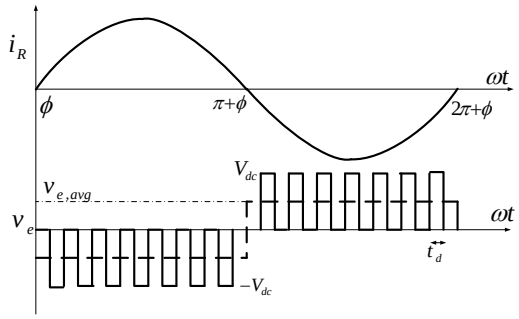


Fig. 5. Average dead-time error voltage over a fundamental cycle.

B. Average error voltage

The average error voltage over a carrier cycle is given by

$$v_{e,avg} = -V_{dc}t_d f_{sw} sign(i_R) = -V_{dc}\frac{t_d}{T_{sw}} sign(i_R) \tag{2}$$

where f_{sw} is the switching frequency, and T_{sw} is the switching time period. The average error voltage over a fundamental cycle of the current is seen to be a square wave of amplitude $v_{e,avg}$, and is out of phase with the fundamental load current. This error voltage increases with increase in switching frequency and dc bus voltage.

The fundamental component of the dead-time error voltage is given by

$$V_{e,avg,1} = \frac{4}{\pi} v_{e,avg} = \frac{4}{\pi} V_{dc}\frac{t_d}{T_{sw}} \tag{3}$$

This adds up to the ideal fundamental voltage V_{ideal} to yield the actual fundamental voltage V_{actual} as shown by the phasor diagram in Fig.6.

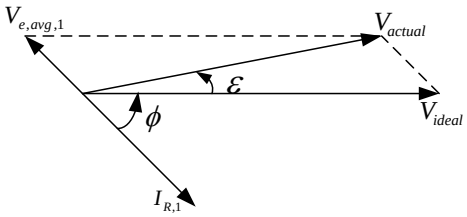


Fig. 6. Phasor diagram depicting the effect of the dead-time on fundamental output voltage.

C. Equivalent stator resistance due to dead-time effect

The difference between the actual fundamental voltage and ideal fundamental voltage on account of dead-time is given by $V_{e,avg,1}$ defined in (3). Since $V_{e,avg,1}$ is out of phase with the fundamental phase current ($I_{R,1}$) as shown by Fig.6, this voltage can be regarded as a resistance drop in series with the stator resistance as indicated by Fig. 7. Thus, the dead-time effect can be viewed as an equivalent resistance $R_{eq,dead-time}$ which can be expressed as follows:

$$R_{eq,dead-time} = \frac{V_{e,avg,1}}{I_{R,1}} \tag{4}$$

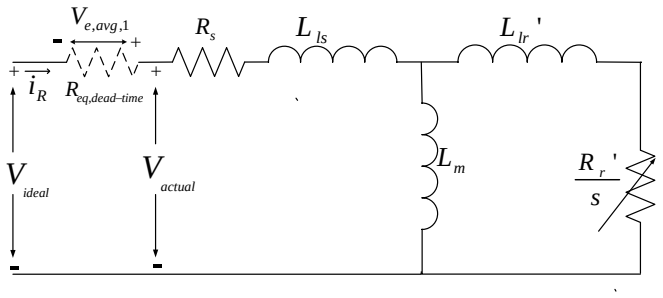


Fig. 7. Induction motor equivalent circuit with dead-time equivalent resistance included in series with the stator resistance.

This equivalent series resistance could be comparable to or even higher than the actual stator resistance R_s, particularly in high-power induction motor drives. This increase in stator resistance could have a significant impact on the stability of the high-power motor as brought out in the following subsection.

D. Small-signal stability

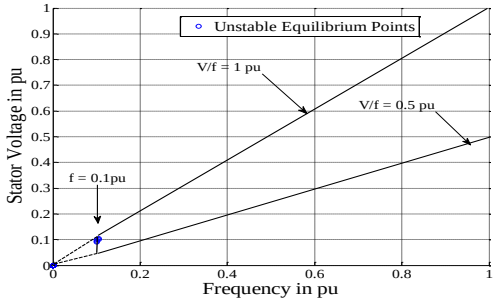
The induction motor dynamic equations, in the synchronously revolving reference frame, are linearised about their equilibrium operating points to obtain the small-signal model [3]–[5]. The state space representation of the small-signal model is derived to obtain the eigen values of the system at each equilibrium point. A positive real part of any eigen value indicates an unstable equilibrium point.

Stability analysis of the motor is carried out at all points on the V/f plane, considering a frequency range of 5 Hz to 50 Hz and with the V/f ratio ranging between 0.5 pu and 1 pu. With the induction motor parameters as shown in Table I and disregarding the dead-time effect, the results of the stability analysis are shown in Fig. 8(a). As seen from the figure, a small set of unstable equilibrium points are observed close to 5 Hz and a V/f ratio of 1 pu.

TABLE I
INDUCTION MOTOR PARAMETERS

R_s	R_r'	L_m
0.0277Ω	0.02Ω	$0.024H$
$L_{ls} = L_{lr}'$	J	B
$0.417mH$	$9kgm^2$	$0.05Nm/(rad/sec)$

Considering V_{dc} = 615 V, t_d = $5\mu s$ and f_{sw} = 5 kHz, the peak value of the error voltage $V_{e,avg,1}$ equals 19.6 V. The no-load magnetising current of the induction motor is 45 A (peak). Hence, the series equivalent resistance $R_{eq,dead-time}$ is 0.44Ω (which is 22 times the actual stator resistance) as per equation (4). The stability analysis is repeated considering a more conservative value of 0.2Ω than 0.44Ω for $R_{eq,dead-time}$. Now, the unstable equilibrium points in the V/f plane are very much increased as shown in Fig. 8(b). Thus, dead-time has an adverse effect on the stability of open-loop V/f induction motors under light-load conditions. Instability is observed over the widest range of fundamental frequency at a V/f ratio of 1 pu.



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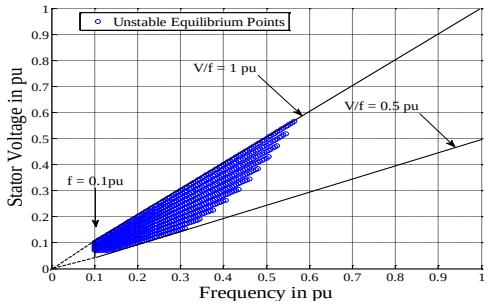


(b)

Fig. 8. Small-signal stability of the 100-kW induction motor with (a) original stator resistance: 0.0277Ω (b) increased stator resistance: 0.2277Ω

Considering a V/f ratio of 0.9 pu. and a stator frequency of 10 Hz, simulation results of the stator current waveform without dead-time, and with 1 μs and 5 μs dead-time are shown in Fig. 9(a), Fig. 9(b) and Fig. 9(c) respectively. The stator currents without dead-time are observed to be sinusoidal, while sub-harmonic oscillations at a frequency close to $1/4^{th}$ the fundamental are observed when a 1 μs dead-time is considered. The amplitude of the sub-harmonic oscillations is increased with a 5 μs dead-time, and the sub-harmonic frequency is observed to be around $1/6^{th}$ the fundamental

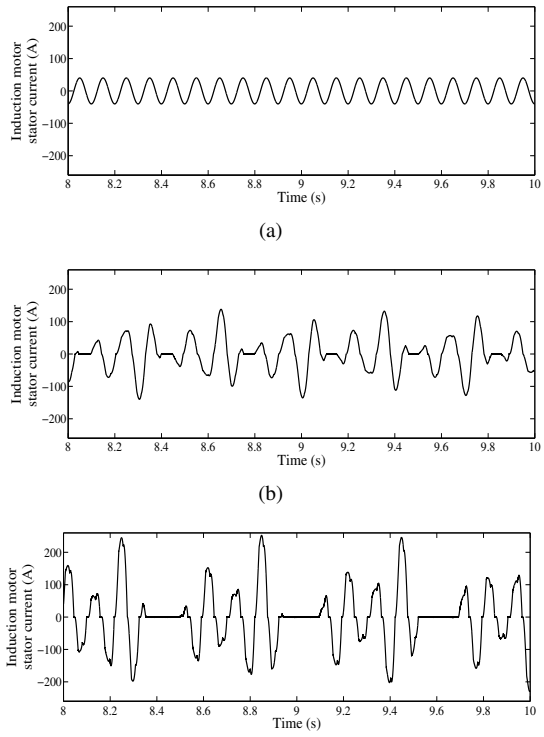


Fig. 9. Simulated induction motor currents at 10 Hz and V/f ratio of 0.9 pu (a) without inverter dead-time, (b) with 1 μs dead-time, (c) with 5 μs dead-time.

frequency. Further, when dead-time is considerable, the motor current is nearly zero over certain interval in the sub-harmonic cycle. It can be confirmed that the stability of the motor is definitely impacted by the inverter dead-time. Taking into consideration the longer time taken by high-power devices to turn-off and gate-driver delays, a longer dead-time duration is required in comparison with a lower power converter [12], [13]. Hence, the experimental inverter has a dead-time of $5\mu s$ for sufficient margin of safety.

III. Dead-time compensation scheme

A few dead-time compensation schemes have been presented in [11], [14]–[18]. A simple software based dead-time compensation scheme is employed here. A compensating term Δm is added or subtracted, depending on the line current polarity, to the sinusoidal modulating signal m_R to obtain the compensated modulating signal $m_{R,comp}$ as given by (5).

$$\begin{aligned} m_{R,comp} &= m_R + \Delta m,\ i_R > 0 \\ &= m_R - \Delta m,\ i_R < 0 \end{aligned} \tag{5}$$

The compensating term Δm is given by (6).

$$\Delta m = \left(\frac{t_d}{T_{sw}}\right) V_p \tag{6}$$

where V_p is the peak of the unipolar triangular carrier. With dead-time compensation, the width of the pulse S_{1compd} equals the width of the ideal gating signal S_1, as illustrated by Fig. 10. Hence the actual pole voltage with dead-time compensation is identical to the ideal pole voltage except for a shift in time by 0.5 t_d.

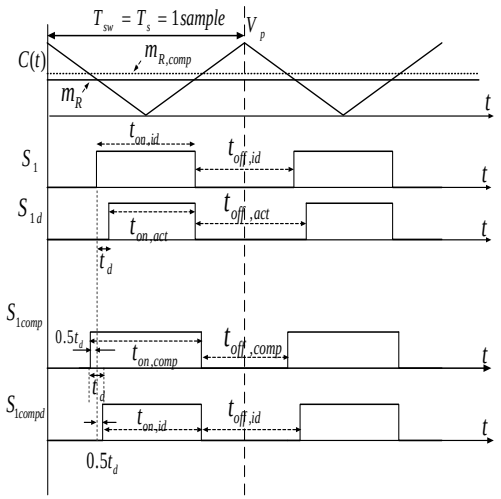


Fig. 10. Dead-time compensation illustrated for positive current.

IV. Experimental Results

The 415-V, 100-kW squirrel-cage induction motor in Fig. 1 is fed from a two-level voltage source inverter with a dc bus voltage of 615 V. The inverter is switched using sine - triangle modulation scheme at a carrier frequency of 5 kHz, with a dead-time of $5\mu s$. The V/f ratio is maintained at 63 % of the rated value as mentioned in section I. A TMS320F2812 digital signal processor based controller board is used to control the drive. Experimental results without and with dead-time compensation at different speeds are presented in Fig.11 to Fig.15.

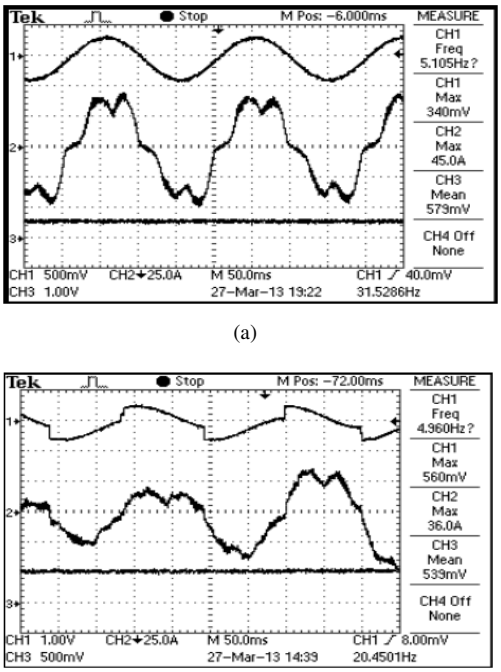


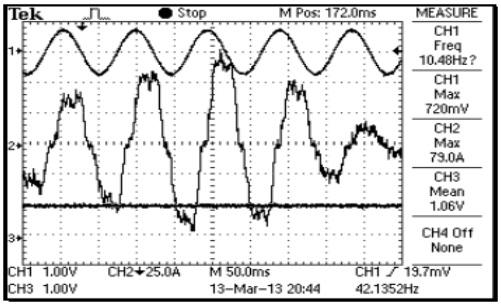
Fig. 11. Measured induction motor currents at 5 Hz (a) without dead-time compensation, Trace 1: modulating signal (0.5 V/div), Trace 2: stator current (25 A/div), Trace 3: frequency command (10 Hz/div) (b) with dead-time compensation. Trace 1: modulating signal (1 V/div), Trace 2: stator current (25 A/div), Trace 3: frequency command (5 Hz/div).

The measured motor current without dead-time compensation at an applied stator frequency of 5 Hz is shown in

Fig. 11(a). As seen, the motor current is distorted and contains significant low-frequency harmonic content. The torque developed is insufficient for the motor to start, overcoming inertia and static friction. With the implementation of the dead-time compensation scheme, discussed in section III, the compensated modulating signal is as shown by trace 1 in Fig. 11(b). With such a modulating signal, the motor starts rotating, but the current waveform is still distorted and contains sub-harmonic oscillations as seen from Fig. 11(b). It may be note that only a portion of the sub-harmonic cycle is visible in Fig. 11(b).

Thus, at a fundamental frequency of 5 Hz, the compensation helps the motor to get started and run, while not being good enough to ensure sinusoidal motor currents without sub-harmonic oscillations.

The improvement in stator current waveforms with this simple dead-time compensation is clearer at a modulation frequency of 10 Hz as seen from Fig. 12 than at 5 Hz. There is considerable sub-harmonic oscillation in the current without dead-time compensation as shown by Fig. 12(a). Dead-time compensation reduces the sub-harmonic oscillations, low-frequency harmonic distortion and also zero cross-over distortion in the current waveform as seen from Fig. 12(b). Similar improvements are also observed at fundamental



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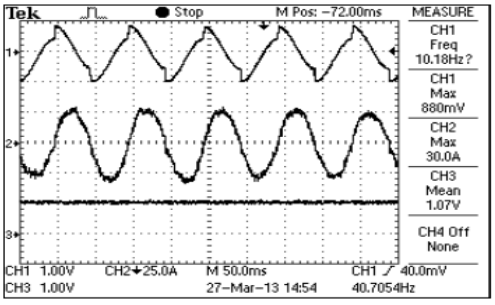
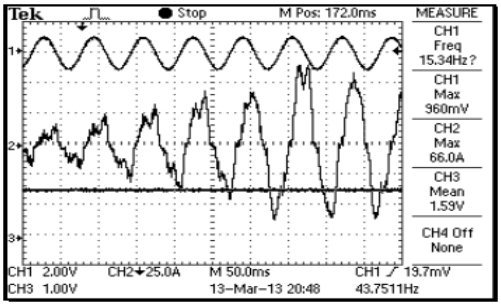


(b)

Fig. 12. Measured induction motor currents at 10 Hz (a) without dead-time compensation, (b) with dead-time compensation. Trace 1: modulating signal (1 V/div), Trace 2: stator current (25 A/div), Trace 3: frequency command (10 Hz/div).

frequencies of 15 Hz and 20 Hz as brought out by Fig. 13 and Fig. 14, respectively, with dead-time compensation.

The uncompensated sinusoidal modulating signal (say trace 1 in Fig. 11(a)) is significantly different from the compensated modulating signal (say trace 1 in Fig. 11(b)), at low frequencies such as 5 Hz , 10 Hz and 15 Hz. However, at 45 Hz, the uncompensated (sinusoidal) and compensated modulating



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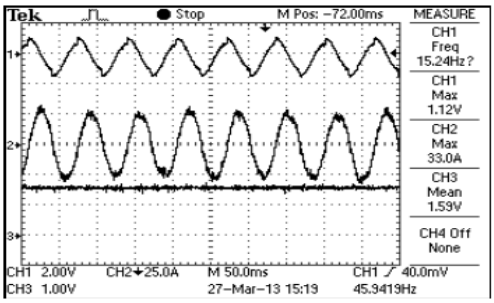
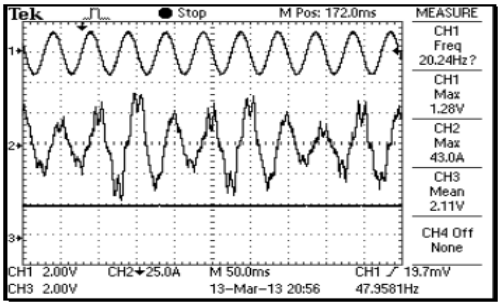


(b)

Fig. 13. Measured induction motor currents at 15 Hz (a) without dead-time compensation, (b) with dead-time compensation. Trace 1: modulating signal (2 V/div), Trace 2: stator current (25 A/div), Trace 3: frequency command (10 Hz/div).



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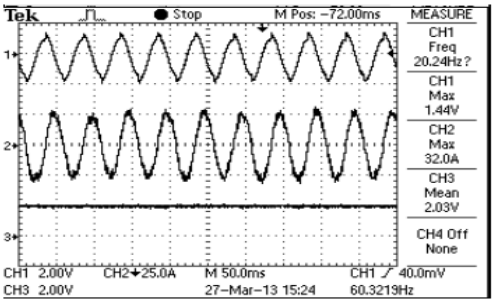
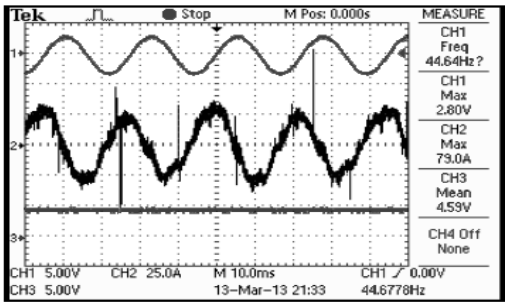


(b)

Fig. 14. Measured induction motor currents at 20 Hz (a) without dead-time compensation, (b) with dead-time compensation. Trace 1: modulating signal (2 V/div), Trace 2: stator current (25 A/div), Trace 3: frequency command (20 Hz/div).

signals are quite similar as seen from Fig. 15(a) and Fig. 15(b). Further, the motor current waveforms are also quite similar without and with dead-time compensation.



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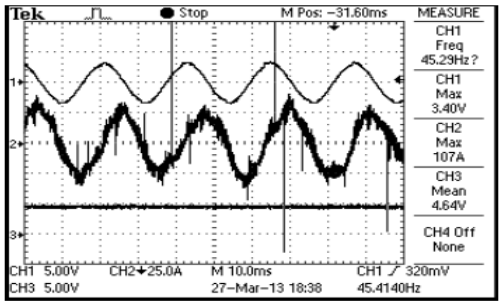

(b)

Fig. 15. Measured induction motor currents at 45 Hz (a) without dead-time compensation, (b) with dead-time compensation. Trace 1: modulating signal (5 V/div), Trace 2: stator current (25 A/div), Trace 3: frequency command (50 Hz/div).

The dead-time compensation scheme employed facilitates smooth starting and operation of the induction motor, avoiding inverter current trips. The sub-harmonic oscillations in the motor currents are reduced significantly, and also the waveform quality of the motor current is improved considerably. The improvement is particularly significant in the range of 10 Hz to 20 Hz, where the sub-harmonic oscillations were prominent prior to the dead-time compensation.

It may be noted that the analysis of dead-time effect in section II and the dead-time compensation scheme in section III consider only the fundamental component of the motor current and ignore the ripple current. However, the ripple current is quite significant at high modulation frequencies since the ratio of the switching frequency to the modulating frequency is low. Also, there are zero-current clamp intervals (see trace 2 in Fig. 11(a)) at low frequencies of the drive [19]. Research is in progress to evolve an improved dead-time compensation scheme, capable of addressing the above issues.

V. Conclusion

Dead-time between the complementary devices in an inverter leg tends to distort the inverter output voltage. In case of induction motor drives, the effect of dead-time at the fundamental output voltage can be modelled as an equivalent resistance in series with the stator. The increased stator resistance has an adverse impact on the light-load stability of the induction motor. This increase is particularly significant in high-power motor drives, where the actual resistance of the stator winding is low. This paper presents experimental evidence for such light-load instability at low speeds of a 100-kW induction motor drive.

A simple dead-time compensation scheme is employed in this paper which reduces the light-load instability significantly, particularly in the range of 10-20 Hz. The compensation scheme ensures smooth starting and operation of the motor drive. Oscillations in the stator current are reduced. The acoustic noise is very much reduced and its sub-harmonic component is no longer perceptible.

Thus, this paper reconfirms the instability problem in open-loop V/f drives under light-load conditions. Further the paper demonstrates, through experimental evidence, that dead-time compensation is an effective method to handle this instability and mitigate the associated oscillations.

References

[1] W. Leonhard, *Control of electrical drives*. Springer, 2001.

[2] G. Rogers, "Linearised analysis of induction-motor transients," *Proc. IEE*, vol. 112, no. 10, pp. 1917–1926, 1965.

[3] R. H. Nelson, T. A. Lipo, and P. C. Krause, "Stability analysis of a symmetrical induction machine," *IEEE Trans. Power App. Syst.*, no. 11, pp. 1710–1717, 1969.

[4] F. Fallside and A. Wortley, "Steady-state oscillation and stabilisation of variable-frequency invertor-fed induction-motor drives," *Proc. IEE*, vol. 116, no. 6, pp. 991–999, 1969.

[5] R. Ueda, T. Sonoda, K. Koga, and M. Ichikawa, "Stability analysis in induction motor driven by a v/f controlled general-purpose inverter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 2, pp. 472–481, 1992.

[6] R. Ueda, T. Sonoda, and S. Takata, "Experimental results and their simplified analysis on instability problems in pwm inverter induction motor drives," *IEEE Trans. Ind Appl.*, vol. 25, no. 1, pp. 86–95, 1989.

[7] V. Vasic, D. Marcetic, D. Oros, and F. Kulic, "Prediction of local instabilities caused by inverter dead time in ac drive," in *Proc. 13th European Conf. Power Electron. and Applicat.*, 2009, pp. 1–9.

[8] B. Peterson, "Oscillations in inverter fed induction motor drives," Master's thesis, Department of Industrial Electrical Engineering and Automation (IEA), Lund University, Sweden, 1991.

[9] Y. Murai, T. Watanabe, and H. Iwasaki, "Waveform distortion and correction circuit for pwm inverters with switching lag-times," *IEEE Trans. Ind. Appl.*, no. 5, pp. 881–886, 1987.

[10] X. Mao, R. Ayyanar, and A. K. Jain, "Dead time effect in two-level space vector pwm voltage source inverters with large current ripple," in *Proc. IEEE Applied Power Electron. Conf and Expo*, Fort Worth, TX, USA, Mar. 2011, pp. 679–684.

[11] M. R. Krishna and G. Narayanan, "A dead-time compensation circuit for voltage source inverters." in *Proc. National Power Electron. Conf.*, Roorkee, India, Jun. 2010.

[12] P. Palmer, X. Yang, and W. He, "Dead-time minimisation using active voltage control gate drive for high-power igbt converters," in *Proc. IEEE Ind. Electron. Conf.*, Montreal, QC, Canada, Oct 2012, pp. 333–338.

[13] Infineon, *Application note AN2007-04, Deadtime calculation for IGBT Modules*, 2007. [Online]. Available: http://www.infineon.com

[14] D. Leggate and R. J. Kerkman, "Pulse-based dead-time compensator for pwm voltage inverters," *IEEE Trans. on Ind. Electron.*, vol. 44, no. 2, pp. 191–197, 1997.

[15] J. W. Choi and S. K. Sul, "Inverter output voltage synthesis using novel dead time compensation," *IEEE Trans. Power Electron.*, vol. 11, no. 2, pp. 221–227, 1996.

[16] S.-H. Hwang and J.-M. Kim, "Dead time compensation method for voltage-fed pwm inverter," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 1–10, 2010.

[17] H. Zhengyi and J. Xuewu, "A new inverter compensation strategy based on adjusting dead-time on-line," in *IEEE Int. Symp. on Ind. Electron.*, 2008, pp. 768–773.

[18] R. Yang, W. Chen, Y. Yu, and D. Xu, "Stability improvement of v/f controlled induction motor driver systems based on reactive current compensation," in *Proc. IEEE Int. Conf. Electrical Machines and Systems*, Wuhan, China, Oct 2008, pp. 88–90.

[19] J.-W. Choi and S.-K. Sul, "A new compensation strategy reducing voltage/current distortion in pwm vsi systems operating with low output voltages," *IEEE Trans. Ind. Appl.*, vol. 31, no. 5, pp. 1001–1008, 1995.