Comparative Evaluation of Switching and Average Models of a DC-DC Boost Converter for Real-Time Simulation

Janamejaya Channegowda*, B. Saritha, Habeeb Rahman Chola and G. Narayanan
 Dept. of Electrical Engineering,
 Indian Institute of Science,
 Bangalore, India.
 bcjanmay.work@gmail.com*

Abstract— This paper presents a comparative evaluation of the average and switching models of a dc-dc boost converter from the point of view of real-time simulation. Both the models are used to simulate the converter in real-time on a Field Programmable Gate Array (FPGA) platform. The converter is considered to function over a wide range of operating conditions, and could do transition between continuous conduction mode (CCM) and discontinuous conduction mode (DCM). While the average model is known to be computationally efficient from the perspective of off-line simulation, the same is shown here to consume more logical resources than the switching model for real-time simulation of the dc-dc converter. Further, evaluation of the boundary condition between CCM and DCM is found to be the main reason for the increased consumption of resources by the average model.

Keywords— Average model, continuous conduction mode, dc-dc converter, discontinuous conduction mode, FPGA, logical cells, real-time, switching model.

I. INTRODUCTION

Digital platform based real-time simulation of dc-dc converters is a well-established concept in the field of power electronics. Real-time simulation is necessary to evaluate the performance of a controller in a complex power-electronic system [1]. Field programmable gate array (FPGA) is a widely employed digital platform for real-time simulation of power electronic converters [2]-[4], due to its potential for high parallelism. DC-DC boost converter is an important component in a large system such as grid connected photovoltaic (PV) converters. Boost converter is generally simulated using a) Switching model b) Average model. The switches in the switching model are simulated to be ideal or with a detailed v/i characteristics [5]. In this paper, the switch is modeled as small/large resistors, depending on its ON/OFF condition.

The voltage across the switches or current through the switches is averaged over a switching period and average model of power electronic converters is simulated [6, 7]. The purpose of average model is to ensure the operation of converter, obeying certain specifications of the user. The

average model can also reproduce the dynamics of the system [7], but the variation in switching frequency is not considered in the average model. In this paper, the average model of boost converter is simulated, by averaging the voltage across the switch SW and current through the diode D (Fig. 1).

Fig. 1. Schematic of ideal boost converter

In this paper, the state-space approach is used for modeling the boost converter. Two distinct difference equations, describing the circuit are obtained, depending on ON/OFF condition of switch. The non-idealities such as resistance of switch (R_{sw}), voltage drop across the diode (v_f), resistance of inductor (R_L) and ESR of capacitor (R_c) are considered. The real-time model of converter can represent both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) of operation.

During offline simulation, the time step for simulating the average model of boost converter can be higher than the switching period (T_s). The time step for simulating the switching model of boost converter must be less than T_s i.e. $0.01 T_s$; to emulate the transition in ON/OFF condition of switches. Hence, the average model is advantageous over switching model, in terms of computation time during off-line simulation.

In real-time simulation, the time step for simulation is decided by the processing speed of FPGA. The simulation of high frequency (≈ 100 kHz) switching converters may impose the limitation on FPGA clock speed. In general, the modern FPGA offers decent clock speed, to enable the simulation of power converters using state-space approach. Hence, the comparison of average and switching model of boost

converter is performed, on the basis of logical resources consumed within FPGA. When a large system such as grid connected PV module is simulated in FPGA, the individual components are represented by switching or average model. Hence the comparison of switching and average model in real-time simulation domain is necessary.

The paper is organized as follows: Mathematical representation of boost converter is given in section II; Implementation in FPGA is discussed in section III; Real-time simulation results are presented in section IV; Experimental verification of accuracy is given in section V; followed by conclusion in section VI.

II. MATHEMATICAL REPRESENTATION

In boost converter, the current through inductor i_L and voltage across the capacitor v_c , are taken as state variables. The output variables are inductor current i_L and output voltage v_o . The state equations, when the switch SW is ON and OFF, are given by (1)-(4). The output voltage (v_o) of boost converter is obtained by the sum of v_c and drop across ESR of capacitor, as given in (5). The ON/OFF condition of switch SW is indicated by a switching function S_1 ($S_1 = 1$: ON; $S_1 = 0$: OFF). The difference equations representing the state space representation of boost converter are given by (6)-(9). The time step " Δt " for simulation is $2e-6$ sec. The load connected to boost converter is assumed to be resistive R . For ideal boost converter, the non-idealities such as R_{sw} , v_f , R_l and R_c are not considered. The switching model is realized using (6)-(10). If the state variable i_L in (8) is less than zero, then the converter enters into DCM. Under DCM, the state variable i_L is equated to zero and capacitor voltage v_c is determined using (9).

$$\frac{di_L}{dt} = \frac{V_g - i_L(R_l + R_{sw})}{L}; \quad 0 < t \leq DT_s \quad (1)$$

$$\text{Where } V_g \text{ is the input dc voltage.} \quad (2)$$

$$\frac{dv_c}{dt} = -\frac{v_o}{RC}; \quad 0 < t \leq DT_s \quad (3)$$

$$\frac{di_L}{dt} = \frac{V_g - v_o - v_f - i_L R_l}{L}; \quad DT_s < t \leq (1-D)T_s \quad (4)$$

$$\frac{dv_c}{dt} = \frac{i_L}{C} - \frac{v_o}{RC}; \quad DT_s < t \leq (1-D)T_s \quad (5)$$

$$v_o(t) = v_c(t) + C \frac{dv_c}{dt} R_c \quad (6)$$

$$i_L(k+1) = \frac{(V_g - i_L(k)(R_l + R_{sw}))}{L} * \Delta t + i_L(k); \quad S_1 = 1 \quad (7)$$

$$v_c(k+1) = -\frac{v_o}{RC} * \Delta t + v_c(k); \quad S_1 = 1 \quad (8)$$

$$i_L(k+1) = \frac{(V_g - v_o(k) - v_f - i_L(k)R_l)}{L} * \Delta t + i_L(k); \quad S_1 = 0 \quad (9)$$

$$v_c(k+1) = \left(\frac{i_L(k)}{C} - \frac{v_o(k)}{RC} \right) * \Delta t + v_c(k); \quad S_1 = 0 \quad (10)$$

$$v_o(k) = v_c(k+1) \frac{CR_c}{\Delta t} + \left(1 - \frac{CR_c}{\Delta t} \right) * v_c(k) \quad (10)$$

In average model of boost converter, the voltage across the switch (v_p) and diode current (i_D) are averaged over a switching period T_s . The averaged variables of model are indicated in capital letters, in order to differentiate them from instantaneous quantities. The switch SW is ON for the duration DT_s and OFF for the duration $(1-D)T_s$. The duty cycle "D" is obtained by averaging the switching function S_1 over a time period T_s . Under CCM, the diode is conducting for the duration $(1-D)T_s$. Under DCM, the diode is conducting for the duration D_2T_s and the value of D_2 is given by [11]:

$$D_2 = \frac{K + \sqrt{K^2 + 4D^2K}}{2D}; \text{ where } K = \frac{2L}{RT_s} \quad (11)$$

The value of V_p and I_D of non-ideal boost converter are given in Table I. The non-idealities are not considered, during the implementation of ideal boost converter.

TABLE I. AVERGED VALUE OF V_p AND I_D

Variable	Boost converter under CCM	Boost converter under DCM
$V_p(k)$	$I_L(k) R_{sw} D + \{ (V_o(k) + v_f) * (1-D) \}$	$I_L(k) R_{sw} D + \{ (V_o(k) + v_f) D_2 \} + V_g (1-D-D_2)$
$I_D(k)$	$I_L(k) (1-D)$	$I_L(k) D_2$

The difference equations representing the average model of boost converter is given in (12)-(14).

$$I_L(k+1) = \frac{(V_g - V_p(k) - I_L(k)R_l)}{L} * \Delta t + I_L(k) \quad (12)$$

$$V_c(k+1) = \left(\frac{I_L(k)}{C} - \frac{V_o(k)}{RC} \right) * \Delta t + V_c(k) \quad (13)$$

$$V_o(k) = V_c(k+1) \frac{CR_c}{\Delta t} + \left(1 - \frac{CR_c}{\Delta t} \right) * V_c(k) \quad (14)$$

TABLE II. PARAMETERS OF BOOST CONVERTER

Model Parameters	Value of parameters
Inductor (L)	2 mH
Capacitor (C)	10 μ F
Load (R)	105 Ω
Drop across diode (V_f)	0.8 V
ON resistance of switch (R_{sw})	55 m Ω
Resistance of inductor (R_l)	2 Ω
ESR of capacitor (R_c)	0.6 Ω

III. IMPLEMENTATION OF MODELS

The models of boost converter are implemented in ALTERA's FPGA EP1C12Q240C8. EP1C12Q240C8 has 12060 logical elements, 52 RAM blocks and 249 I/O pins. The system clock of EP1C12Q240C8 is 20 MHz. The switching frequency of boost converter is 50 kHz and it can be implemented easily in the selected FPGA. The time step for simulating the models is chosen as $2\mu s$ ($= 500$ kHz) and it is synchronized with the system clock. The enable pulse of 500 kHz frequency, with ON time as $0.05\mu sec$, is used for

implementing the models. The output from real-time models in FPGA are visualized in oscilloscope using two channel 12-bit DAC. The input to models can be given through 4-channel 12-bit ADC and I/O pins. The duty cycle D is an input to average model and the switching pulse S_1 is an input to the switching model. The setup of FPGA in lab is shown in Fig. 2. The parameters of simulated boost converter are shown in Table II.

Fig. 2. FPGA setup in lab

The difference equations in section II are implemented on per unit basis. The base quantities are defined as follows: voltage $V_b=100V$, current $I_b=4A$, load $Z_b=25\Omega$. If the input voltage V_g is 21.4, it is implemented within FPGA as 0.214 per unit (pu). $(3FFF)_h$ is taken as a representation for 1 pu of any quantity. The variables in pu can be altered during run time of the program using in-system memory window of QUARTUS software.

a) Switching model

b) Average model

Fig. 3. Start-up transient in the boost converter a) Switching model b) Average model

IV. REAL-TIME SIMULATION RESULTS

The average and switching models of boost converter are evaluated for its dynamic performance, with the following parameters: $V_g = 21.4 V$, $R = 105 \Omega$ and $D = 0.5$. The boost converter is operating under CCM and the start-up transients in the inductor current and output voltage of the converter are shown in Fig. 3. From Fig. 3, it is clear that the response

from switching and average model is similar. The transient study of the models is performed with the following test cases: a) Load is changed from 105Ω to 500Ω ; b) Input voltage is varied from 21.4 to 28 V; c) Duty cycle is varied from 0.2 to 0.5.

Fig. 4. Flow of logic depicting the FPGA programming parameters

a) Switching model

b) Average model

Fig. 5. Transients due to load variation 105Ω to 500Ω ; $V_g = 21.4V$, $D = 0.5$, $f_{sw} = 50kHz$ a) Switching model b) Average model

Under all the above cases, the response form models are shown in Fig. 5, 6 and 7. It is clear from Fig. 3, 5, 6 and 7 that the average model can reproduce the behavior of boost converter, similar to switching model; except the ripple in currents and voltages.

The FPGA programming parameters used in the current boost converter model have been presented in Fig. 4.

Fig. 6. Transients due to input voltage variation from 21.4V to 28 V: $R = 105\Omega$, $D = 0.5$, $f_{sw} = 50\text{kHz}$ a) Switching model b) Average model

Fig. 7. Transients due to variation in duty cycle from 0.2 to 0.5: $V_g = 21.4$, $R = 105\Omega$, $f_{sw} = 50\text{kHz}$ a) Switching model b) Average model

TABLE III. RESOURCES UTILIZED BY MODELS UNDER CCM

Resources	Switching model	Average model
Logical Elements	6641/12060	5143/12060
Logical Cell Registers	914	1309
Look-up-table Logical cells	4229	5332
Look-up-table Register Logical cells	767	1163

The device utilization summary of switching and average model of boost converter under CCM is tabulated in Table III. From Table III, it is clear that the average model consumes fewer resources and hence it is beneficial to use it to represent the CCM operation of boost converter than the switching model.

TABLE IV. RESOURCES UTILIZED BY MODELS UNDER DCM

Resources	Switching model	Average model
Logical Elements	5333/12060	7084/12060
Logical Cell Registers	918	843
Look-up-table Logical cells	4415	6241
Look-up-table Register Logical cells	785	788

The boost converter is operating under DCM, with $V_g = 20$ V, $R = 2450\Omega$ and $D = 0.5$. To realize the average model of converter, operating under DCM, the variable D_2 has to be computed. The computational burden of average model of the converter, under DCM is higher than of that of converter, operating under CCM. The switching model of converter, operating under DCM does not vary broadly. Hence, the computational burden of switching model of the converter has not increased. The resources consumed by the models of converter, operating under DCM are tabulated in Table IV.

The output voltage and inductor current of boost converter, operating under DCM, is shown in Fig. 8. The ripple in inductor current is notable in DCM, but the ripple in output voltage is small. In general, for the performance evaluation of large systems such as electric vehicles, the boost converter is a component and the output voltage of boost converter is essential for the controller. The representation of boost converter by average model is also a good idea, for performance evaluation of controllers.

The models of boost converter, capable of operating under CCM as well as DCM, are built in FPGA. The resources consumed by the switching and average models of boost converter are tabulated in Table V. It is clear from Table V that the average model consumes large resources, compared to switching model. It is mainly due to the computations, involved in the DCM operation of boost converter.

Fig. 8. Output voltage and inductor current of boost converter under DCM, with $V_g = 20$, $R = 2450 \Omega$, $D = 0.5$ a) Switching model b) Average model

TABLE V. RESOURCES CONSUMED BY MODELS OF BOOST CONVERTER, CAPABLE OF OPERATING UNDER CCM AS WELL AS DCM

Resources	Switching model	Average model
Logical Elements	5334/12060	9310/12060
Logical Cell Registers	918	928
Look-up-table Logical cells	4416	8382
Look-up-table Register Logical cells	785	788

V. EXPERIMENTAL VERIFICATION

The experimental setup consists of a 40W boost converter, PWM controller TL494 and resistive load. The boost converter is built with the parameters listed in Table II and the MOSFET IRF740 is used as an active switch. The switching frequency and duty cycle are varied using TL494. The inductor current and output voltage of the converter under various operating (CCM/DCM) conditions are measured. The measured steady state current and voltage are compared with the results from real-time models in Fig. 9. From Fig.9, it is clear that the results from real-time models match with the experimental results and hence the models are accurate.

a) Experimental results

Fig. 9. Inductor current and output voltage of boost converter under $V_g = 20$ V, $D = 0.5$, $f_{sw} = 25$ kHz, $R = 250\Omega$; a) Experimental results b) Results from switching model c) Results from average model

VI. CONCLUSION

In this paper, the comparative evaluation of the real-time switching and average models of boost converter is performed. The performance of models is studied under transient and steady-state operating conditions. The average model consumes large resources in FPGA, in contrast to switching model. In offline simulation, the average model has less computation time compared to switching model and hence it is preferred for large system study. In contradiction to offline simulation, the real-time simulation shows that the switching model is beneficial over average model, in terms of device utilization. The disadvantages that exist in off-line simulation such as greater program execution time for smaller time-steps and the inability to change input programming parameters during the execution of the model are overcome by implementing the boost converter model on FPGA. The comparison of real-time models is a useful study material for the students and engineers.

REFERENCES

- [1] M. Matar, M. Abdel-Rahman and A.-M. Soliman, "FPGA-Based Real-Time Digital Simulation," in Proceedings of IPST'05, Montreal, Canada, Paper No. 149, June 19-23, 2005.
- [2] H.F. Blanchette, T. Ould-Bachir and J.P. David, "A state-space modeling approach for the FPGA-based real-time simulation of high switching frequency power converters", IEEE Trans. Ind. Elec., vol. 59, no. 12, Dec. 2012, pp. 4555-4567.
- [3] M. Matar, R. Iravani, "FPGA implementation of the power electronic converter model for real-time simulation of electromagnetic transients", IEEE Trans. Power Delivery, vol. 25, no. 2, Apr. 2010, pp. 852-860.
- [4] Luis Herrera, Cong Li, Xiu Yao, Da Jiao, and Jin Wang, "FPGA based real time electro-thermal modeling of power electronic converters", Proc. APEC 2013, pp. 1725-1729.
- [5] A. Myaing and V. Dinavahi, "FPGA-based real-time emulation of power electronic systems with detailed representation of device characteristics", IEEE Trans. Ind. Elec., vol. 58, no. 1, Jan. 2011, pp. 358-368.

- [6] C. Jaon, R. Pindado, J. Pou and V. Sala, "Adaptive model applied to PWM DC-DC converters using averaging techniques", IEEE ISIE 2006, July 9-12, 2006, Montreal, Canada, pp. 1347-1352.
- [7] A. Davoudi, J. Jatskevich, P.L. Chapman and A. Khaligh, "Average-switch modeling of fourth-order PWM DC-DC converters considering conduction losses in discontinuous mode", IEEE Trans. Pow. Elec., vol. 22, no. 6, Nov. 2007, pp. 2410-2415.
- [8] M.B.Patil, V.T.Ranganathan and V. Ramanarayanan, "Dynamic Performance of Switched Mode Power Converters" in "*Simulation of power electronic circuits*", Narosa, New Delhi, 2009. ch.17, sec.17.9, pp.17.9-17.19.