SEU Reliability Improvement Due to Source-Side Charge Collection in the Deep-Submicron SRAM Cell

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***Abstract*—The effect of technology scaling (0.5–0.09 μm) on single event upset (SEU) phenomena is investigated using full two-dimensional device simulation. The SEU reliability parameters, such as critical charge ($Q_{\rm crit}$), feedback time ($T_{\rm fd}$) and linear energy transfer (LET), are estimated. For $L_g < 0.18$ μm, the source node collects a significant fraction of radiation-induced charge resulting in an increase of LET, despite the lower critical charge at the sensitive drain node. The effect of striking location on LET confirms this finding.**

***Index Terms*—Bipolar injection effect, critical charge ($Q_{\rm crit}$), deep submicron (DSM), drain-induced barrier lowering (DIBL), feedback time ($T_{\rm fd}$), linear energy transfer (LET), single event upset (SEU), source-side charge collection (SSCC).**

I. Introduction

THE aggressive downscaling of CMOS technology has resulted in several reliability concerns. The radiation-induced single event upset (SEU) reliability is expected to get worse. The critical charge required to flip a memory cell decreases due to the scaling of the supply voltage and the cell capacitance [1]. This, in turn, implies that the minimum linear energy transfer (LET) required by the radiation to flip the cell would also decrease. The decreasing trend in LET with the shrinking device dimensions has indeed been demonstrated over three generations of Sandia's n-substrate technology (0.5, 1, and 2 μm) observed by Dodd *et al.* [2]. In another paper, by Roche *et al.* [3], it has been shown that SEU vulnerability is multiplied by a factor of three if the gate length is roughly reduced by a factor of two for 0.35- and 0.5-μm technology.

In the design of deep-submicron (DSM) transistors, the effect of drain-induced barrier lowering (DIBL) on the subthreshold leakage current has been very well recognized [4]. Due to the proximity, the drain electrical field influences the carrier injection at the source junction. The purpose of this paper is to investigate whether a similar proximity effect occurs with respect to SEU phenomena, due to the source influencing the radiation-generated charge at the drain node. We have used a full two–dimensional (2-D) process, device, and mixed-mode simulation-based approach to design and characterize six different technology nodes from 0.5 to 0.09 μm. For the first time, we have demonstrated a turnaround effect in the SEU reliability with scaling.

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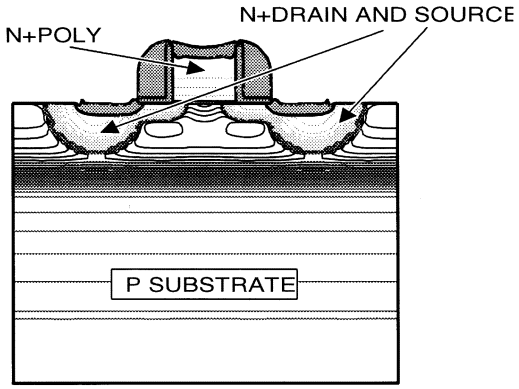

Fig. 1. 0.09-μmm nMOS transistor cross section showing channel engineering.

II. Simulation Methodology

We have used DIOS process simulator (from ISE) to design the transistors for different technology nodes. The design is performed such that the transistor leakage current is restricted to less than 10 pA/μm. The source/drain engineering (shallow extension) and the channel engineering (i.e., pocket-halo and supersteep retrograde channel) have been implemented to suppress the short-channel effects. The disposable spacer technique has been used to decrease the poly-Si gate depletion and suppress the source/drain diffusion [5]. For 0.12- and 0.09-μm transistors, silicon nitride gate dielectric has been used to suppress the direct tunneling leakage current. Fig. 1 shows the process-generated transistor cross section. Table 1 summarizes salient features of nMOS transistor parameters at each node. We have followed the constant field scaling to limit the average vertical field to 6 MV/cm and the average lateral electric field to 10 V/μm. The SRAM cell is constructed using the process-generated nMOS and pMOS transistors. The gate length of all four transistors in the cross-coupled SRAM cell is chosen to be the minimum allowed ($L_{\rm min}$) at each node. The width of the nMOS and pMOS transistors are 1.5 and 2 $L_{\rm min}$, respectively. In order to simulate the radiation effect, the length of the heavy-ion penetration track is made equal to the epitaxial layer thickness of 0.5 μm. The radiation charge is Gaussian in space and time, with a characteristic radius of 0.2 μm and a characteristic time of 2 ps.

TABLE I
NMOS TRANSISTOR PARAMETERS. V_t IS MEASURED USING THE CONSTANT CURRENT TECHNIQUE AT A VALUE OF 40 $nA * W/L$. THE WIDTH IS 1 μm IN ALL CASES

L_g (μm)	V_{dd} (volt)	Gate Dielectric Material	T_{ox} (Å)	I_{off} (pA)	I_{on} (mA)	V_t (volt)
0.50	5.0	Oxide	80	8.00	0.98	0.316
0.35	3.3	Oxide	55	10.0	0.78	0.320
0.25	2.5	Oxide	42	10.0	0.68	0.330
0.18	1.8	Oxide	30	10.0	0.51	0.370
0.12	1.2	Nitride	38	6.00	0.41	0.387
0.09	0.9	Nitride	29	6.75	0.26	0.393

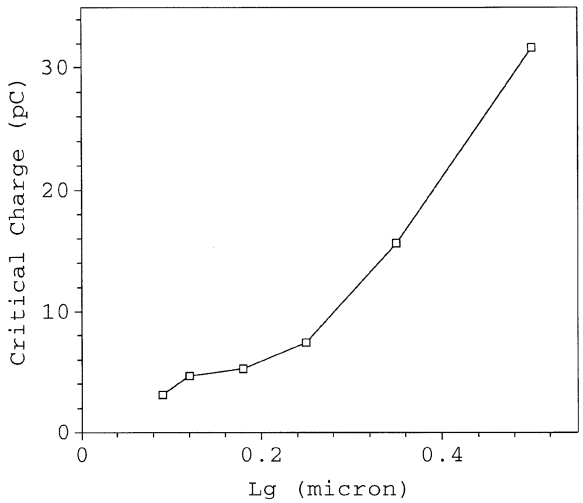

Fig. 2. Critical charge variation with the gate length.

III. SIMULATION RESULTS AND DISCUSSION

Fig. 2 shows the critical charge at different technology nodes, which can be calculated by integrating the current at the sensitive drain node of the nMOS transistor after the strike [1].

$$Q_{\text{crit}} = \int_0^{T_{\text{fd}}} I_{\text{ds}_\text{n}} dt \tag{1}$$

where I_{ds_n} is the drain current at the struck node. T_{fd} is the feedback time.

The critical charge can also be defined as a charge stored on the capacitance of the struck node [6]:

$$Q_{\text{crit}} = C_N * \Delta V_N + \int_0^{T_{\text{fd}}} I_{\text{ds}_\text{p}} dt \tag{2}$$

where

C_N total capacitance of the node;

ΔV_N change in gate voltage of the struck transistor during T_{fd};

I_{ds_p} pMOS drain conduction current in the struck inverter.

The Q_{crit} decreases with scaling as expected due to the decrease in the cell capacitance (C_N) and the supply voltage ($Q_{\text{crit}} \alpha C_N V_{dd}$). However, the critical LET shows a very interesting turnaround effect, as illustrated in Fig. 3. The LET value reaches a minimum at $L_g = 0.18$ μm and then starts increasing with decrease in device dimension. In fact, the LET value at 0.09 μm is comparable to that of a 0.5 μm device. We have also monitored the charge collected at the source node. Fig. 4 indicates a significant increase in the source charge collection for $L_g < 0.18$ μm. The negative charge for 0.35 and 0.5 μm essentially indicates the presence of parasitic bipolar effect in these devices, as illustrated in Fig. 5. For $L_g < 0.18$ μm, a significant fraction of radiation-generated charge is collected by the source and, hence, does not contribute to the flipping of the drain node. Therefore, even though Q_{crit} is lower for the smaller gate-length transistors, the LET increases due to the fact that the efficiency of the radiation charge to cause SEU decreases. In fact, the source effect on the LET has been explained explicitly in a paper by Castellani-Coulie *et al.* [7] that states that the source junction competes for charge collection with the drain when the striking location shifts toward the source and,

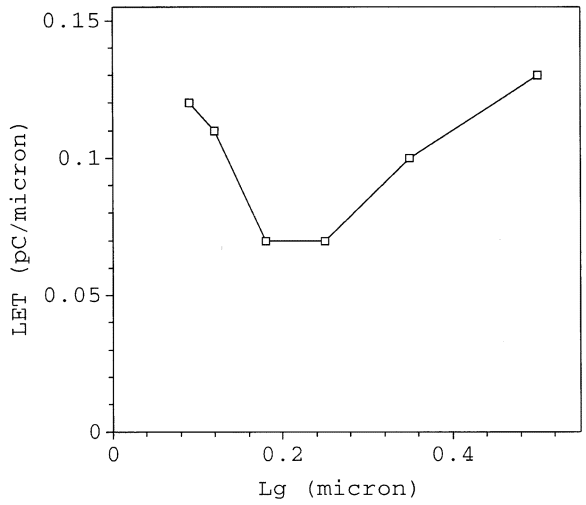

Fig. 3. LET variation with the L_g showing the turnaround effect after $L_g \leq 0.18$ m.

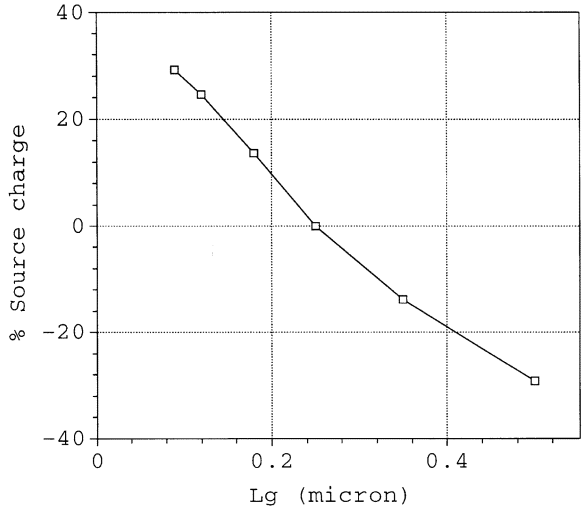

Fig. 4. Percentage source charge at each technology node. Negative value indicates the presence of bipolar injection effect in transistors for $L_g \geq 0.35$ μm.

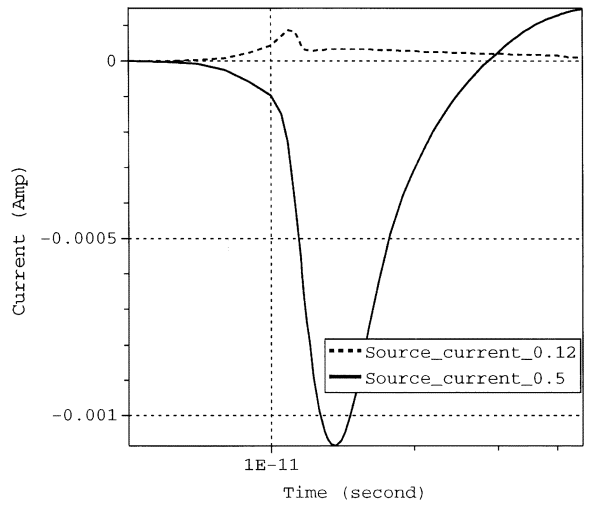

Fig. 5. Source current for the 0.5- and 0.12-μm devices. The negative current for the 0.5-μm device indicates electron injection from source to substrate.

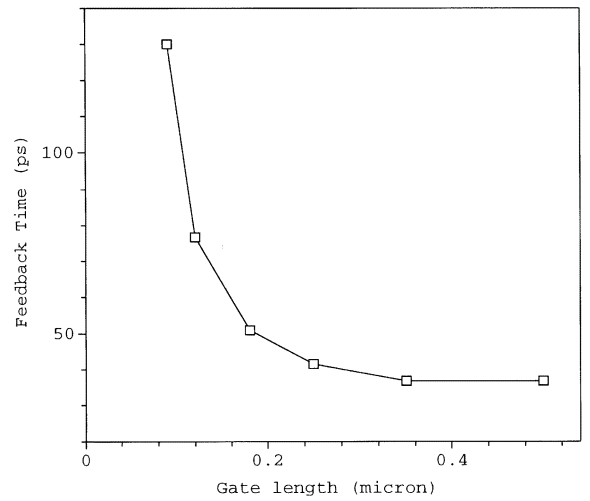

Fig. 6. Feedback time variation with the gate length for the radiation striking at the drain–gate edge.

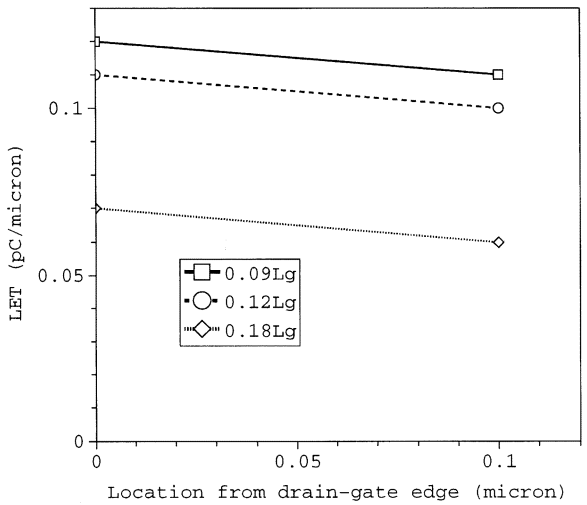

Fig. 7. LET variation with the striking position.

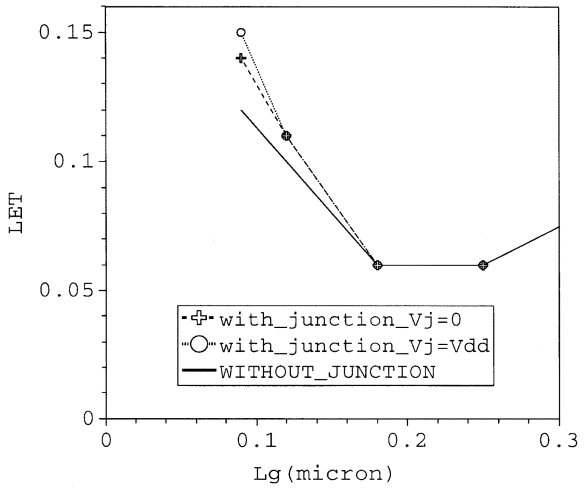

Fig. 8. Inclusion of an extra n+ junction representing the drain of an adjacent SRAM cell results in a change of LET value for the $L_g \leq 0.12$ μm for both $V_j = 0$ and $V_j = V_{dd}$.

hence, the upset threshold increases. Fig. 6 demonstrates the $T_{\rm fd}$ variation as a function of gate length. A very sharp increase in $T_{\rm fd}$ for $L_g < 0.18$ μm indicates the lowering of the prompt charge amount collected at the drain node.

The effect of different striking locations on LET is also evaluated. The striking location is moved away from the source to a point 0.1 μm from the drain–gate edge. Fig. 7 shows the LET value for $L_g \leq 0.18$ μm SRAM as a function of the striking location. Since the influence of the source decreases slightly, the LET decreases for a striking location of 0.1 μm. The effect of the neighboring junction from the adjacent SRAM cell is evaluated in Fig. 8 as a function of the junction voltage V_j. An increase in the LET value due to the charge sharing is evident for both $V_j = 0$ and $V_j = V_{dd}$.

It is important to visualize the significance of turnaround effect on the critical LET. For example, an aluminum ion with the impinging energy of 3.41 Mev is able to flip the memory cell of gate lengths 0.25 and 0.18 μm. The stopping power (LET) of silicon for an aluminum ion with the given energy is equal to the simulated LET value, 0.07 pC/μm (7 MeV cm^2/mg) and, hence, is sufficient to flip the memory cell of the given gate lengths [8]. Due to the turnaround effect in LET, the same aluminum ion does not have sufficient LET to flip the memory cell of gate lengths 0.12 and 0.09 μm. This fact essentially demonstrates the SEU immunity with the scaling in the DSM regime, even though the critical charge decreases.

IV. Conclusion

A systematic simulation-based design and characterization of the SEU phenomenon as a function of technology scaling is performed. Even though the critical charge decreases with scaling in the sub-0.18-μm regime, the external manifestation of the single event reliability shows an opposite trend. The LET increases with the scaling in this regime. This phenomenon is explained based on the source proximity influence on the source-side charge collection (SSCC). The trends in the feedback time, the impact of striking location on LET, and the effect of the adjacent junction corroborate this finding. The significance of this observation is described with an example.

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