Response Surface Modeling of 100nm CMOS Process Technology using Design of Experiment

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Abstract

100nm CMOS technology has been characterized through Design of Experiment (DOE) and statistical modeling. Initially, a set of 21 process parameters (factors) have been identified to determine their impact on transistor performance metrics such as threshold voltage V_t, sub-threshold slope SS, drive current I_{ddrive}, *leakage current* I_{dleak}, both in saturation and linear region. Through first order linear modeling of V_t, *SS*, I_{ddrive}, and I_{dleak}, *a subset of 10 most significant process parameters are picked using Plackett-Burman screening experiment for both NMOS and PMOS devices. Significant process parameters which impact the device characteristics are seen to be different, for NMOS and PMOS devices, inspite of a common process flow. Response surfaces (RS) have been built in terms of these 10 parameters for NMOS device. Statistical parameters of the device characteristics fluctuations like mean*(μ) *and standard deviation* (σ) *for* V_t, SS, I_{ddrive}, I_{dleak} and G_m *(maximum transconductance), have been determined by Monte carlo (MC) analysis of these response surfaces. Application of the Transmission of Moment Technique (TMT) on these models is shown to be a simple means to determine* μ *and* σ *of the device characteristics, with simple mathematical calculations.*

Keywords – Disposable spacer, Sensitivity analysis, CMOS technology, Transmission of moments technique, Statistical modeling, Plackett-Burman design, Response surface methodology, Monte carlo analysis.

1. Introduction

The transistor mismatch due to random variations in process parameters has become one of the major issue in the DSM technology. The term transistor mismatch refers to the fact that supposedly identical transistors at the design phase come out as distinct devices after manufacturing [1] due to statistical process variations. The process variations influence the transistor output parameters which in turn have a significant impact on circuit performance and yield [2–4]. The transistor mismatch effect will become worse in the future due to demanding requirement on process tolerance. The International Technology Roadmap for Semiconductors (ITRS) expects to reduce the overall cost of manufacturing of the Deep Sub-Micron (DSM) ICs by 35% in the future, by the use of TCAD-tools [5]. The manufacturing yield of a technology is a strong function of statistical process variations. In order to decrease the Short Channel Effect (SCE), in DSM devices, additional process steps are involved. This increases the complexity in device design and process control. The statistical distribution of transistor parameters can be evaluated, in principle, through rigorous Monte Carlo analysis by accounting for the random statistical distribution of parameters of various processes such as lithography, oxidation, implantation etc. However this technique demands a lot of computing resources [6]. Hence it becomes essential to come up with a computationally efficient modeling technique for characterization.

In this work, we have initially explored a 21 dimensional parameter space to investigate the relative significance of each parameter for 100nm CMOS technology. Next, we have considered top 10 significant parameters that most influence the device behavior. Finally, second order response surfaces for NMOS device characteristics have been determined in terms of the corresponding 10 significant process parameters, which will enable the process engineering and manufacturing team to track the process and monitor for the desired target and minimum variability. In Section II, we discuss the principles of statistical modeling, in section III, design of 100nm NMOS and PMOS. Section IV describes the process characterization for 100nm CMOS using screening DOE technique. In section V, a detailed response surface study is performed in terms of the 10 key process parameters and MC and TMT are applied on these response surfaces to evaluate the mean and total variability of responses. In Section VI, we conclude with the discussion on, the techniques used and the results that are obtained.

2. Modeling Methodology

Plackett-Burman DOE [7, 8] with 28 runs for a maximum of 27 variables have been performed as screening experiment for the initial study of the CMOS process. A first

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order model for a response y, with 21 variables is of the form [8]

$$y=b_0 + b_1x_1 + b_2x_2 + \ldots + b_{21}x_{21} \quad (1)$$

where b_0 is a constant, x_is are the normalized process parameters varying between -1 to +1, and b_is are the corresponding fitting constants determined by the data obtained from the screening experiment, for i=1…21, as shown in Table 1. The magnitude of b_i in equation 1 indicates the relative significance of the corresponding x_i, as these x_is are normalized between -1 to +1, with respect to their 3σ.

As a case study, second order response surfaces [8, 9] have been built using DOE, for NMOS device in terms of the 10 significant parameters. Remaining 11 parameters are set at their nominal values. The models fitted to data from a suitable DOE, contain a constant term, main factor terms, all possible two factor interaction terms and quadratic terms. Thus any response represented as a second order model will have a total of 66 terms for 10 factors, which will be of the form

$$y=\beta_0 + \beta_1x_1 + \beta_2x_2 + \ldots + \beta_{10}x_{10} + \beta_{12}x_1x_2 + \beta_{13}x_1x_3 + \ldots + \beta_{23}x_2x_3 + \beta_{24}x_2x_4 + \ldots + \beta_{910}x_9x_{10} + \beta_{11}x_1^2 + \beta_{22}x_2^2 + \ldots + \beta_{1010}x_{10}^2 \quad (2)$$

where β_0 is a constant, x_is are the most significant factors as determined from screening experiment, varying between -1 to +1, and β_is are the corresponding fitting constants determined by the data obtained from the response surface DOE, for i=1…10. In general, response y can be any of the device characteristics, V_t, SS, I_{ddrive}, I_{dleak} and G_m, in either linear or saturation region. Equation 2 can now be used in MC loop to determine the mean and variance of any response with 10 factors, which are assumed to be normal random variables. When the RS modeling is performed, TMT [6, 10] on these models, can readily obtain μ and σ of the device parameters. According to TMT, any nonlinear relation $y = f(x_1, x_2, ...x_N)$ between a dependent response variable y and independent variables $x_1, x_2, ...x_N$ can be approximated as a truncated Taylor's series.

$$y = f(\mu_{x_1}, \mu_{x_2}, \ldots \mu_{x_N}) + \sum_{i=1}^{N} \frac{\partial f}{\partial x_i} \Delta x_i \quad (3)$$

where μ_{x_i} is the mean value of the ith process parameter. According to the TMT, mean of the response, y is

$$\mu_y = f(\mu_{x_1}, \mu_{x_2}, \ldots \mu_{x_N}) \quad (4)$$

and the variance of y is,

$$\sigma_y^2 = \sum_{i=1}^{N} (\frac{\partial f}{\partial x_i})^2 \sigma_{x_i}^2 + 2\sum_{i=1}^{N} \sum_{j=i+1}^{N} \frac{\partial f}{\partial x_i} \frac{\partial f}{\partial x_j} \rho_{x_i x_j} \times \sigma_{x_i} \sigma_{x_j} \quad (5)$$

where $\sigma_{x_i}^2$ is the variance of x_i and $\rho_{x_i x_j}$ is the correlation between the variable x_i and x_j. In equation 3 and 5, partial derivatives are taken about the nominal point of the process parameters. If x_is are statistically independent then the second term in equation 5, vanishes.

3. Design of nominal NMOS and PMOS device

We have used Integrated System Engineering-Technology Computer Aided Design (ISE-TCAD) tool in the implementation of this work [11]. In realizing the nominal 0.1μm NMOS and PMOS (without silicidation) device of Figure 1, we have followed the technique outlined in [12–15]. A detailed process flow followed in DIOS-ISE process simulation which accounts for the initial 21 parameters is given in Table 1. The definition of the gate length appears at the top of the simulation command file, as it appears first, in Table 1. The shallow extension/deep junction depth for NMOS and PMOS transistor are 0.04μm/0.1μm and 0.05μm/0.15μm respectively. The gate source/drain (s/d) overlap is maintained at about 15nm for the parasitic series resistance considerations. The gate length L_g=0.1μm (metallurgic channel length, L_{met}=0.07μm), oxide thickness T_{ox}=20Å and these devices has been simulated at a supply voltage, $|V_{ds}|$=1.5V. Figure 2 shows the $I_d - V_{gs}$ characteristics simulated in the saturation ($|V_{ds}|$=1.5V) and linear ($|V_{ds}|$ = 50mV) region for the NMOS and PMOS devices. DESSIS-ISE has been used for device simulation. An interface trap density of $5 \times 10^{10}/cm^2$ is applied at the Si/Oxide boundary during the simulation. For NMOS the saturation/linear region, V_t=0.233/0.31V, SS=85.8/83.6mV/dec, I_{ddrive} = 0.91/0.124mA/μm, I_{dleak}=0.69/0.064nA/μm and G_m=0.92/0.14mS/μm. The respective quantities for PMOS are 0.23/0.26V, 84.1/84.0mV/dec, 0.33/0.034mA/μm, 0.93/0.29nA/μm and 0.35/0.04 mS/μm respectively. The V_ts that are indicated above are the constant current V_t (@$40nA \times (W/L_g)$, with W=1μm and L_g=0.1μm).

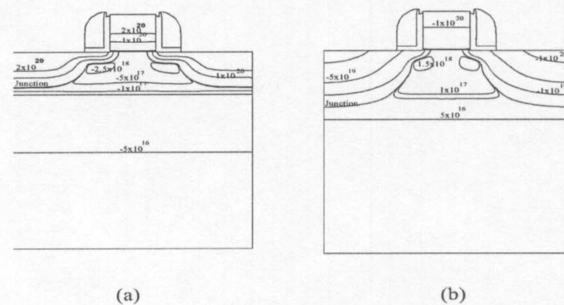

Figure 1. Process simulated (a)NMOS and (b)PMOS devices, contours of doping concentration can be seen

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Table 1. Symbolic representation of the 21 process parameters, respective model coefficients in equation 1, their nominal and 3σ values. Values in the parentheses pertain to PMOS. coeff=model coefficient, SSRC=super steep retrograde channel, LDD=light doped drain, RTA=rapid thermal anneal.

factors	coeff	factor description	3σ
Lg	b_1	gate length=0.1(0.1)μm	0.01(0.01)μm
initoxtemp	b_2	10nm screening oxide @T=900(900)^{o}C	10(10)^{o}C
ztiltdose	b_3	0° implant B(P) dose=2(2) $\times 10^{12}/cm^2$	0.2(0.2) $\times 10^{12}/cm^2$
ztiltenergy	b_4	0° implant energy=200(400)keV	20(40)keV
tiltdose	b_5	7° implant B (P) dose=1(2) $\times 10^{12}/cm^2$	0.1(0.2) $\times 10^{12}/cm^2$
tiltenergy	b_6	7° implant energy=100(200)keV	10(20)keV
ssrc_dose	b_7	In(Sb) SSRC dose=5.7(5.7) $\times 10^{12}/cm^2$	0.57(0.57) $\times 10^{12}/cm^2$
ssrc_energy	b_8	In(Sb) SSRC energy=146(186)keV	14.6(18.6)keV
goxtemp	b_9	gate oxidation @T=800(800)^{o}C	10(10)^{o}C
reoxtemp	b_{10}	poly-reoxidation @T=800(800)^{o}C	10(10)^{o}C
spnithick1	b_{11}	spacer thickness=96(96)nm	9.6(9.6)nm
deep_dose	b_{12}	deep s/d As(B) dose=6(1) $\times 10^{15}/cm^2$	0.6(0.1) $\times 10^{15}/cm^2$
deep_energy	b_{13}	deep s/d energy=30(5)keV	3(0.5)keV
anneal_temp1	b_{14}	20s anneal @T=1050(1050)^{o}C	10(10)^{o}C
ldd_dose	b_{15}	LDD As(B) dose=1(0.1) $\times 10^{15}/cm^2$	0.1(0.01) $\times 10^{15}/cm^2$
ldd_energy	b_{16}	LDD energy=7(1)keV	0.7(0.1)keV
halo_dose	b_{17}	halo B(P) dose=6.65(5.85) $\times 10^{12}/cm^2$	0.665(0.585) $\times 10^{12}/cm^2$
halo_energy	b_{18}	halo energy=10(25)keV	1(2.5)keV
halo_tilt	b_{19}	halo tilt =30(30)^o	3(3)^o
anneal_temp2	b_{20}	4s anneal @T=1050(1050)^{o}C	10(10)^{o}C
spnithick2	b_{21}	final spacer thickness=40(40)nm	4(4)nm

Table 2. Coefficients of first order model for NMOS (PMOS).

coeff	V_{tsat} $\times 10^{-3}$	SS_{sat}	$I_{dsatdrive}$ $\times 10^{-6}$	$I_{dsatleak}$ $\times 10^{-9}$
b_0	220(180)	87.6(82.4)	940(420)	5.4(15.5)
b_1	24(2.4)	-3.24(-0.9)	-110(-13)	-4.5(-7.9)
b_2	8.2(-0.12)	-0.19(-0.52)	12.9(6)	-2.7(2.6)
b_3	1.5(-0.63)	0.05(-0.52)	-5(3)	2(5.6)
b_4	-1.3(-5.1)	-0.09(-0.19)	13.5(2.4)	-1.1(1.8)
b_5	1(-1.3)	0.12(-0.3)	-15.8(1.2)	-2.1(-4)
b_6	0.14(-4.1)	-0.22(-0.69)	13(4.6)	2.3(1.5)
b_7	7(8)	-0.24(-0.19)	-7.6(-8.7)	-2.2(-7.9)
b_8	-24(-10)	0.88(1.42)	2(5)	3.6(-2.5)
b_9	10(7)	0.61(0.62)	8.3(-5.3)	-1.2(2.8)
b_{10}	7(9.5)	0.6(0.52)	-53.6(-14)	1.9(-1.1)
b_{11}	0.72(35)	0.22(0.86)	-22(-39)	-2.1(-13.6)
b_{12}	-2.6(-21)	-0.26(-0.87)	23.6(22)	1.6(9.5)
b_{13}	-1.2(-1.4)	-0.08(0.05)	19.9(2.2)	1.5(1.9)
b_{14}	-2.6(-23)	-0.48(-0.98)	47.1(24)	1.9(12.4)
b_{15}	-8.7(-13)	0.3(0.75)	16.9(14)	2.7(7.8)
b_{16}	-4.8(-4.2)	0.31(0.59)	5.2(7.4)	3.1(-0.02)
b_{17}	21(22)	-0.1(0.23)	-24.7(-18)	-2.7(-4.4)
b_{18}	16(9.5)	-0.56(-0.54)	-29.5(-6.8)	-3.5(-3.4)
b_{19}	28(28)	-0.62(-0.03)	-38.7(-17)	-3.9(-6.7)
b_{20}	-25(-14)	1.23(0.49)	38.1(14)	3.7(10)
b_{21}	-1.4(-5.6)	0.17(-0.1)	-7.2(4)	-1(4.7)

Table 3. Top 10 statistically significant process parameters for NMOS and PMOS.

Rank	NMOS	PMOS
1	Lg	spnithick1
2	halo_tilt	anneal_temp1
3	anneal_temp2	deep_dose
4	ssrc_energy	halo_tilt
5	halo_energy	anneal_temp2
6	halo_dose	ldd_dose
7	reoxtemp	halo_dose
8	ldd_dose	Lg
9	Initoxtemp	ssrc_dose
10	anneal_temp1	ztiltdose

Table 4. Statistics that are obtained by MC and TMT calculations on the response surfaces.

Device parameters	MC		TMT	
	Mean	σ	Mean	σ
V_{tsat}(V)	0.243	0.019	0.246	0.018
V_{tlin}(V)	0.316	0.014	0.319	0.014
SS_{sat}(mV/dec)	87.06	1.367	87.0	1.33
SS_{lin}(mV/dec)	84.64	0.949	84.7	0.93
$I_{dsatdrive}$(μA/μm)	832	58.4	820	53.4
log[$I_{dsatleak}$A/μm]	-21.2	0.41	-21.3	0.4
$I_{dlindrive}$(μA/μm)	113	5.1	112	4.1
log[$I_{dlinleak}$A/μm]	-23.6	0.394	-23.65	0.38
G_{msat}(mS/μm)	0.869	0.05	0.86	0.047
G_{mlin}(mS/μm)	0.138	0.007	0.14	0.005

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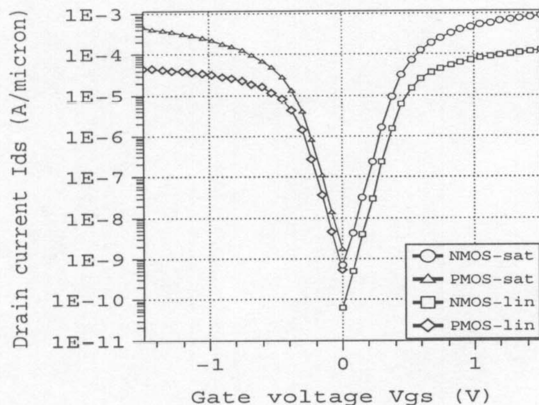

Figure 2. $I_d - V_{gs}$ characteristics of NMOS and PMOS devices in the linear and saturation region

4. Screening experiment for characterizing 100nm CMOS process

Plackett-Burman DOE with 28 runs for a maximum of 27 variables, have been performed as screening experiment for the initial study of the CMOS process. The number of process parameters that are investigated by this DOE are 21, which are tabulated in Table 1 with their description (quantities in the parentheses, pertains to PMOS). The standard design matrix for Plackett-Burman experiment with a maximum of 27 variables with 28 runs can be found in [7, 8]. The experiment has been performed by assigning 21 process parameters to each column of the standard design matrix (omitting the last 6 columns). The whole experiment has been repeated 4 times by changing the process parameter allocation to columns of the design matrix. Model coefficients of equation 1 are determined by single regression of the results from all the 4 experiments. This is essential only to increase the effectiveness of the screening experiment in properly deciding the significance (in terms of rank) of the 21 parameters under study. The first order model coefficient in equation 1 for V_t, SS, I_{ddrive} and I_{dleak} in saturation region, obtained from this DOE are listed in Table 2 for NMOS and PMOS (in parentheses). Note that the subscript, d=drain, sat=saturation, lin=linear, drive=on-state and leak=leakage, in the further discussion. e.g V_{tsat}=V_t in the saturation region, $I_{dsatdrive}$=on-state drain current in the saturation region, etc. Equation 1 should not be used for extensive study except for determining the significance of the factors, because it is taking only the approximate first order effect of the process parameters. For a detail study of the process, with respect to these factors, one has to use response surface DOE and modeling, which will be discussed in the next section. The magnitude of the model coefficients will indicate the relative significance of the corresponding process parameter. This procedure helps in picking a subset of significant factors out of initial 21. Table 3 is the list of top 10 ranking factors for NMOS and PMOS device. It can be seen that this subset is not common between NMOS and PMOS devices, as the boron and arsenic diffusivity is different in silicon, even though the process flow is common, which have the direct impact on the SCE in the devices.

5. Response surface modeling, Monte carlo and Transmission of moments analysis

The response surface modeling, has been performed by using Face Centered Central Composite (FCCC) Design [8, 9, 16] on the 10, key process parameters of Table 3, for NMOS device. This design is a highly fractionated 3 level DOE for fitting second order response surfaces. For 10 factors, a fraction of 1045 experiments have been chosen, out of a large set of 3^{10}(=59049) full factorial design. The process parameters under consideration are varied by $\pm10\%$ except temperatures, which are varied by $\pm10^oC$, about their nominal values. It is assumed that $\pm10\%$ or $\pm10^oC$, corresponds to $\pm3\sigma$ variation in the process under study. A total of 1045 process and 1045 device simulations have been performed. The tool flowchart that has been used in GENESISe framework is shown in Figure 3.

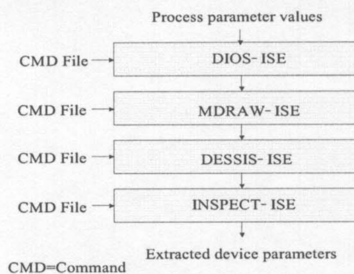

Figure 3. GENESISe tool flow chart for statistical modeling

GENESISe, [11] also called the work bench of ISE-TCAD tool is used to construct project and run, automatically. DIOS-ISE has been used to process simulate the devices and DESSIS-ISE, for device simulation. A boundary/doping editor tool MDRAW-ISE has been used to build mesh automatically. INSPECT-ISE has been used for automatic extraction of the simulation results. The second order models that have been obtained by the regression technique using simulation results are long polynomials, in the form of equation 2. The device parameters that have been modeled are V_t, SS, I_{ddrive}, I_{dleak} and G_m, in the saturation and linear region. These models have been tested for their validity to predict the response values, by substituting the same combination of the factor levels that have been used in the response surface DOE. The original experimental response and the model predicted response correlate very well with the correlation coefficient, $r > 0.9$.

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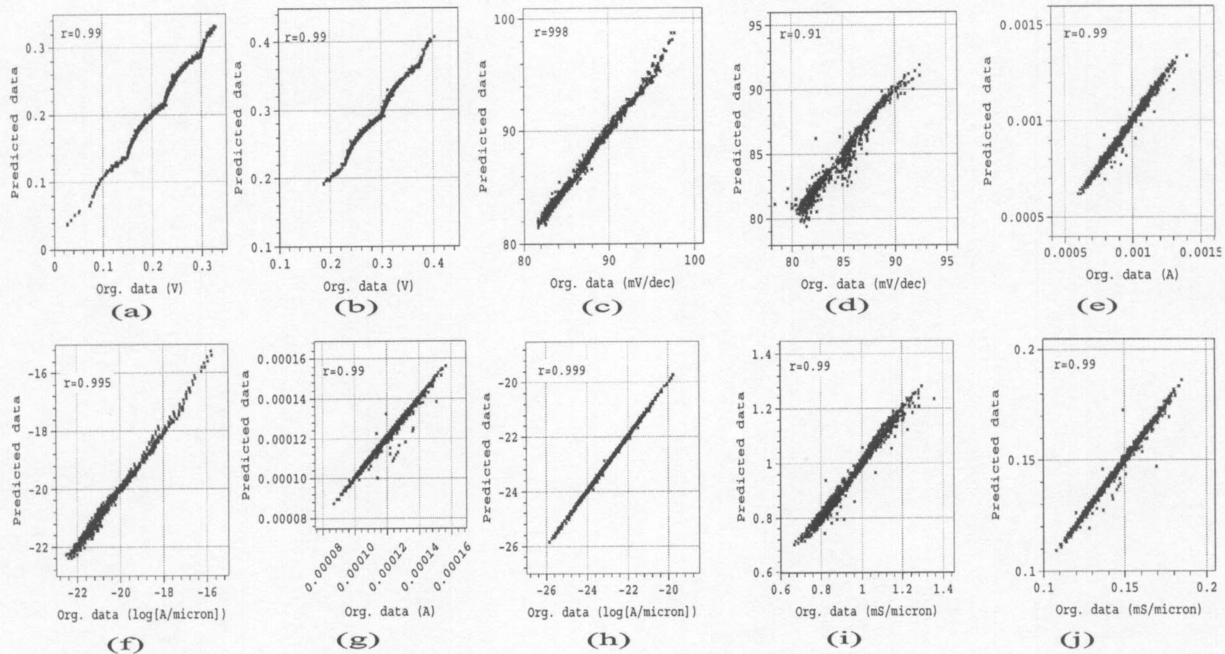

Figure 4. The correlation plots of the statistical model between the original DOE data and the model predicted data for (a)V_{tsat}, (b)V_{tlin}, (c)SS_{sat}, (d)SS_{lin}, (e)$I_{dsatdrive}$, (f)$I_{dsatleak}$, (g)$I_{dlindrive}$, (h)$I_{dlinleak}$, (i)G_{msat}, and (j)G_{mlin}. The correlation coefficients are also depicted for each plot

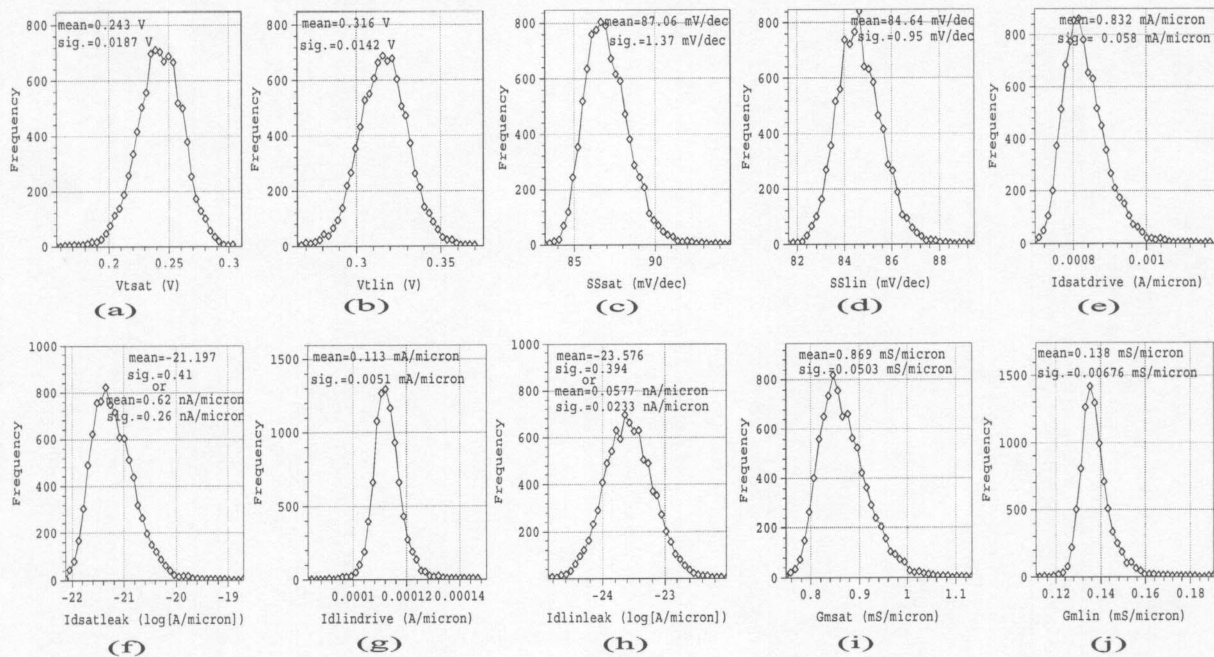

Figure 5. Statistical distributions that are obtained by the MC calculations on the models for (a)V_{tsat}, (b)V_{tlin}, (c)SS_{sat}, (d)SS_{lin}, (e)$I_{dsatdrive}$, (f)$I_{dsatleak}$, (g)$I_{dlindrive}$, (h)$I_{dlinleak}$, (i)G_{msat}, and (j)G_{mlin}. The μ and σ for each of these quantities are also shown on each plot

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Correlation plots for these device parameters along with their correlation coefficient r, are depicted in Figure 4. In modeling the leakage currents, logarithmic transformation have been used, as the range of variation of these quantities with factor levels were too large, and also to improve the model fitting [8]. Therefore the model predicted data for leakage currents must be inverse transformed to interpret, with proper units. In order to study the statistical nature of 0.1μm process with respect to 10 key parameters, that are selected, we have generated 9000 normally and independently distributed pseudo-random (PR) numbers for each of these 10 key process parameters with μ equal to their nominal values and σ equal to 3.33% ($= \frac{10}{3}\%$) of their nominal values. The σ value for the temperature parameters are 3.33°C ($= \frac{10}{3}^{o}$C). Model equation for, V_t, SS, I_{ddrive}, I_{dleak} and G_m, in the saturation and linear regions are run in a Monte carlo loop by plugging in these PR numbers. The resulting distribution of these models for the corresponding device parameters are portrayed in Figure 5, along with the resulting μ and σ values. The values of σ for the saturation region quantities are compared with that in the literature [6] that are available for implant dose fluctuations alone. The variability that has been observed in our study is 3 to 4 times more than that, as a result of the device parameters being too sensitive to the fluctuations in the process parameters under consideration.

Finally, we have applied TMT on these models to evaluate μ and σ. The statistics that are calculated from the MC and TMT, are shown in Table 4, which match very well. In order to further validate the illustrated technique, in terms of accuracy and computational efficiency, we are currently pursuing, rigorous Monte carlo process and device simulation.

6. Conclusions

Characterization of 100nm CMOS process has been performed on a large set of 21 process parameters, through screening experiment. Response surface study on a subset of 10 key parameters has been performed to assess the total variability (mismatch) of several NMOS device parameters. In calculating the mismatch, we have used standard techniques like, MC and TMT. The results are compared with that available in the literature for implant dose fluctuations alone. These 10 key parameters are causing nearly 3 to 4 times the fluctuations arising from implant doses. The mismatch that is arising from the process has direct impact on circuit delay fluctuations, causing switching errors in the circuit.

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