A UNIFIED MODEL FOR THE ZVS DC-DC CONVERTERS WITH ACTIVE CLAMP

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Abstract

Active clamp dc-dc converters are recently introduced family of two switch pulse width modulated converters featuring zero-voltage switching. The topological structure of these converters in relation to their hard-switched PWM converters is highlighted. With proper designation of the circuit variables (throw voltage V and the pole current I), all these converters are seen to be governed by an identical set of equations. In this framework, these circuits exhibit 6 sub-periods per cycle with identical current waveform in the resonant inductor. With idealized switches, the steady-state performance is obtainable in an analytical form. This set of equations may be solved through a simple spreadsheet programme. The steady-state performance provides a design constraint on the normalized current. The conversion ratio of the converter is also readily available. A generalized equivalent circuit emerges for all these converters from this steady-state conversion ratio. It is interesting to note that this equivalent circuit provides a dynamic model as well. The circuit model proposed in this paper enables one to use the familiar state space averaged results of the standard PWM dc-to-dc converters (both steady-state and dynamic) for their ZVS active clamp counterparts.

1 *Introduction*

Single ended active clamp converters are becoming popular for compact dc-dc converters switching at frequencies beyond 100KHz. The analysis of such converters has been presented with different topologies and different levels of approximation [1]. The realization of ZVS active clamp variation for many of the dc-dc converter topologies has also been presented in the past[2]. Such proliferation of converters with variable frequency control under the classification of quasi-resonant converter has also been reported earlier. The unified model of all quasi-resonant converters was brought out elegantly in a paper in 1987[3].

The present paper identifies such a unified performance results of the ZVS active clamp converters. This is done by defining a normalized current (I_N) through the pole current (I), throw voltage (V), and the switching period (Ts) of the switch[4]. With such a definition, the circuit intervals and the defining equations become identical in all the ZVS active clamp dc-dc converters. In the sections that follow the method of analysis is outlined through the example of Buck converter with active clamp. The circuit -Topologies in the sub-interval and the solution for the same under idealized operation are derived Equivalent circuits valid for steady state as well as dynamic performance is proposed.

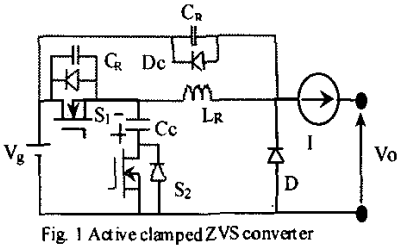

Fig. 1 Active clamped ZVS converter

Fig. 1 shows the active clamped ZVS buck converter. This circuit is obtained from the hard-switched buck converter with the additional circuit elements added as shown in fig. 2.

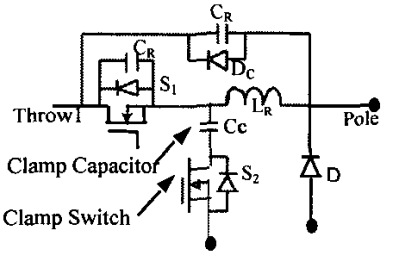

Fig. 2 Additional elements in the active clamped buck converter

The rules for the additional elements are as follows.

1. C_R in parallel with the Main switch S_1
2. L_R in series with the switch S_1
3. C_R and D_C in parallel with the switch and inductor ($S_1 + L_R$)
4. Clamp capacitor C_c and Clamp switch S_2 from the midpoint of S_1 and L_R to Clamp point. Any fixed voltage point can serve as a clamp point.

2. *Principle and operation of active clamp buck converter*

The ZVS buck converter with active clamp, illustrated for analysis here is presented in fig. 3.

The operation of the circuit follows sequentially the sub-circuits shown below.

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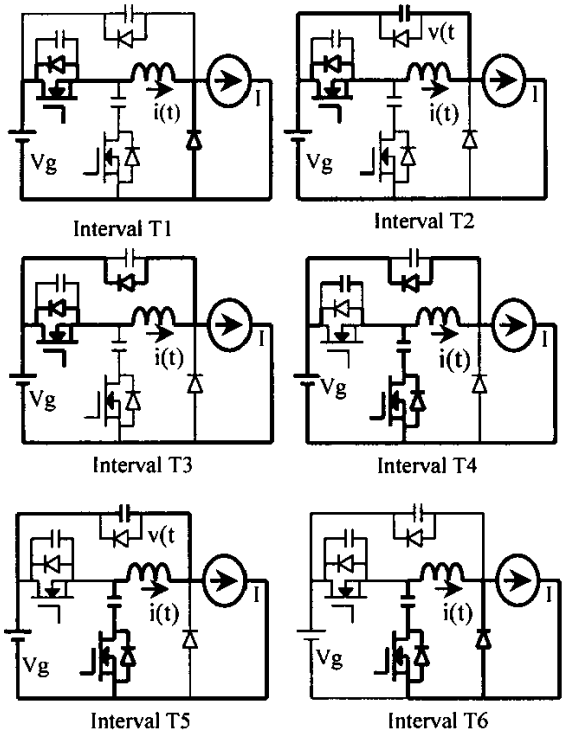


Fig. 3 Active clamped ZVS buck converter with its 6 sub-periods over a period

The ZVS buck converter with active clamp, illustrated for analysis here is presented in fig. 3, along with idealized waveforms. The operation of the circuit follows sequentially the sub-circuits shown above.

Interval T1 starts when the main active switch turns on following the freewheeling state. This is followed by commutation of current from freewheeling diode (T2). In interval T3, the resonant inductor is freewheeling. At the end of T3, the main active switch is turned off. In interval T4, L_R loses its excess energy and after a short resonant interval T5, the circuit moves on to the freewheeling state. The simulated and the idealized waveforms of i(t) (current through L_R), capacitor current and the pole voltage waveforms are shown in fig. 4.

3 Steady-state performance analysis:

The analysis is done by solving the defining equations in each interval with appropriate initial conditions and finally equating the initial condition of first sub-period with the final conditions of the last sub-period.

Interval T1: Linear charging of inductor L_R

$$i(0)=-kI(T5);\ v(0)=V;$$

$$i(t)=-kI(T5)+\frac{V}{L_R}t;$$

$$T1=\frac{I+kI(T5)}{V}L_R;$$

Normalized current is defined in terms of pole current I, throw voltage V, and the switching period Ts.

$$I_N=\frac{L_R I}{V T_s};$$

Interval T2: Resonant charging of inductor L_R and discharging of C_R

$$i(0)=I\ ;\ v(0)=Vg$$

$$i(t)=I+V\sqrt{\frac{C_R}{L_R}}\sin\frac{t}{\sqrt{L_R C_R}};$$

$$v(t)=V\cos\frac{t}{\sqrt{L_R C_R}};\ v(T2)=0$$

$$T2=\frac{\pi}{2}\sqrt{L_R C_R}\ ;\ i(T2)=I+V\sqrt{\frac{C_R}{L_R}}$$

Interval T3: Resonant inductor L_R is freewheeling.

$$L_R\frac{di}{dt}=0\ ;\qquad i(t)=I+V\sqrt{\frac{C_R}{L_R}};$$

$$T1+T2+T3=DTs\ ;$$

Interval T4:

$$i(0)=I+V\sqrt{\frac{C_R}{L_R}};\ L_R\frac{di}{dt}=V+V_C;\ \frac{V_C}{V}\triangleq\beta$$

$$i(t)=I+V\sqrt{\frac{C_R}{L_R}}-\frac{V+V_C}{L_R}t;\qquad i(T4)=I;$$

$$T4=\frac{V}{V+V_C}L_R\sqrt{\frac{C_R}{L_R}};\ T4=\frac{1}{1+\beta}\frac{1}{2\pi f_R}$$

Interval T5: V, V_C, L_R, C_R form a resonant loop

$$i(0)=I\ ;v(0)=0;$$

$$i(t)=I-(V+V_C)\sqrt{\frac{C_R}{L_R}}\sin\frac{t}{\sqrt{L_R C_R}}\ ;$$

$$v(T5)=V=(V+V_C)\left(1-\cos\frac{T5}{\sqrt{L_R C_R}}\right);$$

$$I(T5)=I-V(1+\beta)\sqrt{\frac{C_R}{L_R}}\ ;$$

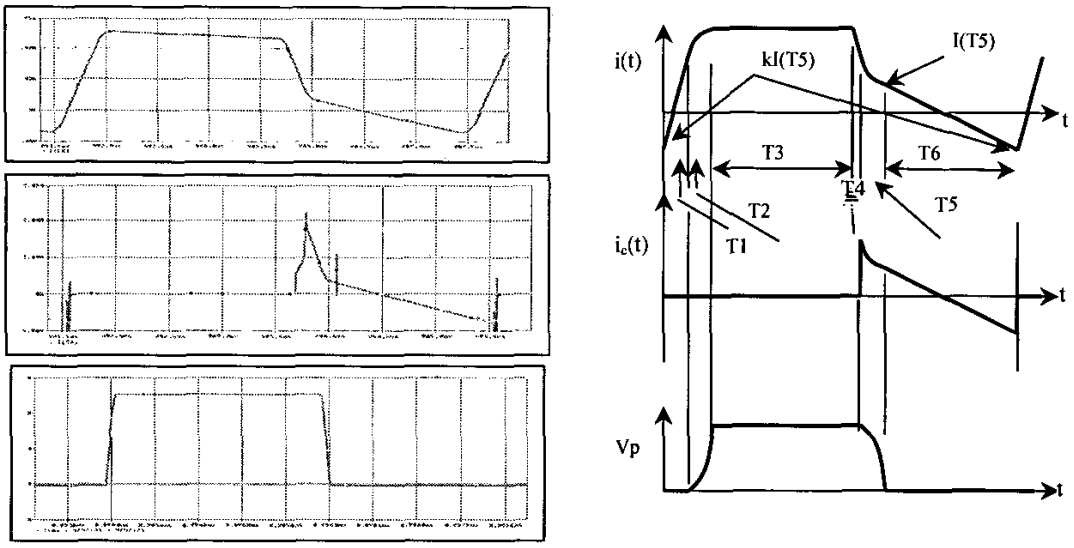


Fig. 4 Simulated & idealized resonant inductor current, clamp capacitor current and pole voltage waveforms

Interval T6: The inductor current drops from I(T5) to kI(T5) linearly in T6 with a rate of change of current of V_C/L_R. kI(T5) is the same current as the starting current in T1. With a few steps of calculation the following may be established. The power that flows into the clamp capacitor must be zero in a switching cycle for the operation to be steady. The voltage across C_c is constant, so its average current must be zero. Thus from $I_c(t)$ waveform we have:

$$Q(T4)+Q(T5)+Q(T6)=0;$$

$$IT4+\frac{VC_R}{2(1+\beta)}+IT5-VCR+\frac{I(T5)T6(1-k)}{2}=0;$$

$$k-1=\frac{2[(I(1-D)T_S-T_6)-\frac{VC_R(1+\beta)}{2}]}{I(T_5)T_6};$$

$$\beta=A\left(I_N-\frac{f_S}{2\pi f_R}\right);$$

$$A=\frac{(k+1)Ts/T6}{\left(1+\frac{k+1}{T6}\frac{1}{2\pi f_R}\right)};\ \text{Where}\ \beta=\left(\frac{V_C}{V}\right);$$

3.1 *Spread sheet organization table for steady state performance*

Starting with an initial value of V_C and kI(T5), one may compute sequentially through the 6 intervals to obtain a steady-state solution. A spreadsheet may be conveniently used for this purpose as shown in Table 1. The first guess for the initial current kI(5) and V_C are entered and re-entered from the computed values till convergence is obtained. The number of iterations is in most cases not more than 3.
Figure 5 shows the clamp ratio and conversion ratio as a function of the normal current I_N. Note the X-axis intercept in the clamp ratio ($f_S/2\pi f_R$).

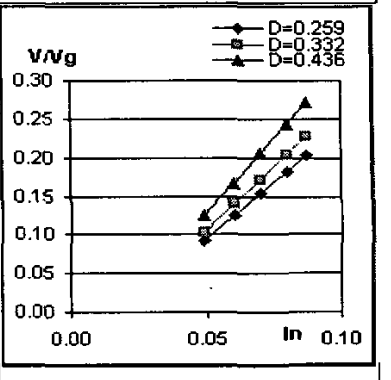
3.2 *Steady state conversion ratios:*

The conversion ratio $M=V_o/V_g$ can be evaluated by averaging the pole voltage over a full cycle. Under the assumption that the resonant frequency is much higher than the switching frequency, the conversion ratio for the buck converter is

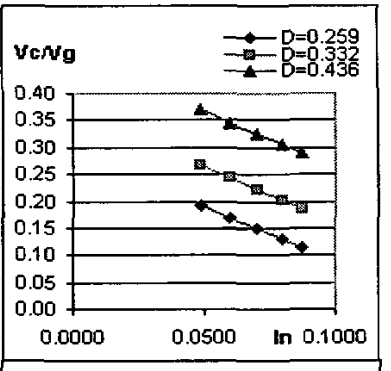
$$M=\frac{V_o}{V_g}=D-(1+k)I_N$$

Table 1: Spread sheet organization for steady–state performance solution

Inductor Current	I	1.95	2.4	2.8	3.2	3.5
Throw Voltage	V	50	50	50	50	50
Resonant Inductor	L_R	7.00E-06	7.00E-06	7.00E-06	7.00E-06	7.00E-06
Resonant Capacitor	C_R	1.00E-09	1.00E-09	1.00E-09	1.00E-09	1.00E-09
Resonant Freq r/s	W_R	1.41E+07	1.41E+07	1.41E+07	1.41E+07	1.41E+07
Resonant Freq Hz	F_R	2.22E+07	2.22E+07	2.22E+07	2.22E+07	2.22E+07
Switching Frequency Hz	Fs	2.50E+05	2.50E+05	2.50E+05	2.50E+05	2.50E+05
Switching Period	Ts	4.00E-06	4.00E-06	4.00E-06	4.00E-06	4.00E-06
Switch Initial Current	kI(T5)	1.40	1.87	2.30	2.72	3.03
Clamp Initial Voltage	VC	4.61	6.23	7.66	9.08	10.15
Current after T6	kI(T5)	1.40	1.87	2.30	2.72	3.03
Clamp Voltage	VC	4.61	6.23	7.66	9.08	10.15
Duty Ratio	D	0.259	0.259	0.259	0.259	0.259
S1 ON Time	DTs	1.04E-06	1.04E-06	1.04E-06	1.04E-06	1.04E-06
Dbar	1-D	0.741	0.741	0.741	0.741	0.741
Interval 1	T1	3.35E-07	4.27E-07	5.10E-07	5.92E-07	6.53E-07
Interval 2	T2	1.11E-07	1.11E-07	1.11E-07	1.11E-07	1.11E-07
Interval 3	T3	5.90E-07	4.98E-07	4.15E-07	3.33E-07	2.72E-07
Interval 4	T4	6.47E-08	6.29E-08	6.13E-08	5.98E-08	5.88E-08
Interval 5	T5	1.05E-07	1.03E-07	1.02E-07	1.00E-07	9.91E-08
Interval 6	T6	2.79E-06	2.80E-06	2.80E-06	2.80E-06	2.81E-06
Current after T5	I(T5)	1.18	1.61	1.99	2.37	2.66
Current Factor	k	1.18	1.16	1.15	1.14	1.14
Pole Voltage	Vp	9.65	8.51	7.48	6.46	5.70
Normal Current	I_N	0.05	0.06	0.07	0.08	0.09
Clamp Ratio	V_C/V	0.09	0.12	0.15	0.18	0.20
Voltage Ratio	V/Vg	0.19	0.17	0.15	0.13	0.11



Conversion ratio [Vo/Vg]



Clamp ratio [V_c/V_g]

Fig 5 Conversion ratio and Clamp ratio as a function of normalized current

Table 2

Definitions of Base voltage & current for the different Converters

	Buck Converter	Boost Converter	Buck-Boost Converter	Cuk Converter
V	Vg	Vo	Vg+Vo	Vg+Vo
I	Io	Ig	I_L	Ig+Io
R_d	$\frac{(1+k)L_R}{Ts}$	$\frac{(1+k)L_R}{Ts}$	$\frac{(1+k)L_R}{Ts}$	$\frac{(1+k)L_R}{(1-D)Ts}; \frac{(1+k)L_R}{DTs}$
M	$D-(1+k)I_N$	$\frac{1}{1-D+(1+k)I_N}$	$\frac{D-(1+k)I_N}{1-D+(1+k)I_N}$	$\frac{D-(1+k)I_N}{1-D+(1+k)I_N}$

3.3 *Equivalent circuits of active clamp ZVS converters*
The conversion ratio (Vo/Vg) shown for the buck converter in the table 2 may be simplified as follows:

$$\frac{V_o}{V_g} = D - I_N(1+k); \frac{V_o}{V_g} = D - \frac{L_R I(1+k)}{V_g T_s};$$

$$V_o = DV_g - \frac{L_R I(1+k)}{T_s};$$

This may be shown by the following equivalent circuit fig. 6

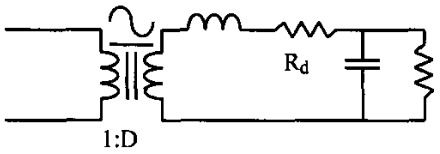


Fig. 6 Equivalent circuit of active clamp ZVS Buck

The interesting result is that the active clamped converters retain the qualitative nature of the hard-switched counterparts with additional lossless damping introduced in the equivalent circuit as shown in Fig. 6. The resonant sub-interval T1 introduces lossless damping to the predominantly second order dynamic model of the converter. This is very similar to the current dependent delay introduced in current programmed converter[5] .This damping resistance is R_d and is a function of resonant Inductor L_R and switching Frequency T_S. This simplification process may be done for all types of converters. The results on the conversion Ratio and damping resistance is given in table 2. The equivalent circuits for a few converters are given in fig. 7.

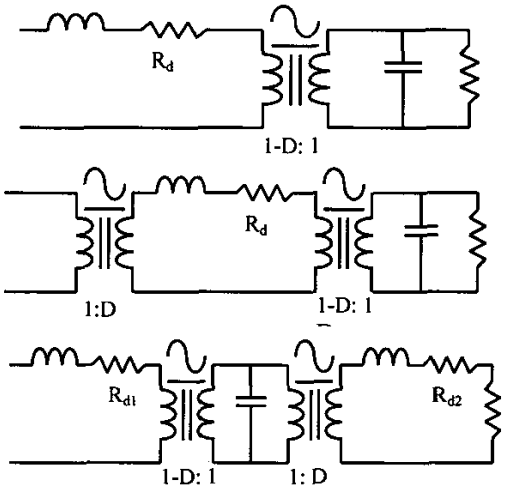


Fig. 7 Equivalent circuits of the active clamped ZVS boost, buck-boost and cuk converters

6 Small signal model:
The signal model is obtained by the basic assumption that the natural time constants of the converter network are much longer than the switching period. This assumption coincides with the requirement of small switching ripple. Hence, with this basic assumption, the resulting averaged model is obtained in the fig. 8 by averaging the converter waveforms over the switching period T.

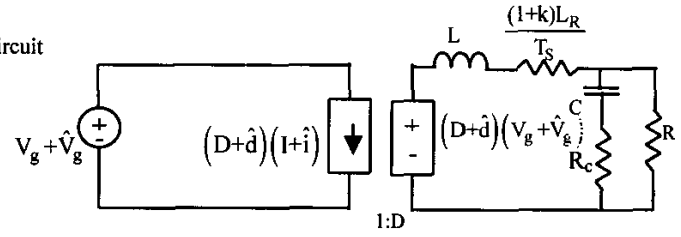


Fig. 8-a Perturbation of the nonlinear circuit averaged model about a quiescent operating point.

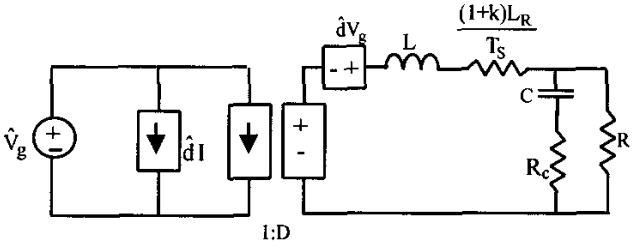


Fig. 8-b Lineralized circuit averaged model

The dependant linear sources are replaced by an equivalent ideal transformer, yielding the final small signal ac circuit averaged model.

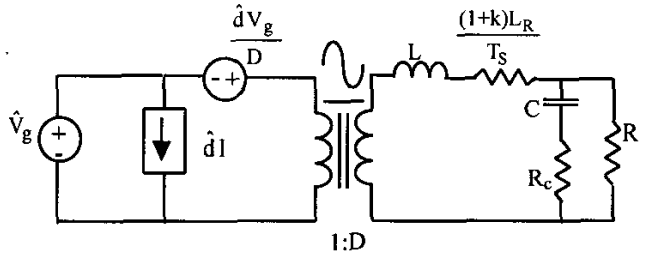


Fig. 8-c Small signal ac model of active clamp buck converter

Fig. 8 shows the averaged model of a active clamp ZVS buck converter obtained following the linear circuit reduction techniques[5]. Dynamic models are obtainable for the whole family of active clamp converters from the circuit models.

5 *Experimental results*

As a means of verifying the steady state model given in fig. 6 and the small signal model given in the fig. 8, an active clamp buck converter prototype is implemented. Following are the specifications of the prototype implemented.

Output power = 60 watts
Input voltage = 50 volts
Output voltage = 20 volts
Switching frequency = 250 KHz

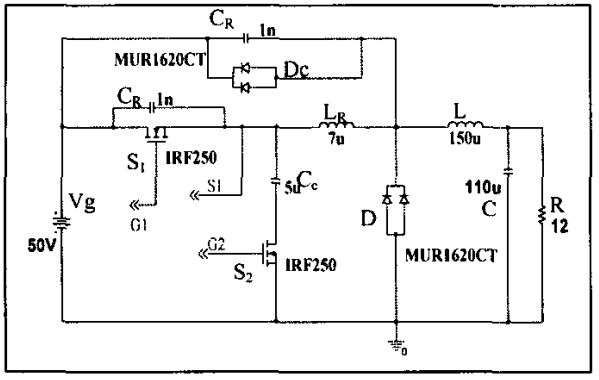


Fig. 9 Active clamp buck converter

Steady state performance results, dynamic model confirmation results, experimental waveforms of active clamp Buck converter are presented in section 5.1, section 5.2 and section 5.3 respectively.

C

5.1 *Steady state performance of the converter*

A set of design curves showing the relationship between DC conversion ratio [V_o/V_g] and Clamp ratio [V_c/V_g] as a function of normalized current obtained by spreadsheet design table in fig. 5 was experimentally verified and the results are as shown in the fig. 10-a and fig. 10-b respectively. They show good agreement with the theoretical obtained graphs with the spreadsheet design.

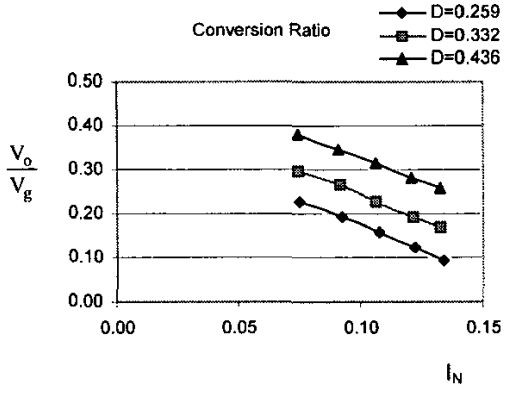


Fig 10-a DC Conversion ratio as a function of normalized current

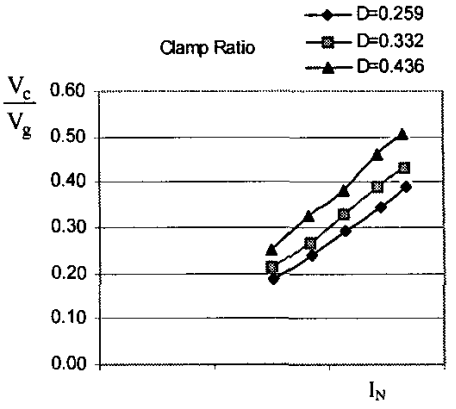


Fig 10b Clamp ratio [Vc/Vg] as a function of normalized current

The X-axis intercept in the clamp ratio ($fs/2\pi f_R$) is found to lie between 0.02 to 0.03 in both experimental results and spreadsheet design results.

5.2 *Small signal model of active clamp buck converter*

As a means of confirmation of the small signal model of the active clamp buck converter, output impedance is measured using the network Analyzer.

The output impedance measurement is done with both the active clamp circuit disabled (hard switched buck converter) and the active clamp circuit enabled for the circuit shown in fig, 9. Fig. 11 shows the magnitude and phase plot of output impedance of the hard switched buck converter and the active clamp buck converter.

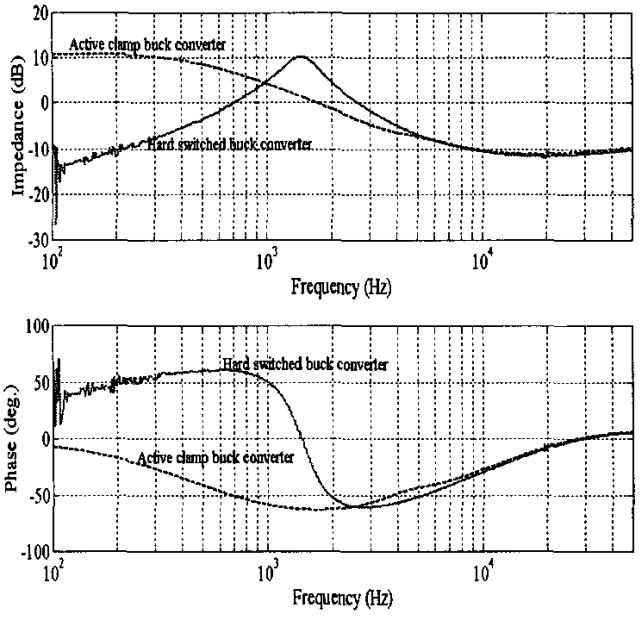


Fig. 11 Measured output impedance of Hard-switched buck converter and Active clamp buck converter

The impedance plot of the hard-switched buck converter shows high Q effect (seen by the peak in the magnitude as well as a sharp change in the phase angle at the natural frequency of the filter). The Q for the hard-switched buck converter is seen to be 2 [5.3dB]. The active clamp converter exhibits damping and resultant low Q. The output impedance does not have complex conjugate poles at all. The damping is quite substantial so that the natural frequencies of the output filter are now all real.

5.3 *Experimental waveforms of active clamp buck converter*

The Experimental waveforms of gating pulses for switches S_1 an S_2, resonant inductor current waveform, drain to source voltage and gate pulses of switches S_1 and S_2 indicating Zero voltage switching, clamp capacitor current and pole voltage waveforms are presented.

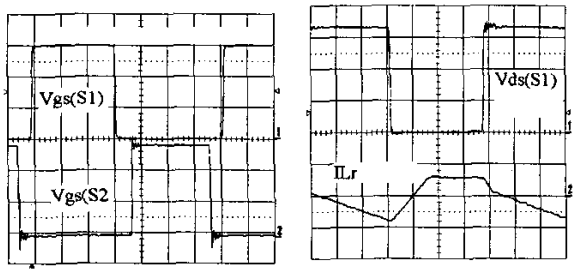


Fig a: Gating pulses for switches S1 and S2; Vds (S1) and Inductor Lr Current

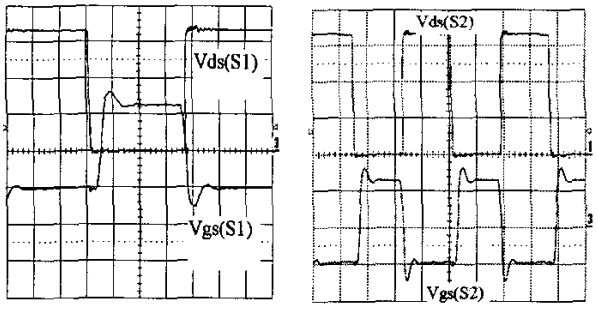


Fig b: Vgs and Vds of S1 showing ZVS; Vgs and Vds of S1 showing ZVS

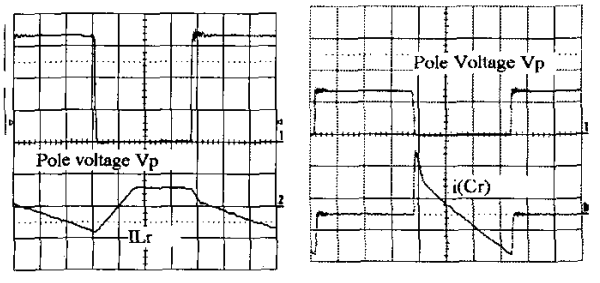


Fig c Pole voltage and Inductor current waveforms; Pole voltage and Clamp capacitor current waveforms

6 *Conclusions:*

Active clamped ZVS converters have become popular recently. This family of converters is derivable from the hard-switched dc-dc converters by addition of resonant circuit elements following simple rules. Though there are a large number of variations present, all these converters are seen to have the same 6 sub-intervals per cycle. Further the circuit equations governing these sub-intervals are identical when expressed in terms of pole current; throw voltage and freewheeling resonant circuit voltage (I, V, and V_C). It is seen that the steady state and dynamic equivalent circuits can be obtained from this idealized analysis. Apart from reducing the switching losses in the converter, the resonant sub-interval introduces lossless damping in the converter dynamics. The most striking result is the simple elegance of the equivalent circuit of this family of converters.

7 *References:*

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