

Digital Dead Time Logic and Protection Circuitry for PWM Voltage Source Converters

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Abstract—Power semiconductor devices have finite turn on and turn off delays that may not be perfectly matched. In a leg of a voltage source converter, the simultaneous turn on of one device and the turn off of the complementary device will cause a DC bus shoot through, if the turn off delay is larger than the turn on delay time. To avoid this situation it is common practice to blank the two complementary devices in a leg for a small duration of time while switching, which is called dead time. This paper proposes a logic circuit for digital implementation required to control the complementary devices of a leg independently and at the same time preventing cross conduction of devices in a leg, and while providing accurate and stable dead time. This implementation is based on the concept of finite state machines. This circuit can also block improper PWM pulses to semiconductor switches and filters small pulses below a threshold time width as the narrow pulses do not provide any significant contribution to average pole voltage, but leads to increased switching loss. This proposed dead time logic has been implemented in a CPLD and is implemented in a protection and delay card for 3- ϕ power converters.

Index Terms—Dead time, independent control, pulse filtering, finite state machine.

I. INTRODUCTION

All practical power semiconductor switches, such as IGBTs and MOSFETs, need a finite time of hundreds of nano seconds to turn on or to turn off. Turning on one device immediately after turning off other device in the leg results in shorting DC bus due to cross conducting at the time of switching [1]. Generally to avoid this shorting of the DC bus is avoided by a by: (1) Taking one pulse per leg and generating its complementary signal for the two switches in a leg of a Voltage Source Inverter (VSI); and (2) The rising edge of each PWM signal is then delayed by a blanking time to generate the gate pulse, which provides the dead time. For this logic to work, the PWM signals to the leg of the converter is assumed to be complementary and does

not yield the direct provision to providing off signals to both switches of the power converter. Independent control over the two devices in a leg will be helpful in inverters to diagnose fault conditions of the converter and its control circuitry, and the connected load. It is also helpful in emulating a momentary open circuit of the leg of the inverter for testing purposes. While controlling the complementary switches in a leg independently, dead time can be provided by just chopping rising edge of the PWM signals, which can be done in the digital controller or using discrete digital components and passive RC network. However, providing dead time for independent control over the two devices of a leg using the aforementioned methods is not a preferred one as it cannot prevent PWM gate signals that try to turn on both the top and bottom devices. To serve better in such a situation a new logic has been proposed and is implemented in a digital platform. It can control the two devices in a leg independently, and at the same time maintaining a high accuracy pre-set dead time that is stable and is independent of ageing. It has additional advantages of being able to maintain the same amount of dead time for all the legs of the power converter, which is helpful for compensating the effect of the dead time using the system controller. This logic is implemented using a Complex Programmable Logic Devices (CPLD) [2]. This facilitates changes in its logic without requiring hardware changes, occupies less space on the printed circuit board, and is immune to circuit parasitic effects and ageing.

II. DEAD TIME LOGIC

The block diagram shown in Fig. 1 shows the conventional method of providing dead time for complementary devices in a leg by chopping rising edge of each PWM pulse. Logically ANDing the signal and its delayed version results in chopping the rising edge of the original signal. The required dead time can be set using the delay network. This delay block can either be an RC network or a flip-flop whose clock period is same as

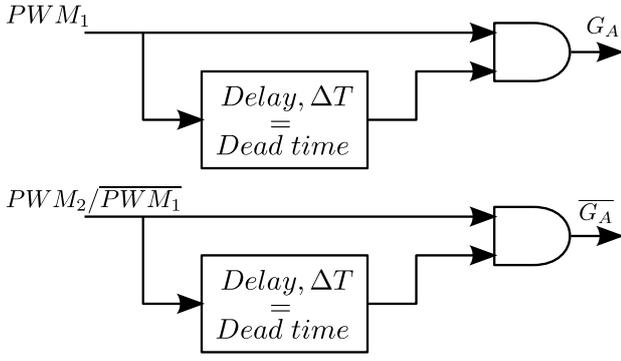


Fig. 1. A simple conventional dead time logic circuit that ensures that complementary switches in the leg are not simultaneously high by making $PWM_2 = \overline{PWM_1}$.

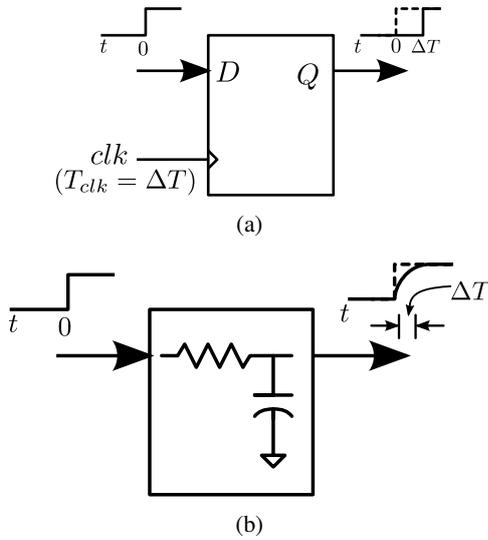


Fig. 2. Types of delay networks for dead time and pulse filtering. (a) Flip-flop based delay network. (b) RC delay network.

that of the dead time as shown in Fig. 2. Passive RC network provides unequal delay for each PWM signal because of the tolerance in the passive elements, which is different for each network and it also varies with inverter cabinet temperature and ageing. If G_A and $\overline{G_A}$ are derived from the PWM_1 signal, the output G_A and $\overline{G_A}$ can not independently be made zero. If G_A and $\overline{G_A}$ are independent signals, then there is a possibility that both can go high simultaneously and can lead to a DC bus short in the inverter. The proposed dead time logic overcomes both these limitations simultaneously using the concept of Finite State Machines (FSM), which is implemented using a CPLD. The concept of FSM is used for implementing the commutation logic of high frequency cycloconverters [3]. This paper discusses its use for the implementing dead time with independent PWM signals to control of the legs of a VSI.

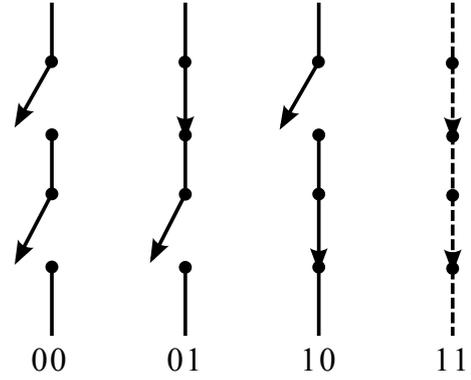


Fig. 3. The possible states of the leg of an inverter. Solid lines indicates the valid states and dotted line indicates invalid state.

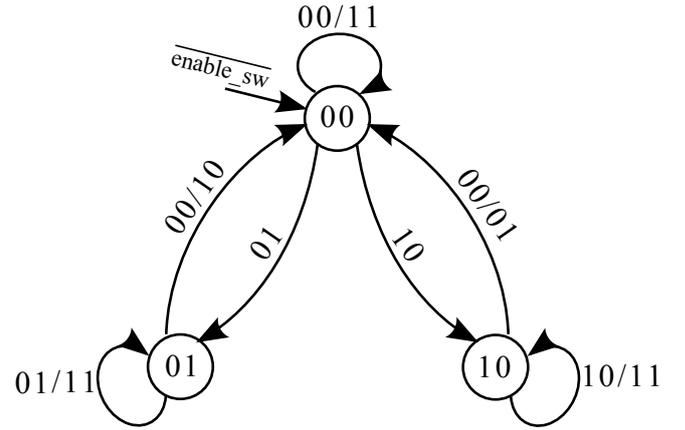


Fig. 4. Finite state machine for implementing the proposed logic for independent PWM signals that is ensured to be valid and with dead time.

A. Proposed Dead Time Logic

In this logic two PWM signals for a leg has been taken as an entity and referred to as a two bit digital word. These PWM signals need not to be complementary. With these signals, consisting of 2-bit digital word, each leg of the converter can have four states as shown in Fig. 3. Among the four states three are valid states “00”, “01” and “10” represented by solid lines and one state is invalid state “11” represented by dotted lines. Invalid state “11” represents the command signals that tries to turn on both the devices in a leg.

Among the valid states one zero state “00” represents the condition when both the devices of a leg are switched off and remaining two valid non-zero states are complementary states. In each complementary state one of the two devices in a leg will be in on state and the other will be in off state. As the number of states of a leg is finite, PWM signals generated by the converter controller can be implemented by using a FSM [4] in which the states correspond to the gate signals of top and bottom devices of a leg of a voltage source inverter. A poly phase inverter

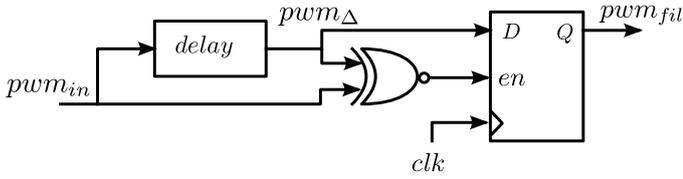


Fig. 5. Functional block diagram of a digital filter small notches and glitches in PWM signals.

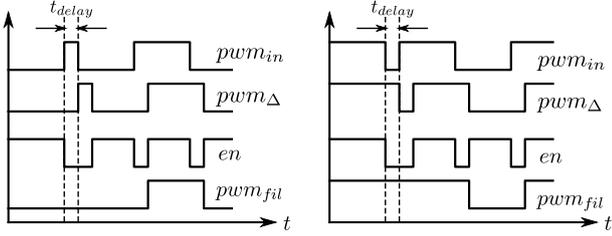


Fig. 6. Illustration of filtering action on PWM signals in the protection and delay card for a voltage source inverter.

would include one such FSM for each of its legs, which is programmed in the CPLD.

In the FSM shown in Fig. 4 there is no direct transition from the state “01” to “10” and vice versa. The only valid path is to go to the zero state “00” to transit from one non-zero state to another non-zero state. This implies that there will be a dead time always and the FSM logic will not allow a device to turn on immediately after turning off the complementary device in the leg. It can stay in any valid state for a long time as long as it is consistent with the PWM command from the controller. Giving an input command for turning on both the devices while one device is already conducting will not result in any transition, which represents the logic that the FSM blocks the invalid state to reach the gate drive card of the converter. These two features are sufficient to drive the complementary devices in a leg reliably with dead time and with independent PWM signals that are generated by the system controller. Also, if the system controller already provides independent signals with adequate dead time, then the proposed logic does not add extra dead time delays to it.

B. Pulse Filtering

At the positive and negative peaks of the modulating signal the duty ratio of the PWM signals will be at the extreme ends. This will result in the gate signals to have the shape of small notches or glitches. In case the turn on or turn off times of these pulses are comparable with the turn on and turn off times of the semiconductor devices, switching the power semiconductor devices by such narrow command signals will have a little contribution to the average pole voltage, but will cause switching power

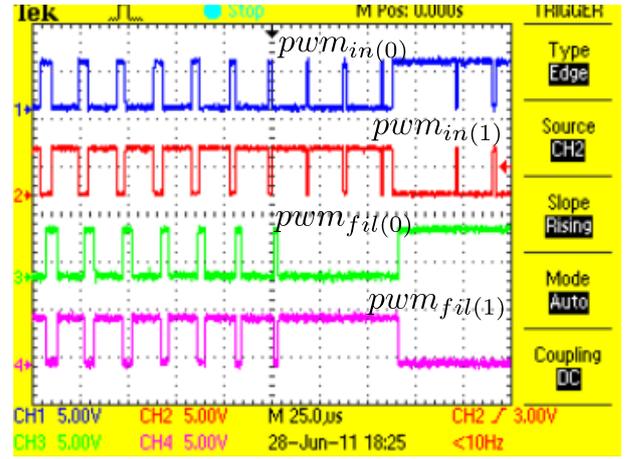


Fig. 7. Test waveforms indicating narrow pulse filtering. All channels are 5V/div, time:25μs/div.

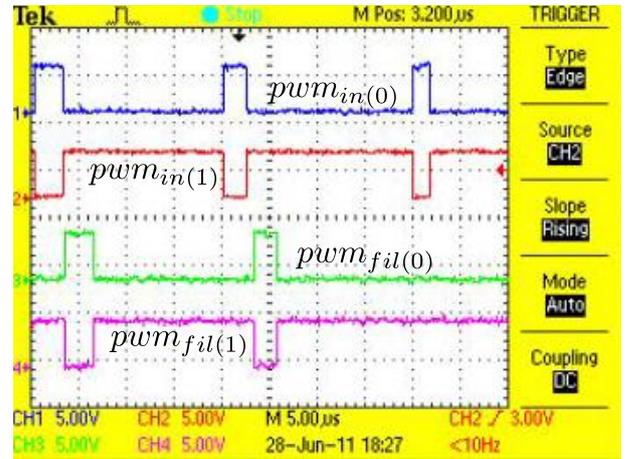


Fig. 8. Test for narrow pulse filtering where pulse of width less than 2μs is dropped. All channels are 5 V/div, time:5μs/div.

loss. Filtering these pulses will reduce switching losses. Fig. 6 is a functional block diagram that is used to filter the PWM signals digitally.

Referring to Fig. 5, the enable to the flip-flop (en) will go to zero whenever the PWM signal has a transition. If the width of the pulse has a time duration is less than Δt_{delay} , then the flip-flop output will not register the pulse. This time duration t_{delay} is the minimum on or off time of the PWM pulse and it can be taken to be of the order of dead time. Fig. 6 shows the complementary PWM pulses wave shapes for both positive and negative narrow pulse filtering corresponding to the logic diagram in Fig. 5.

C. Generalized Protection Card

A generalized protection card [5] has been designed using the proposed dead time logic with pulse filtering. Fig. 9 shows functional block diagram of the designed

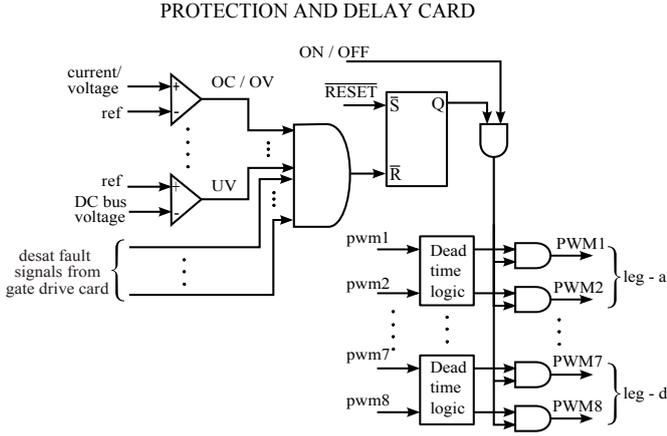


Fig. 9. Functional block diagram of the generalized protection card.

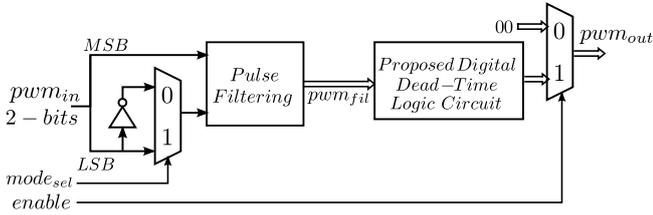


Fig. 10. Complete pulse filtering and dead time logic block diagram corresponding to one leg of an inverter that is implemented in the CPLD.

generalized protection card. Digital dead time logic has been developed using VHDL and is implemented in ALTERA EPM7128-15N CPLD [6]. The designed protection card consists of power converter protection based on:

- 1) 8 V_{CE} sense signals for desaturation detection in 3- ϕ 4 leg inverter,
- 2) 4 over current signals for independent phase and neutral over current protection,
- 3) 2 over voltages, 2 under voltages for a double DC bank of capacitors with consideration of capacitor imbalance and,
- 4) Connector failure detection of the multiple power converter cards such as gate drive card, sensor card, the protection delay card and the system controller card.

All the fault status signals stated are connected in a wired *AND* fashion and detection of any fault blanks all the power semiconductor devices. A status word is send to the digital system controller, which can be decoded for identification of exact type of fault. Processor based and manual rest options have been provided to resume operation of the converter, if appropriate, after a power converter trip due to any fault.

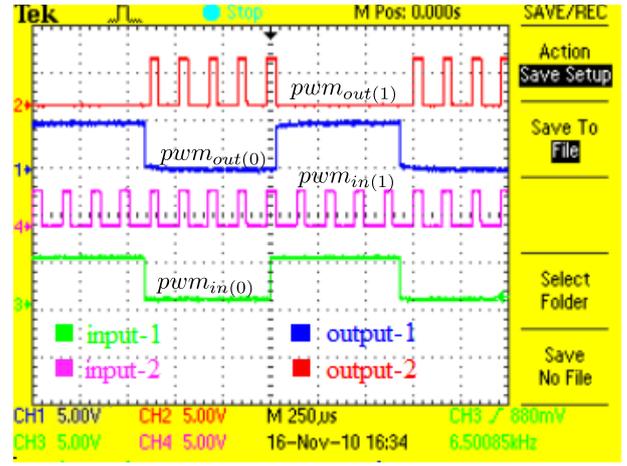


Fig. 11. Test for blocking improper gate pulses. All channels are 5 V/div, time: 250 μ s/div

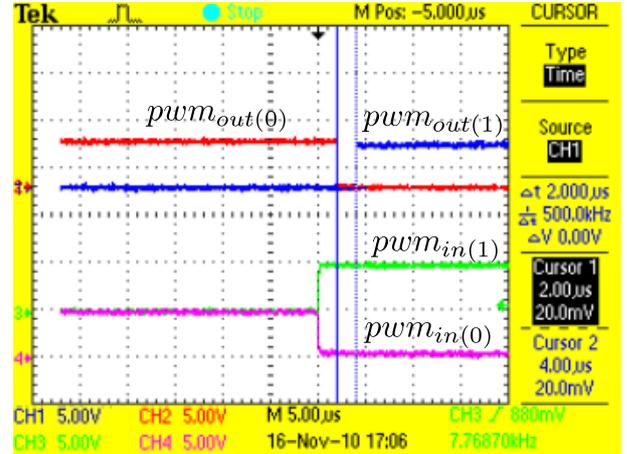


Fig. 12. Test for dead-time with input gating pulses to the leg having no dead-time. All channels are 5 V/div, time: 5 μ s/div.

In Fig. 10 $mode_{sel}$ is to select an option of either independent gating pulses to the leg or the use of only one gate pulse and generating its complementary signal internally. A direct $enable$ is to disable the two devices of the leg is also available, and it is accessible to the system digital controller.

III. RESULTS

The designed protection and delay card has been tested for dead time logic, pulse filtering and operation of the card after identification of fault signals.

To test pulse filtering action, variable duty ratio pulses have been generated from a digital controller and those pulses are given to pulse filtering circuit. The pulse filtering circuit will filter pulses whose on-off time is less than 2 μ s as shown in Fig. 7 and Fig. 8 is enlarged version of Fig. 7 to show the width of the pulse at which filtering action takes place. Pulses of width less than 2 μ s

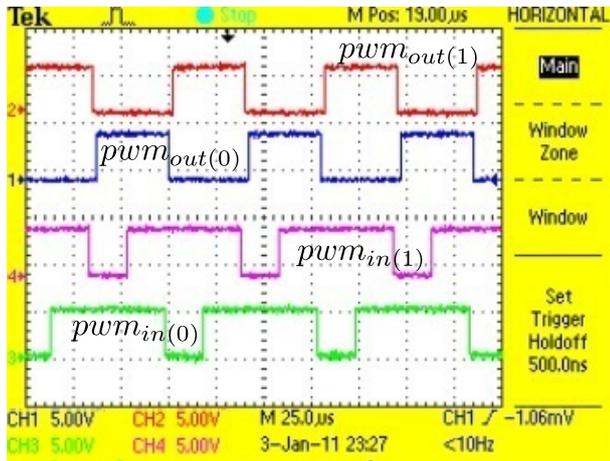


Fig. 13. Test for blocking gate pulses to one device while its complementary device is already conducting. All channels are 5 V/div, time: 25 μ s/div.

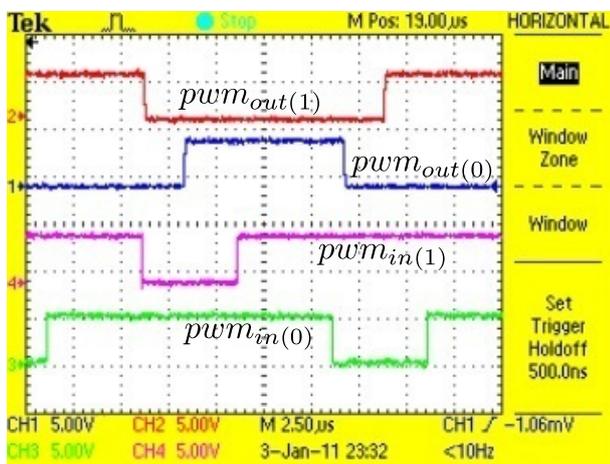


Fig. 14. Test for providing dead-time while blocking improper gate pulses. All channels are 5V/div, time: 2.5 μ s/div.

are eliminated by the filtering. These filtered pulses will go to the dead-time circuit as indicated in Fig. 10.

In Fig. 11 one gating pulse to the leg has high frequency and the other gating pulse is of low frequency. The designed dead time logic circuit is blocking the high frequency gating pulses while the other device is already in conduction.

In Fig.12 two gating pulse to the leg are complementary, there is no dead time in this case. Proposed dead-time logic circuit is providing the pre-set dead time of 2 μ s for this type of input signals.

In Figs. 13 and 14 two gating pulses are trying to turn on one device of the leg while its complementary is already in conduction. The proposed dead-time logic circuit is turning on one device of the leg only after turning off the corresponding complementary device and also providing the pre-set dead-time as can be observed in Fig. 14.

IV. CONCLUSIONS

The proposed digital logic can filter PWM pulses whose turn on and turn off time is very small. It can control two complementary devices in a leg using independent PWM signals and it blocks invalid PWM signals from reach the converter. The digital implementation based on FSM logic has been experimentally validated. Dead time that is provided by the proposed logic is stable and is the same for all legs of the VSI. This type of constant dead time for all legs is helpful to compensate effect of the dead time in current controlled converter easily by adding or chopping, depending on direction of current, the PWM signals by an amount equals to the dead time [7]. The complete logic has been implemented in a CPLD in a prototype generalized protection card that has been assembled and tested.

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