Adaptive Harmonic Elimination Technique in Single Phase PWM Inverters

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***Abstract*—High frequency PWM inverters produce an output voltage spectrum at the fundamental reference frequency and around the switching frequency. Thus ideally PWM inverters do not introduce any significant lower order harmonics. However, in real systems, due to dead-time effect, device drops and other non-idealities lower order harmonics are present. In order to attenuate these lower order harmonics and hence to improve the quality of output current, this paper presents an *adaptive harmonic elimination technique*. This technique uses an adaptive filter to estimate a particular harmonic that is to be attenuated and generates a voltage reference which will be added to the voltage reference produced by the current control loop of the inverter. This would have an effect of cancelling the voltage that was producing the particular harmonic. The effectiveness and the limitations of the technique are verified experimentally in a single phase PWM inverter in stand-alone as well as g rid interactive modes of operation.**

***Key words* – Adaptive filtering, lower order harmonics, PWM inverter, dead time, resonant controller.**

I. Introduction

Presently many distributed generation systems making use of the renewable energy sources are being designed and connected to grid. The power converters form the interface between the energy source and the grid. The interface design is expected to meet the criteria such as: (1) High efficiency of the complete system, (2) Conforming to the standards which specify the amount of harmonic current injection into the grid, (3) Reliability and cost reduction.

The power converter usually consists of a PWM inverter along with filters and transformer in some cases. Fig. 1 shows a power converter topology with an output filter and a transformer. Ideally, this configuration will not have any significant lower order harmonics due to the PWM operation of the inverter. In real system there will be lower order harmonics. The presence of lower order harmonics in the configuration shown is due to:

1) The dead-time introduced between the switchings of devices of the same leg[1]
2) The on-state voltage drops on the switches
3) The saturation characteristics induced magnetizing current drawn by the isolation transformer

A simple solution to the attenuation of lower order harmonics would be to reduce the corner frequency of the filter, which would make the inductor bulky. This is not an attractive option as there would be higher fundamental drop, higher losses and higher cost. Thus in this paper, an adaptive technique is used to attenuate the dominant lower order harmonics. Another method is to use high bandwidth current controllers. However, having higher bandwidth controllers necessitates higher gains, thus increasing the noise susceptibility. Also, this would only attenuate the harmonics and not eliminate them. The proposed method works independently of the main controller while effectively eliminating the undesirable lower order harmonics. Hence with this method, bandwidth for the main controller can be adequately set and at the same time harmonic distortion can be eliminated.

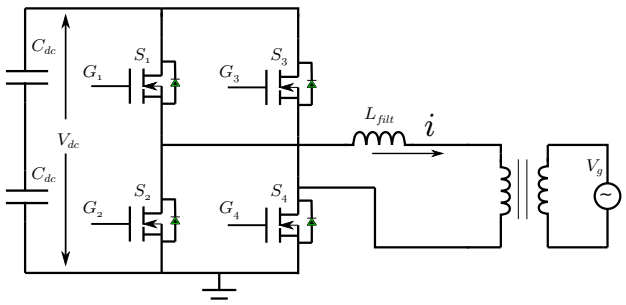


Fig. 1. Schematic of a grid connected 1-ϕ H-bridge inverter connected to the grid through and step-up isolation trasformer.

Reference [2] studies the use of adaptive harmonic elimination for $3-\phi$ inverters with the assumption of an inductive filter between the power converter and the grid. However, studies have not been done in $1-\phi$ dual mode inverter systems with output side transformer that can also be a cause of the harmonics. This paper investigates this system.

II. Adaptive Harmonic Elimination Technique

A. Generalized LMS Adaptive Filter

The adaptive harmonic elimination technique is based on the usage of a Least Mean Square(LMS) adaptive filter to estimate a particular harmonic in the output current and then generate a counter voltage reference to attenuate that particular harmonic. This section discusses the theory of a generalized LMS adaptive filter[6]. The adaptive filters are commonly used in the signal processing applications to remove a particular sinusoidal interference signal of known frequency [3]. The technique discussed in this paper can be considered as an extension of the same. Fig. 2 shows a general adaptive filter with N weights. The weights are adapted by making use of LMS algorithm.

For Fig. 2 coefficient vector is defined as:

$$\overline{w} = [w_o \quad w_1 \quad ... \quad w_{N-1}]^T \tag{1}$$

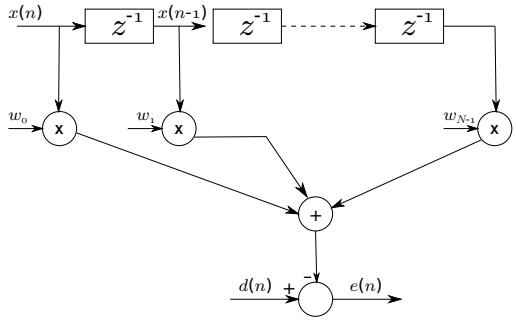


Fig. 2. Structure of a generalized adaptive filter with adaption weights w_i.

Input vector and filter output are given in (2) and (3).

$$\overline{x}(n) = [x(n) \;\; x(n-1) \;\; ... \;\; x(n-N+1)]^T \tag{2}$$

$$y(n) = \overline{w}^T \overline{x}(n) \tag{3}$$

The error signal is,

$$e(n) = d(n) - y(n) \tag{4}$$

Here $d(n)$ is the primary input. A frequency component of $d(n)$ is adaptively estimated by $y(n)$. Now a performance function is defined as

$$\zeta = E[e^2(n)] \tag{5}$$

In any adaptive filter, the weight vector $\overline{w}$ is updated such that the performance function moves towards its global minimum. The performance function in (5) can be expanded as shown in (6) below using (3) and (4)

$$\zeta = E[d^2(n)] - 2\overline{w}^T E[d(n)\overline{x}(n)] + \overline{w}^T E[\overline{x}(n)\overline{x}(n)^T]\overline{w} \tag{6}$$

This is a quadratic function in weight vector $\overline{w}$ and hence a global minimizer exists. Defining $\overline{p} = E[d(n)\overline{x}(n)]$ and $R = E[\overline{x}(n)\overline{x}(n)^T]$, the minimizer occurs for the condition shown in (7). It is obtained by setting the gradient of ζ to zero. $\overline{w}_o$ will be the optimum set of weights.

$$\overline{p} = R\overline{w}_o \tag{7}$$

Thus the updation of weights would be done by moving along the direction of steepest descent as,

$$\overline{w}(k+1) = \overline{w}(k) - \mu \nabla_k \zeta \tag{8}$$

In (8) μ is the step size. The convergence of the adaptive filter depends on the step size μ. A smaller value would make the adaptation process very slow whereas a large value can make the system oscillatory. When the global minimum of ζ is reached, $\nabla\zeta$ will be zero and there will not be any more adaptation in weights.

The generalized algorithm mentioned above applies to all adaptive filters. LMS adaptive filters incorporate a slight modification in the algorithm as in the performance function which is the *expectation of error squared* is approximated to be the *error squared* itself. Thus, for an LMS adaptive filter, the performance function would be,

$$\zeta = e^2(n) \tag{9}$$

From (9), the update equation for LMS algorithm can be deduced. (8) would change as

$$\overline{w}(n+1) = \overline{w}(n) - \mu \nabla e^2(n) \tag{10}$$

∇ is defined as the gradient with respect to the weights of the filter.

Thus,

$$\nabla = [\frac{\partial}{\partial w_o} \;\; \frac{\partial}{\partial w_1} \;\; ... \frac{\partial}{\partial w_{N-1}}] \tag{11}$$

It can be written that,

$$\frac{\partial e^2(n)}{\partial w_i} = 2e(n)\frac{\partial e(n)}{\partial w_i} \tag{12}$$

From (4) and by the assumption that input d(n) is independent of weights, (12) can be expressed as

$$\frac{\partial e^2(n)}{\partial w_i} = -2e(n)x(n-i) \tag{13}$$

Or,

$$\nabla e^2(n) = -2e(n)\overline{x}(n) \tag{14}$$

Combining (14) and (10), the final update equation for weights of an LMS adaptive filter is obtained, which is

$$\overline{w}(n+1) = \overline{w}(n) + 2\mu e(n)\overline{x}(n) \tag{15}$$

B. Adaptive Harmonic Elimination

LMS adaptive filter discussed previously can be used for selective harmonic elimination of any signal, say in the current injected into the grid. In this section, the theoretical treatment of the same is considered.

To reduce a particular harmonic (say i_k) of grid current:

- i_k is estimated from the samples of grid current and phase locked loop (PLL) [5] outputs at that frequency
- A voltage reference is generated from the estimated value of i_k
- The calculated voltage reference is subtracted from the main controller voltage reference. This would have an effect of canceling the voltage that was injecting i_k hence reducing its magnitude

A PLL structure [8] having zero gain at all the frequencies other than fundamental can be used so that distortions are not present in the unit sine and cosine waveform generation.

Fig. 3 shows the block diagram of the adaptive filter that estimates i_k. Suppose k^{th} harmonic of grid current i is to be estimated. The adaptive block takes in two inputs $sin(k\omega_o t)$ and $cos(k\omega_o t)$ from PLL. These samples are multiplied by the weights W_{cos} and W_{sin}. The output is subtracted from the sensed grid current sample which is taken as the error to LMS algorithm. The weights are then updated as per LMS algorithm and the output of this filter would be an estimate of the k^{th} harmonic of grid current.

The weights update would be done by using the equations given below, where T_s is the sampling time, e_n is the error of n^{th} sample and μ is the step size:

$$W_{cos}(n+1) = W_{cos}(n) + 2\mu e_n cos(k\omega_o n T_s) \tag{16}$$

$$W_{sin}(n+1) = W_{sin}(n) + 2\mu e_n sin(k\omega_o n T_s) \tag{17}$$

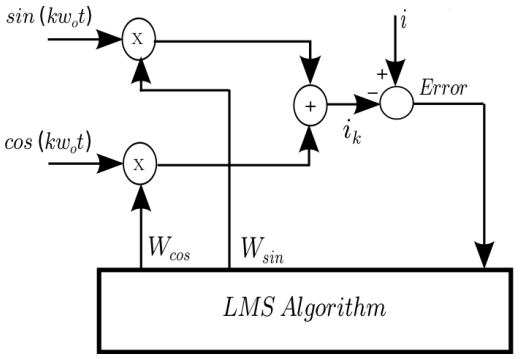


Fig. 3. Block diagram of adaptive estimation of a particular harmonic.

Now a voltage reference has to be generated from this estimated current. The simplest way is to use a proportional gain. Another method reported is to modify Fig. 3 to obtain the direct estimate of the voltage responsible for any particular harmonic[2]. In this work, the proportional gain method is used as it is very simple and gives practically acceptable results.

Fig. 4 shows scheme of the voltage reference generation from estimated harmonic current.

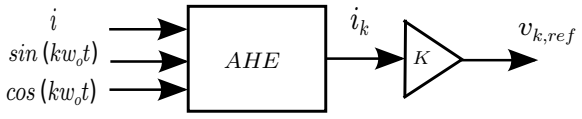


Fig. 4. Generation of voltage reference from estimated k^{th} harmonic component of current.

The proportional gain is designed considering the transfer function for the particular voltage reference produced by the adaptive block and the corresponding harmonic current. It is given by (18)

$$\frac{i_k(s)}{v_{kref}(s)} = \frac{G}{R_s + sL_s} \tag{18}$$

In (18):

- G is the gain which equals $\frac{V_{dc}}{n}$ where n is given by transformer turns ratio $1:n$
- R_s is the net series resistance due to filter inductor and transformer series resistance seen from primary side
- L_s is the net inductance consisting of filter inductance and transformer leakage inductance seen from primary side

Here the inverter is modelled as a pure gain. From Fig. 5 the steady state error in terms of the parameters and K can be evaluated. The transfer function for the error signal e is given by (19) . From (19), the steady state error can be computed.

$$\frac{e(s)}{i_k^*(s)} = \frac{R_s + sL_s}{R_s + KG + sL_s} \tag{19}$$

Depending on allowable steady state magnitude of the harmonic, K can be selected.

The scheme shown in Fig. 4 can be used to eliminate the lower order harmonics. The voltage references generated for these estimated currents would be subtracted from the main reference voltage produced by the closed loop current controller.

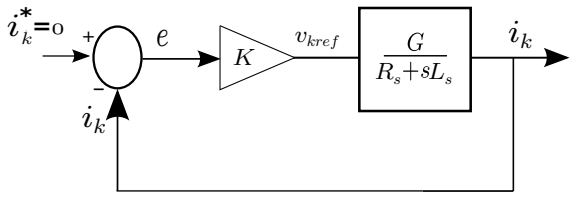


Fig. 5. Control block diagram for selecting the gain K.

III. Closed loop control

A. Conventional Control Scheme

A PWM inverter is usually controlled as a current source in grid connected applications, with a nested two loop control. One dc bus voltage regulation loop and an inner current control loop. The output of current controller, after adding the feedforward terms generates the voltage reference. This voltage reference is compared with a triangular carrier to obtain PWM pulses which will be input to the gate-driver in the inverter hardware. Fig. 6 shows the complete control diagram for a grid connected inverter operating in unity pf.

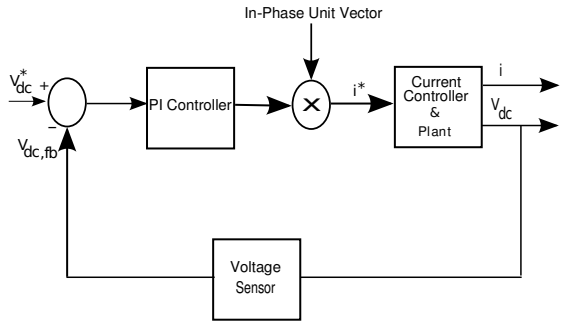


Fig. 6. Block diagram of DC bus voltage and inner current control for a grid connected $1-\phi$ inverter.

The current control diagram is shown in Fig. 7. The single phase case requires the usage of PR controller for zero steady state error[4]. The control design is mainly the design of gains of outer voltage loop and inner current loop. The gains should ensure a stable response with desired speed of reference tracking and zero steady state error.

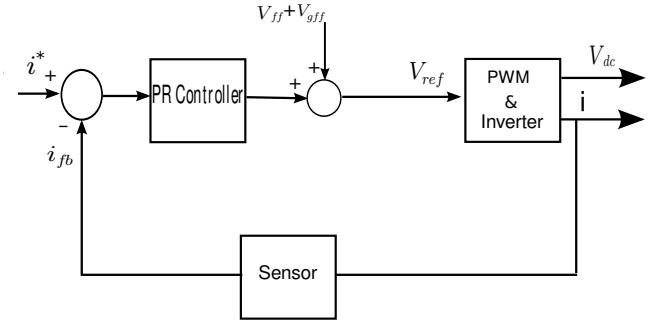


Fig. 7. Proportional-resonant current control loop for $1-\phi$ inverter.

B. Current control with the inclusion of AHE blocks

The adaptive harmonic elimination blocks can be used to attenuate the dominant lower order harmonics. The adaptive blocks are to be connected in cascade to obtain a single voltage reference. This reference would be subtracted from the reference generated by the current controller.

The complete current control with adaptive blocks is shown in Fig. 8. Here the adaptive blocks are used to attenuate the third and fifth harmonics.

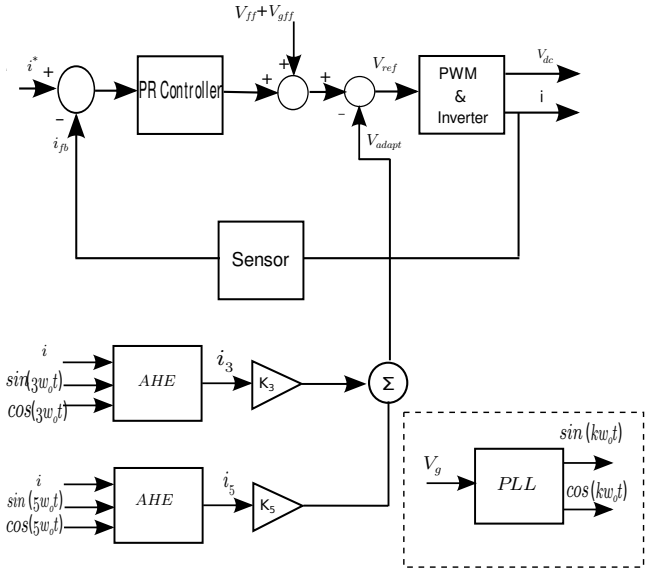


Fig. 8. Current control loop including adaptive blocks.

IV. Experimental Results

The current control with adaptive technique was implemented in hardware for validation. The hardware details and the parameters of AHE technique are listed in Table I. K_2, K_3, K_5 are the proportional gain terms for the adaptive compensation blocks for second, third and fifth harmonic respectively.

TABLE I
Inverter and adaptive control parameters

Parameter	*Value*
DC bus voltage	$40V$
Filter inductance	$667\mu H$
DC bus capacitance	$8.8mF$
Maximum Power	$150W$
Transformer turns ratio	$1:10$
μ	0.08
K_3	32
K_2	32
K_5	24
R_s	0.28Ω
L_s	1.41mH

The experimental verification was done for the following cases:

1) Stand-alone mode without output transformer
2) Stand-alone mode with output transformer
3) Grid connected mode

The control was implemented in Altera EP1C12Q240C8. It is an FPGA chip programmed using any hardware description language. In this work VHDL is used for the programming.

A. Stand-alone mode without transformer

The power circuit topology for this case is shown in Fig. 9. The DC bus is powered with a voltage source and the

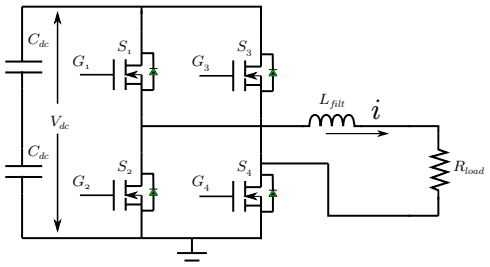


Fig. 9. Power circuit for stand-alone mode without transformer.

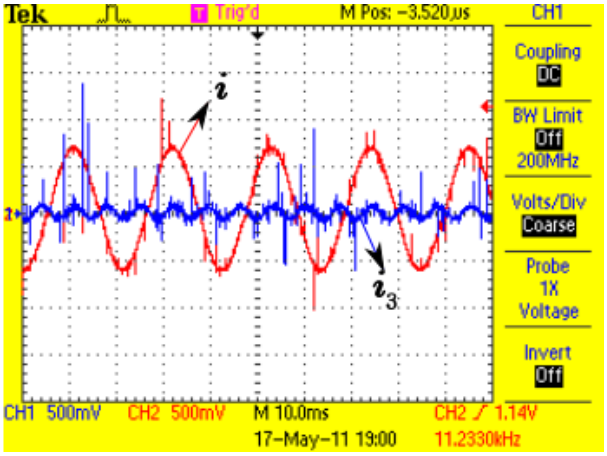
sinusoidal output current is generated after closing the current loop. The importance of testing with stand-alone topology is to highlight the fact that the proposed algorithm works well independent of the output side of the inverter. The method discussed in [2] is applicable only to grid connected topology with the assumption of pure inductive impedance between the inverter and grid. The Figs. 10(a) and 10(b) show the output current with and without adaptive compensation respectively. The compensation is applied for third harmonic alone. The third harmonic estimated in the output current using AHE block is reduced practically to zero when compensation is enabled as can be seen in Fig. 10(b).

B. Stand-alone mode with transformer

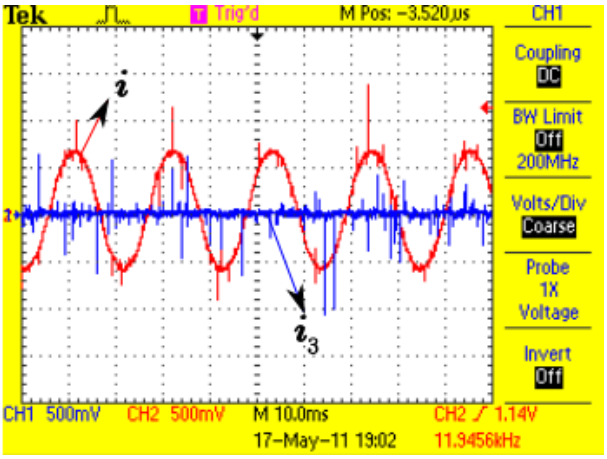
The power circuit topology is shown in Fig.11. In this case, there will be additional distortion due to the magnetizing current drawn by the transformer. Here, the compensation is applied for the secondary current. This is done keeping in mind the grid connected operation of the topology wherein the high-voltage secondary side of the transformer is connected to the grid. The Figs. 12(a) and 12(b) show the waveforms for the cases without and with compensation of third harmonic respectively.

C. Grid connected mode

The power circuit topology for grid connected case is as shown in Fig. 1. In this mode the inverter was controlled as a STATCOM as well as a DG source injecting real power into grid. For this case, apart from the control blocks, a $1-\phi$ PLL [5] is required to generate appropriate ac current reference.
For both upf and STATCOM mode, third harmonic compensation was applied as done in the stand-alone case. The results however showed that the compensation was not effective. It can be seen from Fig. 13(a) that the secondary current, which is the current injected into the grid, lacks half wave symmetry. The same Fig. 13(a) shows the grid current and its second harmonic content. Due to the ripple on the dc bus at 100Hz,



(a) without compensation



(b) with compensation

Fig. 10. Load current[CH2: Red; Scale: 3.2A/1V; marked i] and its third harmonic content[CH1: Blue; Scale: 3.2A/1V; marked i_3] stand-alone without transformer.

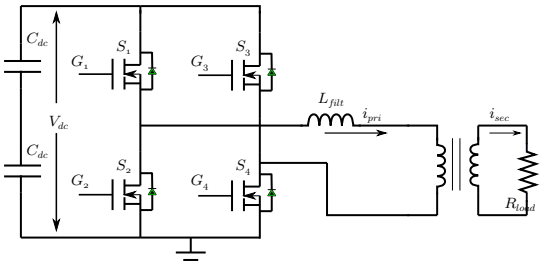
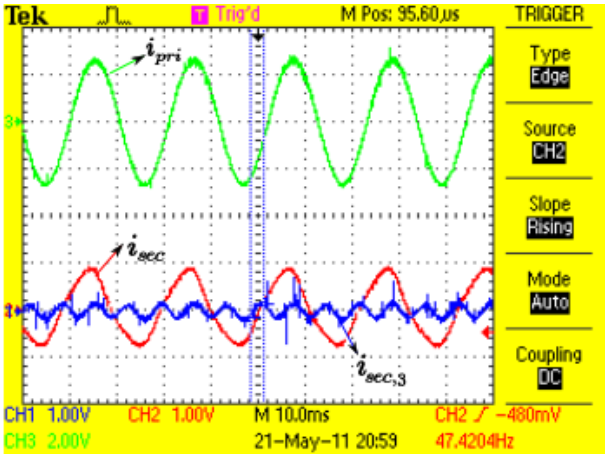


Fig. 11. Power circuit for stand-alone mode with transformer.

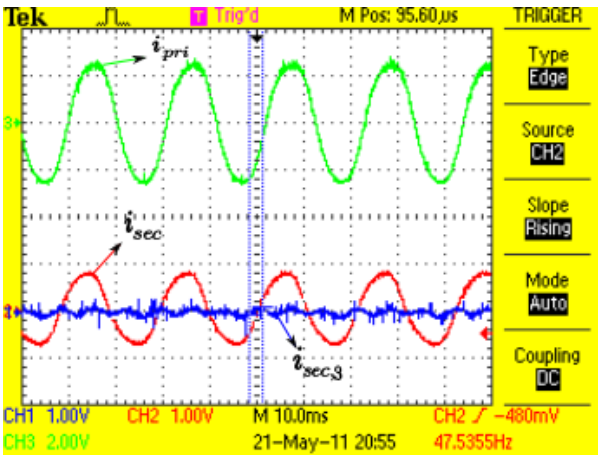
the output current contains even harmonics. The compensation methods available are:

1) Use the AHE technique to add an equivalent second harmonic voltage reference.
2) Pre-multiply current controller output with $V_{dc,ref}$ and divide it by sensed V_{dc}. The output after the division would be the final voltage reference.
3) Use a PR controller for dc bus voltage controller (in addition to PI) at 100Hz[7].

In this work, the adaptive compensation was used. The grid current and its second harmonic are shown in Fig.13(b) after



(a) without secondary side compensation



(b) with secondary side compensation

Fig. 12. Secondary current[CH2: Red; Scale: 1A/1V; marked i_{sec}] , its third harmonic content[CH1: Blue; Scale: 1A/1V; marked $i_{sec,3}$] and primary current[CH3: Green; Scale: 3.2A/1V; marked i_{pri}] stand-alone with transformer.

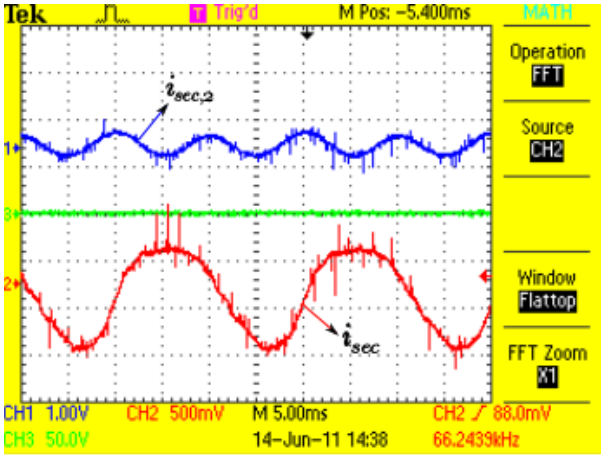
compensation.

From Fig. 13(b) it can be seen that there is an improvement in the grid current wave-shape. However, the adaptive technique to attenuate the distortion due to dc bus ripple might not be a suitable option. The distortion due to dc bus ripple is because of the multiplication of the dc bus voltage to the generated voltage reference. In such case, if a second harmonic reference is added to the main voltage reference, there could be injection of dc component in the output transformer. This is highly undesirable.

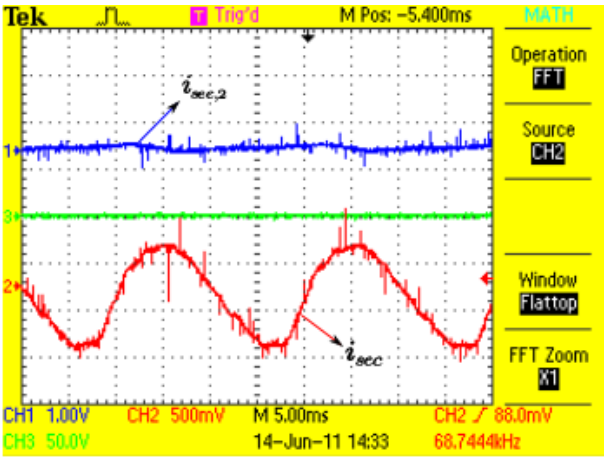
Thus in $1-\phi$ grid connected inverters, alternate methods mentioned can be tested. The adaptive technique is effective to attenuate the distortions which arise due to the additive errors rather than multiplicative errors.

V. Conclusion

In this work, an adaptive technique is described to attenuate the lower order harmonics in PWM inverters. Use of this technique is superior compared to the use of a bulky filter as it would be a lossless technique and does not require increased controller bandwidth. Other advantage is the saving in the cost



(a) Without any compensation



(b) With adaptive compensation of 100Hz

Fig. 13. Grid current[CH2: Red; Scale: 1A/1V; marked i_{sec}], Second harmonic component of grid current[CH1: Blue; Scale: 1A/1V; marked $i_{sec,2}$] for unity pf operation.

of the filter. The technique uses an LMS adaptive filter to estimate a particular lower harmonic to be attenuated and uses a proportional control scheme to generate a counter voltage reference. The effectiveness of the technique was tested in hardware for a single phase inverter with and without output stage transformer. From the experimental results, it is clear that the technique is effective in attenuating the lower order harmonics.

In case of $1-\phi$ grid connected application where there would be lower order even harmonics due to dc bus voltage ripple, this technique might not be a suitable option. This is due to the fact that in large systems there could be injection of dc current if the distortions due to dc bus voltage ripple are attenuated using adaptive technique. Other methods mentioned in the paper can be investigated for the distortions due to dc bus voltage ripple.

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