A Simulation based study & analysis of Double Gate Tunnel FET Performance for Low Standby Power Applications

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Abstract

The conventional metal oxide semiconductor field effect transistor (MOSFET) may not be suitable for future low standby power (LSTP) applications due to its high off-state current as the sub-threshold swing is theoretically limited to 60mV/decade. Tunnel field effect transistor (TFET) based on gate controlled band to band tunneling has attracted attention for such applications due to its extremely small sub-threshold swing (much less than 60mV/decade). This paper takes a simulation approach to gain some insight into its electrostatics and the carrier transport mechanism. Using 2D device simulations, a thorough study and analysis of the electrical parameters of the planar double gate TFET is performed. Due to excellent sub-threshold characteristics and a reverse biased structure, it offers orders of magnitude less leakage current compared to the conventional MOSFET. In this work, it is shown that the device can be scaled down to channel lengths as small as 30 nm without affecting its performance. Also, it is observed that the bulk region of the device plays a major role in determining the sub-threshold characteristics of the device and considerable improvement in performance (in terms of I_{ON}/I_{OFF} ratio) can be achieved if the thickness of the device is reduced. An I_{ON}/I_{OFF} ratio of $2x10^{12}$ and a minimum point sub-threshold swing of 22mV/decade is obtained.

Keywords: Sub-threshold Swing, Tunnel Transistor, Band to band tunneling

1. Introduction

Relentless downscaling of the CMOS technology has led to immense improvements in its performance. However, the switching characteristics of the MOSFET have degraded considerably over the years as a result of scaling. The sub-threshold swing (S) is a very important parameter for any switch. S is defined as the amount of gate voltage needed to change the drain current by 1 decade. It indicates how effectively the MOSFET can be switched OFF by decreasing the gate voltage below threshold voltage (V_{TH}). It also determines the off state current, I_{OFF} (at $V_{GS} = 0$), of the switch. For an ideal switch, S is equal to zero and this leads to a zero off-state current. (Figure. 1)

The MOSFET uses the drift-diffusion mode of carrier transport, and the drain current in the sub-threshold region ($V_{GS} < V_{TH}$) of operation is given by [1],

$$I_{DS} \propto e^{\left[\frac{q(V_{gs}-V_T)}{\eta kT}\right]}\left(1-e^{\frac{-qV_{DS}}{kT}}\right) \quad \text{-- (1)}$$

From the above relation, the sub-threshold swing is obtained to be as follows:

$$S = \left(\frac{d\left(\log_{10} I_D\right)}{dV_{GS}} \right)^{-1} = 2.3\frac{kT}{q}\left(1 + \frac{C_{Si}}{C_{ox}}\right) \quad \text{[mV/decade]} \qquad \text{-- (2)}$$

where, C_{si} = bulk Silicon capacitance and C_{ox} = gate oxide capacitance.

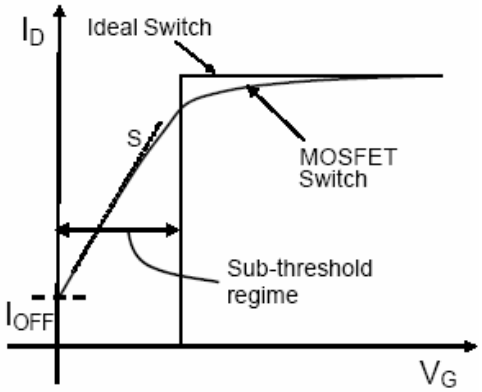

Figure 1: Transfer Characteristics of ideal and MOSFET switch in semi-log scale.

Thus, the minimum possible swing in an ideal MOSFET is S = 2.3kT/q = 60 mV/decade at room temperature (300K). (assuming $C_{si} << C_{ox}$)

The above problem is inherently due to the drift-diffusion mechanism of carrier conduction of the MOSFET where the current is always an exponential function of the gate voltage. Therefore, for future low standby power applications, one requires alternative MOSFET architecture which uses different type of carrier transport mechanism. Various device concepts have been researched and suggested recently.

The Impact Ionization MOSFET (I-MOS) [3], showed characteristics very near to that of an ideal switch. However, due to various problems like V_{TH} shifts due to hot carrier effects, non rail to rail voltage swings and high fields required for operation, it fails to meet the roadmap requirements.

The Tunnel Field Effect Transistor (TFET) [2] with perfect saturation in the output characteristics and exponentially increasing I_{DS} versus V_{GS} has shown a lot of promise for achieving better scaling without severe short channel effects [5]. In the following sections, we discuss in detail, the structure and working of TFET and how it can offer an alternative for future LSTP applications.

Off all the variants of TFET, the Vertical channel TFET (VTFET) [8] with SiGe δ- layer has been the most widely discussed one in the literature. It has shown some very good electrical properties. However, its fabrication, which involves complex processes such as Molecular Beam Epitaxy (MBE) is a very costly and time consuming process.

Thus, it is desirable to have a structure which can be fabricated with the existing process consisting of standard CMOS fabrication steps. In this paper, we study by means of 2D- computer simulations, a planar Double gate structure whose fabrication can be easily integrated with the standard CMOS technology.

2. Device Structure and Operation

The device being studied is the lateral double gate TFET. The TFET is a gated reverse biased p^+-i-n^+ structure which uses the principle of gate controlled Band to Band tunneling for its operation. The schematic of the device is shown in Figure 2. To operate the device, the source is grounded, a positive voltage (1V) is applied to the drain and a voltage is swept across the gate terminals. The simulated band diagrams of the structure are as shown in Figure 3. In the absence of the gate voltage, the tunneling barrier width is much higher than 10nm (the approximate minimum required for tunneling to take place in silicon). However, on application of positive gate voltage (n-type behavior), the bands in the intrinsic region get pulled downwards and a tunneling junction is created at the junction of the p^+-source and the intrinsic channel. Zener tunneling of electrons takes place from the valance band of the source to the conduction band of the channel and the device turns on. Similarly, application of a negative gate voltage creates a layer of holes below the oxide and as a result, the bands in the intrinsic regions get pulled upwards and a tunneling junction is created at the junction of the n^+-drain and the intrinsic channel. The electrons tunnel from valance band of intrinsic region to the conduction band of n^+ region.

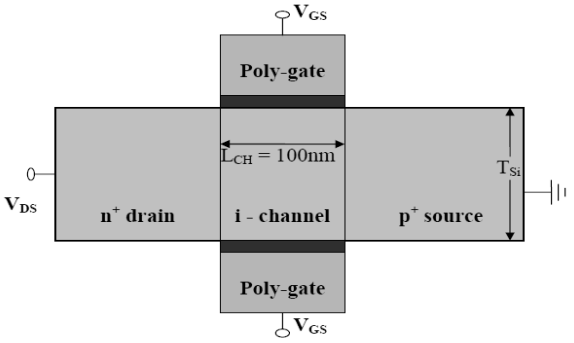

Figure2: Schematic of Double Gate Tunnel FET structure being investigated. (t_{ox}= 2nm)

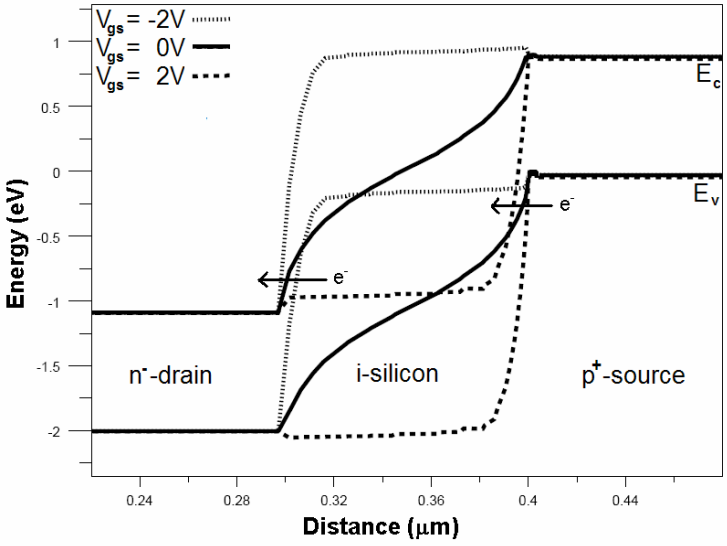

Figure3: Simulated Band diagrams of the Tunnel FET

3. Simulation Tools and Models

2D Device simulations are performed using Medici. Field dependent Kane's model [4] for band to band tunneling available in Medici [10] was used to model the band to band tunneling generation and recombination rate. Kane's model has been shown to give a good match for band to band tunneling in silicon based tunnel transistors at both high and low temperatures [7]. Since the source and drain regions are heavily doped and tunneling is a strong function of bandgap, the bandgap narrowing model (BGN) is also included in simulations. Also, due to high values of doping involved, the Boltzman approximation cannot be used to model the device. Hence, Fermi Dirac statistics are used to improve the accuracy of the simulation at the cost of computational efficiency. For the simulations, a fixed oxide thickness, t_{ox}=2nm is chosen. The n^+ drain is doped $2x10^{19}cm^{-3}$, the p^+ source is doped $1x10^{20}cm^{-3}$, and the substrate is doped $1x10^{16}$ p-type, corresponding to the substrate doping in the standard CMOS process.

4. Simulations and Analysis

The transfer characteristics of the double gate tunnel FET are as shown in Figure 4.

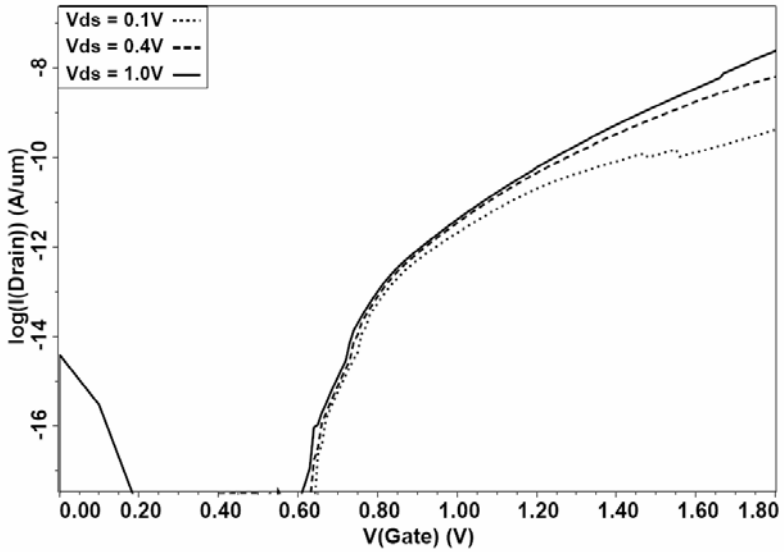

Figure 4: Transfer characteristics of a tunnel FET for various values of drain voltages.

The output characteristics of the device are as shown in figure 5. As compared to the α power dependence on V_{GS} in MOSFET, the behavior seen here is of a much higher order. Also, due to the reverse biased structure, the output impedance of the device is very high. This makes it highly suitable for analog applications such as amplifiers and current mirrors.

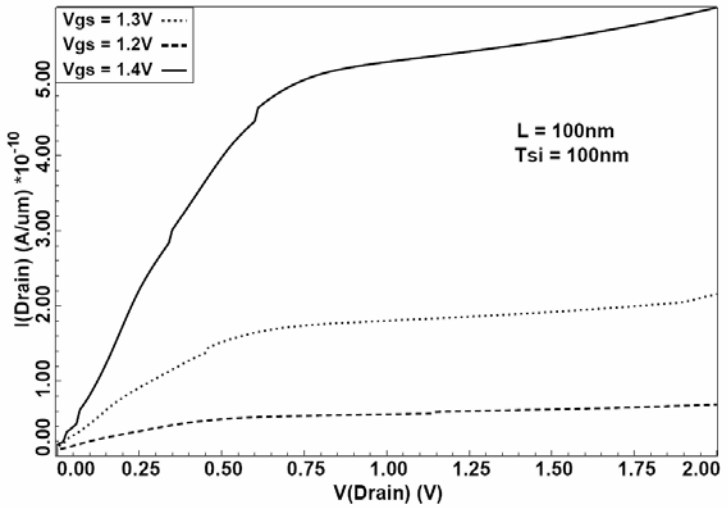

Figure 5: Output characteristics of the double gate tunnel FET.

According to Kane's model, the relation for band-to-band tunneling generation rate is given by

$$G_{B2B} = A_{kane} E^2 W_g^{-1/2} e^{-B_{kane} W_g^{3/2}/E} \tag{3}$$

where,

A_{kane} and B_{kane} are material dependent constants and can be considered independent of the bias conditions.

W_g is the tunneling junction width and E is the electric field at the tunneling junction.

Using the above relation for band-to-band generation and recombination rate, an expression (equ. 4) for the sub-threshold swing of tunnel transistors has been derived in [9]. This derivation is based on two assumptions

(i) The tunneling width (ω), which is gate controlled, is independent of the drain bias. This can be seen from the band diagrams in Figure 6.

(ii) The tunneling electric field (E) is also fairly independent of the drain bias and can be approximated by a relation $E= DV_{GS}^2$, where D is a constant.

$$S = \frac{DV_{GS}^2}{2DV_{GS} + B_{kane} W_g^{3/2}} \tag{4}$$

From the above relation, it is seen that the S of a tunnel FET is a strong function of the gate voltage. Hence, the value of S is very good for lower gate voltages (sub-threshold region) but degrades considerably for higher gate voltages (saturation region) Figure 7 shows the variation of S as a function of the gate voltage for the double gate tunnel FET.

However, it is observed that these assumptions are true only in the surface region (the region very close to the gate terminal) of the device where the bands bend due to the gate work-function. In the bulk region, since the intrinsic channel is fully depleted, the bands in the channel are straight lines (figure 8) as compared to the curved bands in the case of surface region. Therefore, as clearly seen in

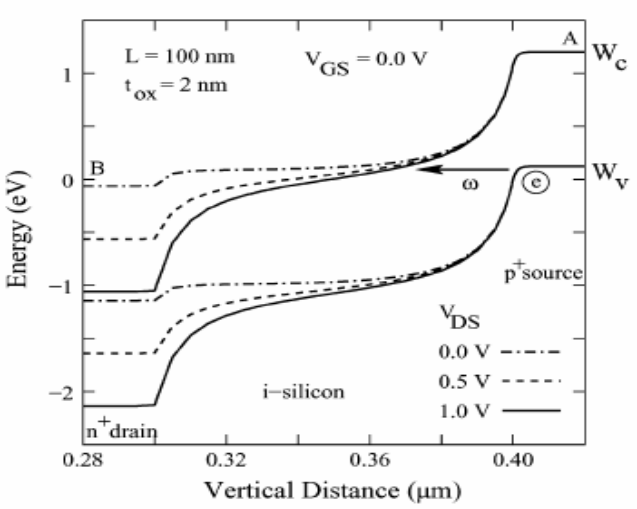

Figure 6: Simulated band diagrams of VTFET (near the surface region) with increasing V_{DS} at fixed V_{GS}=0. The tunnel barrier width ω is nearly independent of V_{DS} [9]

figure 8, the tunneling width reduces considerably with increase in drain bias in the bulk region.

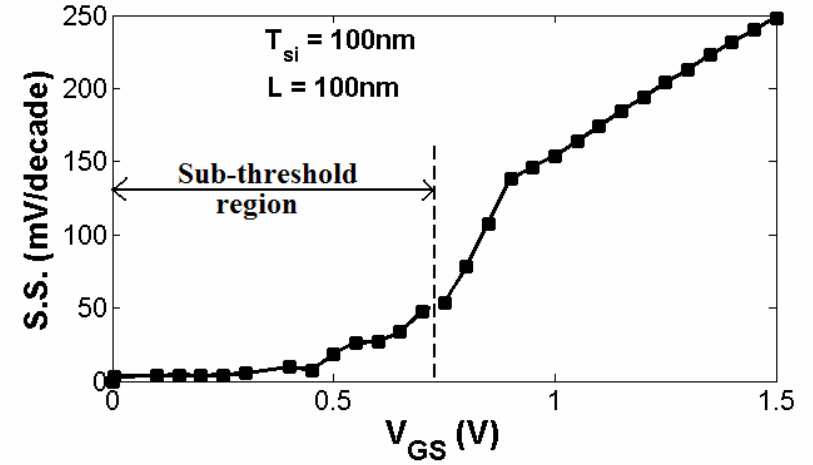

Figure 7: Sub-threshold swing (S) of double gate tunnel FET as a function of the gate voltage. (V_{DS} = 1.0V). S degrades considerably as the device moves from sub-threshold to saturation region

It is also observed (figure 9) that the tunneling electric field (E) is fairly constant with respect to V_{DS} in the surface region but increases linearly with the drain bias in the bulk region.

Since the effect of gate is negligible in the deep seated region of the device, this region is responsible only for the off-state current (I_{OFF}) of the device. Thus, the reduction in ω and an increase in E with an increase in drain bias should lead to an increase in the I_{OFF} of the device. As a result of that, the I_{ON}/I_{OFF} ratio should degrade at higher V_{DS}.

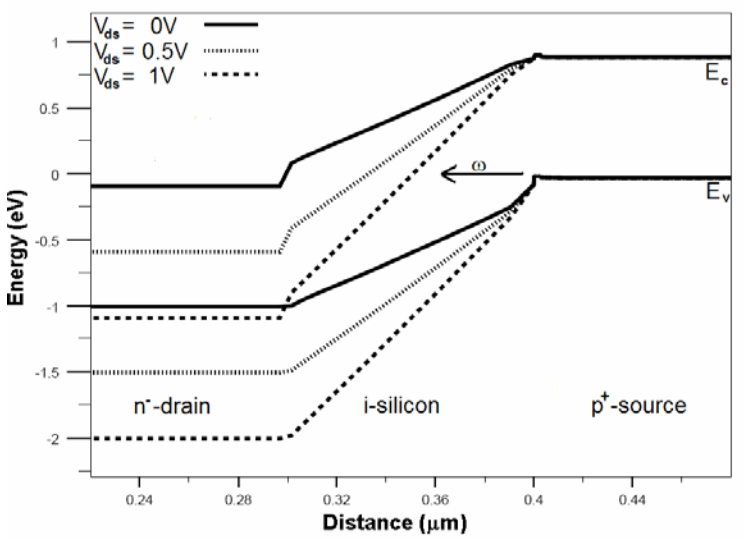

Figure 8: Simulated band diagrams of DGTFET (in the bulk region) with increasing V_{DS} at fixed V_{GS}=0. Tunneling barrier reduces significantly due to increase in V_{DS}

We also need to note that equ. 4 does not take into account the variation of ω and E with respect to V_{DS} in the bulk region. Hence, the value of S predicted by this equation will not be as accurate as it should be. One should keep in mind that this (deviation) happens only at higher drain voltages. The obtained values of S agree very well with the expected values for low drain bias. Figure 10 shows the variation in the minimum point sub-threshold swing S_{min} and I_{ON} to I_{OFF} ratio with V_{DS} for a fixed device. For very low drain voltages (below 0.4V) the I_{ON} of the device is very low and as a result, the I_{ON}/I_{OFF} ratio is not very good. The device shows excellent parameters for V_{DS} between 0.4 and 1.2V.

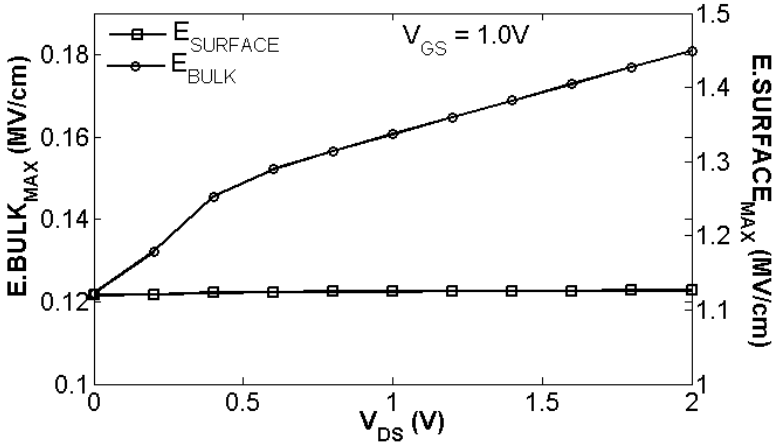

Figure 9: Simulated maximum electric field E_{max}, across the tunnel junction as a function of V_{DS} in the bulk and surface regions of the device. The field is independent of V_{DS} at the surface but varies considerably with drain bias in the bulk region.

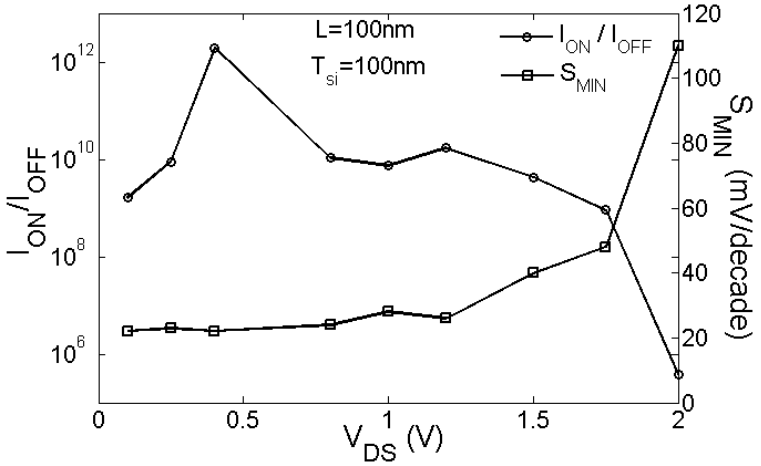

Figure 10: Simulated I_{ON} to I_{OFF} ratio and minimum point Sub-threshold Swing as a function of V_{ds}. As predicted, both the values degrade a lot for higher drain bias

However as we increase the drain bias above this value, both these parameters degrade drastically.

From the analysis above, we can conclude that significant reduction in I_{OFF} of the device can be achieved without affecting the I_{ON} of the device if the thickness of the device is reduced.

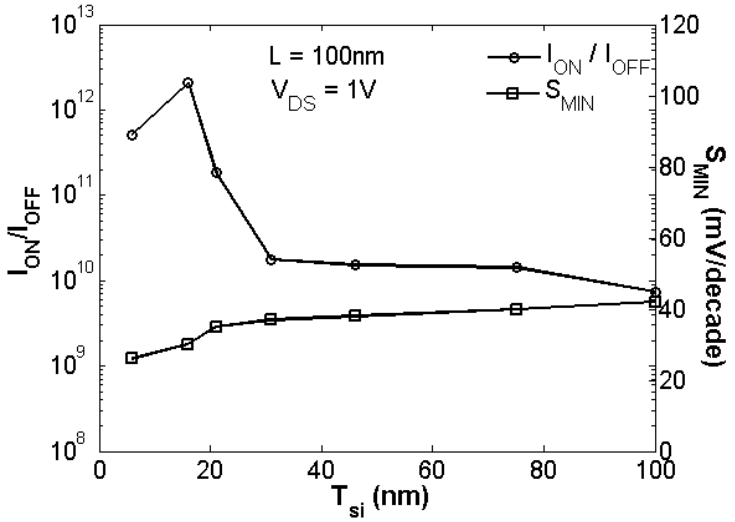

Figure 11: Simulated I_{ON} to I_{OFF} ratio and minimum point Sub-threshold Swing as a function of T_{si}. As expected, both the parameters improve when the body thickness is reduced

The above conclusion was verified using 2D device simulations in Medici. The thickness (T_{Si}) of the double gate structure in figure 2 was varied and the results noted down. It was found that the I_{ON}/I_{OFF} ratio and the sub-threshold swing improved considerably for the thin body device when compared to the thicker structure. Figure 11 shows the improvement in device behavior with reduction in

T_{si}. The I_{ON}/I_{OFF} ratio is seen to degrade for T_{si} less than 10nm. This is because for very thin devices, the on-current (at V_g=1.5V) starts to drop (due to the reduction in the area). Hence, there is a maximum in the I_{ON}/I_{OFF} vs. T_{si} curve at $T_{si} \approx$ 10nm.

5. Scaling of double gate TFET

As we have seen, the active region of the TFET is only the tunneling junction between the source and the intrinsic region of the structure. As a result, the

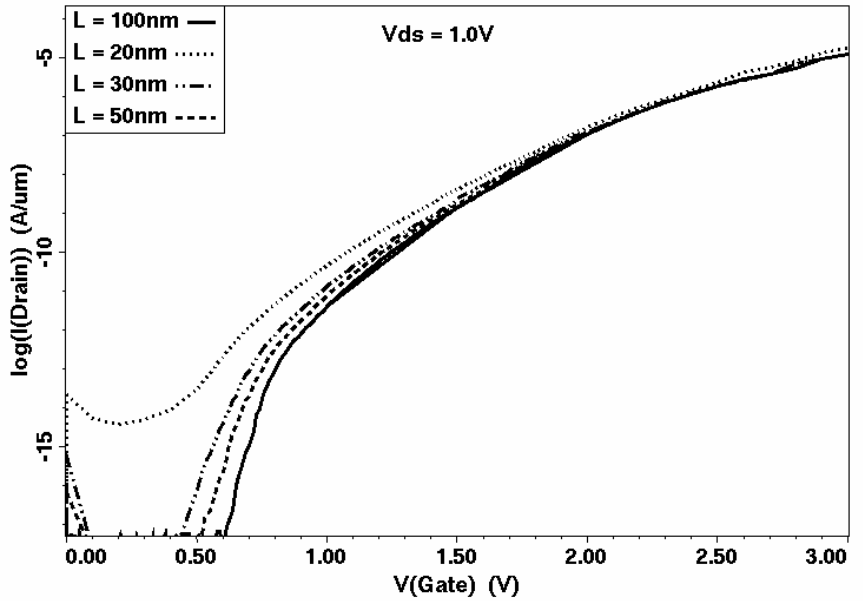

Figure 12: I_{DS} vs. V_{GS} characteristics of the double gate tunnel FET with different channel lengths. The characteristics deviate from normal for the 20nm length device.

device performance is nearly independent of the channel length. This was verified using 2D device simulation. It was found that the main electrical parameters (namely the sub-threshold swing and the I_{ON}/I_{OFF} ratio) were found to remain unchanged upto a channel length of 30nm. However, the parameters degraded below this value of the channel length. This is because the gate length is too less and as a result the gate is not able to bend the bands enough for conduction to take place. Figure 12 shows the variation in $\log_{10}I_{DS}$ vs V_{GS} curves with channel length.

6. Conclusion

In this paper, the double gate TFET was explored using 2D device simulations. Due to the tunneling mechanism involved in its carrier transport, unlike the MOSFET, TFET does not have any physical lower limit to the sub-threshold swing. Also, due to the reverse biased structure, the leakage current is extremely low. Both these properties make the TFET highly suitable for Low-Standby Power applications. It is observed that the bulk of the device plays a major role

in degrading the I_{ON}/I_{OFF} ratio and the S of the device. Using simulations, it is verified that both these parameters can be improved by reducing the thickness (and hence the amount of bulk region) of the device. It is also seen that the TFET performance is nearly independent of the channel length and the device (in its present form) can be easily scaled upto 30nm channel lengths.

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